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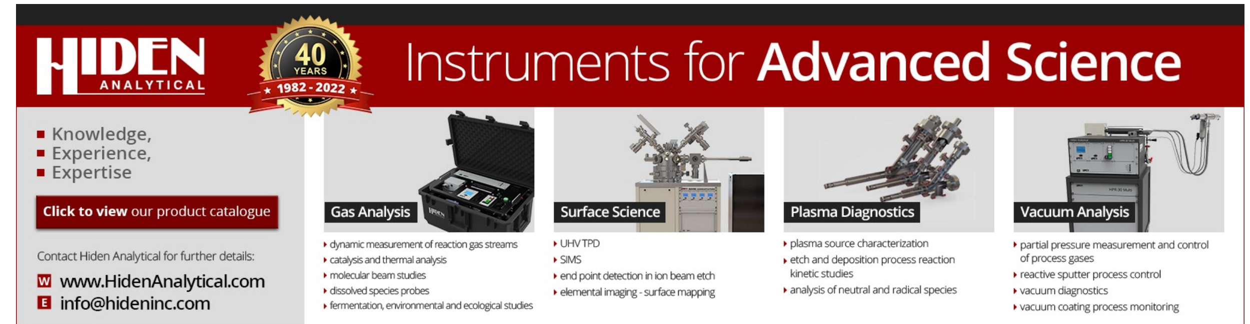

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Study of SnO/ε-Ga_2O_3 *p–n* diodes in planar geometry

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ABSTRACT

SnO/ε-Ga_2O_3 vertical *p–n* diodes with planar geometry have been fabricated on *c*-plane Al_2O_3 and investigated by current–voltage measurements. The effects of the in-plane conduction through the Si-doped ε-Ga_2O_3 layer on the diode performance and their relevance have been evaluated. A significant series resistance is observed, which shows typical features of the variable range hopping transport observed in Si-doped ε-Ga_2O_3; this in-plane transport mechanism is probably induced by the columnar domain structure of this polymorph. The dependence of the series resistance on the geometry of the diode supports the interpretation. A simple equivalent model is presented to describe the experimental behavior of the diode, supported by preliminary impedance spectroscopy investigation.

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I. INTRODUCTION

The research on wide bandgap semiconductors for power electronics is extending very rapidly with particular focus on the family of Ga_2O_3.[1–5] Five polymorphs of this oxide are known, with the monoclinic β-Ga_2O_3 being the thermodynamically stable one.[6] Bulk crystals can be obtained for such a phase,[6] while the other polymorphs can be obtained by different epitaxial techniques.[7] Unintentionally doped β-Ga_2O_3 single crystals are *n*-type with carrier residual concentration in the order of 10^{16}–10^{17} cm^{-3},[8] which can be compensated by Fe or Mg doping to get high-resistivity material.[9,10] On the other hand, the spontaneous *n*-type conductivity can be enhanced by Si and Sn doping to reach electron concentration up to 10^{18}–10^{19} cm^{-3}.[6] Common to all phases of the Ga_2O_3 family is a nearly flat valence band, which prevents effective p-type conduction.[11,12] This physical property led to the preferential development of unipolar n-type electronic devices, such as Schottky diodes and field effect transistors.[13]

β-Ga_2O_3 has been largely used for device fabrication, although presenting some drawbacks mainly related to the low symmetry of its monoclinic structure (e.g., anisotropy in thermal conductivity,[14] presence of cleavage planes,[6] and growth rate as a function of the crystal orientation and related defects[15]), which poses several challenges for the development of devices and their performances.[13] Moreover, the heteroepitaxial deposition of the material on conventional substrates for integrated devices usually leads to the formation of electrically charged domains[16] that so far limited the employment of this polymorph for power electronics to single crystals and/or homoepitaxial layers grown on specific orientations [i.e., (010)[17] or off-cut (100) β-Ga_2O_3 substrates[18]].

For this reason, the interest in other Ga_2O_3 phases is increasing. For instance, the ε-Ga_2O_3 polymorph presents more isotropic physical properties and thermal conductivity with respect to the β-phase, easier epitaxial deposition, and better matching to commercial substrates (e.g., sapphire), while maintaining acceptable thermodynamic stability, up to about 850 °C.[19] This phase has an orthorhombic lattice that can be heteroepitaxially grown on several substrates,[7] always in the (001) orientation. Nonetheless, it exhibits

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a columnar domain structure arranged in pseudohexagonal symmetry.[20] Recently, it has been suggested that the occurrence of such rotational domains could limit the in-plane electronic conductivity,[21] which could imply a different axial and in-plane conductivity. A strategy toward isotropic conductivity could be based on the use of misoriented substrates[18] or unconventional substrates[22] in order to induce step-flow growth and avoid the domains. A similar strategy proved to be successful for epitaxial β-Ga_2O_3 films.

Successful *n*-type doping of the epsilon phase was demonstrated either by adding Si during the epitaxial growth or by *ex situ* Sn-diffusion (net doping levels of few 10^{18} and $10^{17}\,cm^{-3}$ have been obtained for Si and Sn doping, respectively). In both cases, a hopping in-plane transport was observed.[23,24] However, vertical transport is expected to be less influenced by domains, owing to their columnar structure.

The literature on power electronic devices based on β-Ga_2O_3 is extensive,[13] and the reported performances of vertical β-Ga_2O_3 Schottky diodes are remarkable: barrier height of 1.1 eV, rectification ratio of 10^{10}, breakdown voltage up to 1600 V, and a current density at 2 V in the range 50–100 A/cm^2 have been already demonstrated.[25–27] On the other hand, only few articles so far dealt with an ε-Ga_2O_3 based diodes.[21,28–30] Some of these devices were vertical *p*–*n* heterojunctions using the *p*-type oxides NiO and $ZnCo_2O_4$ vertical Schottky barriers, prepared on the conductive template to avoid any in-plane conduction through the ε-Ga_2O_3 layer. A rectification ratio of about seven orders of magnitude has been obtained in the best case and a built-in potential of about 2.1 V.[21] A quasivertical diode structure[28] and planar organic–inorganic hybrid heterjunctions[29,30] have also been proposed for the application in UV-C radiation photodetection.

However, a planar geometry becomes necessary when the diodes are fabricated on insulating substrates. In this case, there are two ways to obtain *p*–*n* junctions: (1) the deposition of *n*-type ε-Ga_2O_3 on a conductive *p*-type layer stacked on an insulating substrate, followed by etching of the top layer in selected areas in order to contact the underlying *p*-type film, then contacting the *n*-type top film; (2) growing a *p*-type layer on selected areas of the *n*-type ε-Ga_2O_3 deposited on the insulating substrate, then fabricate specific ohmic contacts on the *p*- and on the *n*-type layers. In such structures, the current that crosses the junction may encounter a significant series of resistance as it has to flow parallel to the top surface to reach the ohmic contacts (see Fig. 1).

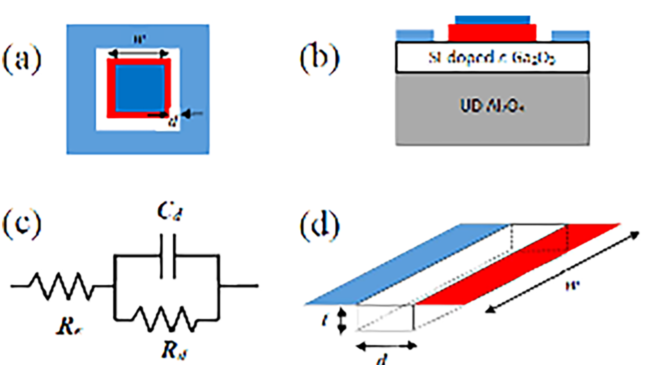

FIG. 1. Sketch of a SnO/ε-Ga_2O_3 diode: (a) top view and (b) cross view. White area: n-type Ga_2O_3 layer. SnO p-typer region is the central squared isolated column in contact with the Ga_2O_3 layer. Ohmic contacts (Ti/Pt/Au stack) are deposited on top of SnO and of Ga_2O_3. (c) equivalent circuit of the structure: R_e represents a resistance in series with the junction, C_d and R_d represent the depletion capacitance of the diode and the leakage resistance, respectively; and (d) sketch of one of the four channels of in-plane current flow between SnO/ε-Ga_2O_3 junction and the ohmic contact around. The ohmic contact is on the left of the ε-Ga_2O_3 channel (in white), hetrojunction is on the right.

In this work, SnO/ε-Ga_2O_3 *p*–*n* heterojunctions of different dimensions, in a planar geometry, were investigated. We report here on the temperature dependent current–voltage characteristics and discuss the limitations of this fabrication approach.

II. EXPERIMENT

Si-doped ε-Ga_2O_3 epitaxial layers were grown by metal-organic vapor phase epitaxy on *c*-oriented sapphire at 600–610 °C, using trimethylgallium and ultrapure water as precursors, with H_2 as carrier gas; *n*-type extrinsic doping was achieved by injecting a diluted mixture of 0.05% SiH_4 in pure H_2 into the growth chamber. Other details of the ε-Ga_2O_3 growth are reported in Ref. 23. The layer thicknesses of the sample in this study were about 550 nm; *n*-type conductivity, Hall density of $3.7\times10^{18}\,cm^{-3}$, Hall mobility of about 4 cm^2/Vs, and resistivity of 0.4 Ω cm were measured at room temperature (RT) on the as-grown layer by the van der Pauw method. After a thermal treatment of the sample to simulate the effects of the process required by the subsequent deposition of SnO, a slight increase of resistivity to 0.5 Ω cm was observed, with a corresponding reduction of the Hall density to about $3.1\times10^{18}\,cm^{-3}$ and a mobility decrease to 3.5 cm^2/Vs.

A 150 nm-thick SnO(001) layer was grown on top of the ε-Ga_2O_3 epitaxial layers by plasma-assisted molecular beam epitaxy (PAMBE). During PAMBE growth, Sn was evaporated from a shuttered single filament effusion cell operated at 1175 °C corresponding to Sn beam equivalent pressure of ~2.7×10^{-7} mbar. Activated oxygen was provided by passing O_2 through a radio frequency plasma source run at 200 W. The Sn-to-O plasma flux ratio and growth temperature window for SnO is limited due to the formation of secondary Sn and SnO_x ($1 < x \le 2$) phases. Hence, in this work, all the films were grown at an optimized substrate temperature of 350 °C and O_2 flux of ~0.18 SCCM.[31] The RT Hall measurement in the van der Pauw geometry of a reference SnO(001) layer on YSZ(100) indicated *p*-type conductivity with a Hall hole concentration $p = 5.87\times10^{18}\,cm^{-3}$, Hall mobility $\mu = 3.1$ cm^2/Vs, and resistivity $\rho = 0.33$ Ω cm. X-ray diffraction is used to structurally investigate the grown SnO(001)/ε-Ga_2O_3 heterostructure. As shown in Figs. S1–S3 in the supplementary material,[32] an SnO film consisting of (001) oriented grains without in-plane epitaxial relation to ε-Ga_2O_3 was grown on the high quality ε-Ga_2O_3 layer which crystallized phase pure and (001)-oriented in epsilon phase.

To isolate SnO square shaped pads [geometry reported in Figs. 1(a) and 1(b)], the sample was subsequently processed, using photolithography resist patterning, followed by 250 nm-deep mesa etching using a reactive plasma ion etching process as described in Ref. 28. For the top contact, we deposited square shaped of 20 nm Ti/100 nm Au metal layers, with linear dimensions ranging

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TABLE I. Geometrical details of the diodes (see Fig. 1): *w* is the side length of the *p*-type area and *d* is the distance between SnO *p*-type layer and ohmic contact to Ga_2O_3. The fifth column reports for each diode the theoretical resistance calculated from Eq. (1), R_e^{teo}, normalized to that one of diode-1 ($R_{e,1}^{teo}$), where *t* is the thickness of ε-Ga_2O_3 after the mesa etching (450 nm). The last column gives the averaged R_e experimental data, R_e^{exp}, obtained from the *I–V* data of sets of diodes of equal size (see the text).

Structure	Side length w (μm)	Distance d (μm)	$d/4\,wt$ (cm^{-1})	Relative $R_e^{teo}/R_{e,1}^{teo}$	R_e^{exp} (Ω)
Diode-1	200	10	278	1	1090
Diode-2	150	10	370	1.33	1230
Diode-3	100	10	556	2.0	2280
Diode-4	70	10	794	2.85	2900

between 55 and 180 μm on top of the SnO layer, using electron-beam evaporation and the liftoff process without additional annealing step. Despite the absence of contact annealing to prevent the transformation of the SnO layer into *n*-type SnO_x (Ref. 33), these contacts are ohmic.[31]

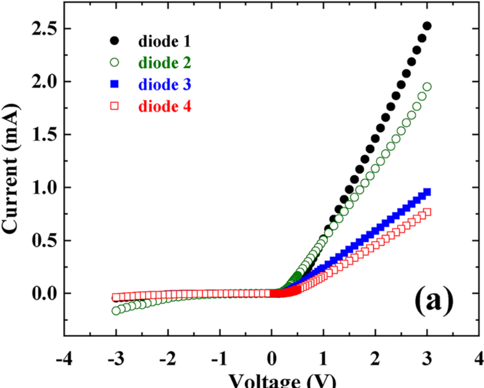
Ohmic contacts on the ε-Ga_2O_3 layer were prepared using 20 nm Ti/100 nm Au metal layers to form a square frame around each SnO mesa at a distance from the latter of $d = 10\,\mu$m (see Fig. 1). Table I gives the values of *w* and *d* for the tested diodes. No passivation of the Si-doped ε-Ga_2O_3 surface was carried out.

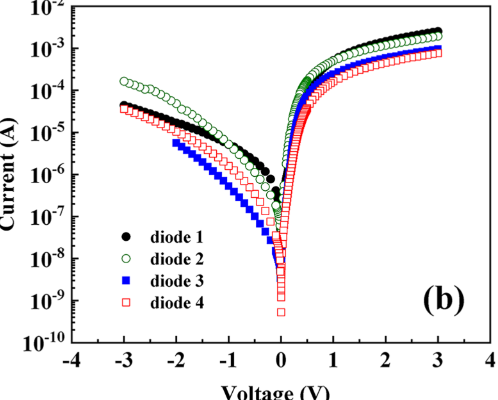
Current–voltage data were measured on the diodes using a Source-Meter Keithley Mod. 2400. Preliminary impedance investigation on a selected structure was also performed at RT, acquired using an HP 192A impedance analyzer.

III. RESULTS AND DISCUSSION

Current–voltage (*I–V*) investigation was performed on several SnO/ε-Ga_2O_3 diodes fabricated on the same SnO/ε-Ga_2O_3 epilayer stack. *I–V* characteristics were acquired at RT on sets of two or three geometrically identical diodes for a statistical average, each set having the dimensions reported in Table I. Moreover, on the diode of the largest area, temperature dependent *I–V* characteristics were recorded in the range of 300–310 K. Figure 2 shows selected *I–V* data of the RT investigation, and the temperature dependences of the electrical data are shown in Fig. 3. Figures 2(a) and 3(a) confirm rectifying characteristics of the diodes. The related rectification ratio at ±1 V of $S_{1-V} = |I(+1\,V)/I(-1\,V)| = 100$, however, is small compared to that of previously demonstrated SnO/β-Ga_2O_3(−201) diodes ($S_{1-V} = 2 \times 10^8$).[31] The low S_{1-V} may in part be related to the visible, high reverse bias leakage current. We tentatively attribute this leakage current to the high donor concentration in the epsilon-Ga_2O_3 film (compared to 2×10^{17} cm^{-3} in Ref. 28) and consequently thin depletion region that allows reverse leakage $I(-1\,V)$ by tunneling.

In forward bias, the apparent linear *I–V* trend suggests a series resistance R_e to dominate over the expected Shockley-like diode behavior. The consequent current limitation is another contribution that decreases the $I(+1\,V)$ part of the rectification ratio—particularly in comparison to the vertical diodes of Ref. 28 with related low series resistance. The equivalent circuit for the present structure





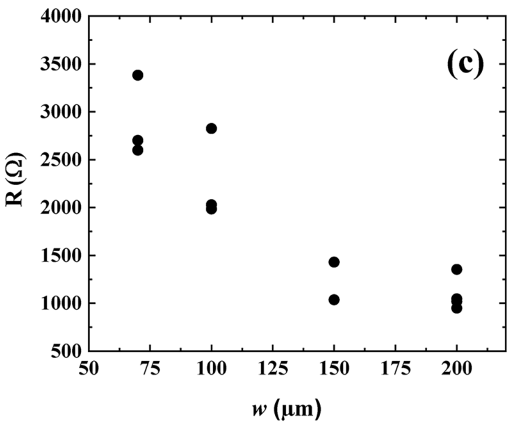


FIG. 2. (a) Selected RT current–voltage characteristics for diodes of different geometrical parameters (see Table I). (b) Same *I–V* data shown in (a) plotted in semilog scale to better evidence the leakage current. (c) Resistance data obtained from the linear fit of the forward *I–V* characteristics, plotted as a function of the linear dimension of the diode (*w* length, see Table I). For each *w* value, the resistance exhibited a certain scattering within the sets of diodes of equal geometrical dimensions.

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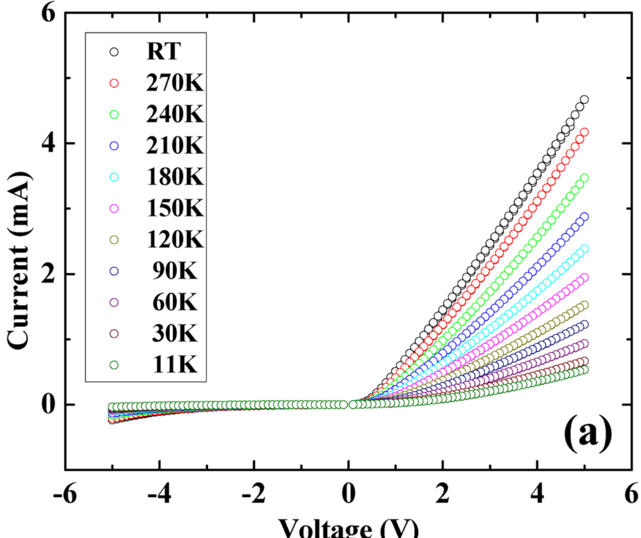

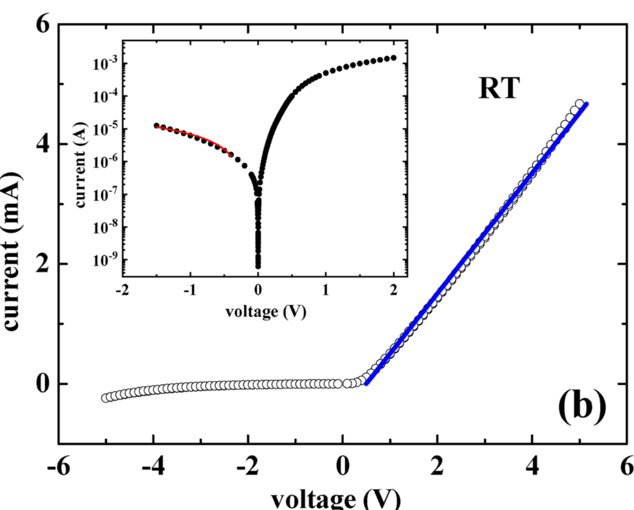

FIG. 3. (a) Current–voltage characteristics taken in the temperature range of 11–300 K. The uppermost I-V profile corresponds to RT; in sequence decreasing temperature up to 11 K (lowest profile). (b) Linear fit (blue line) of the RT *I–V* forward data (symbols), whose slope corresponds to a resistance of 996 Ω. Inset: current vs voltage at RT in a semilog scale: no linear trend is observed, typical of the ideal Shockley law. In the inset, the line provides a rough linear fit of the RT *I–V* reverse characteristic, corresponding to the slope $9 \times 10^{-6}\ \Omega^{-1}$ and a leakage resistance of about $1.1 \times 10^5\ \Omega$.

is shown in Fig. 1(c). R_e depends on the geometry of the diode and scales approximately inversely with the lateral dimension w of the p–n junction, as seen from Fig. 2(c), where the results of the linear fit of the I–V forward data are reported for several diode structures (the experimental slopes being interpreted as $1/R_e$). The averaged values of the resistance data of Fig. 2(c) are reported in Table I as R_e^{exp} for each lateral dimension w of the diodes.

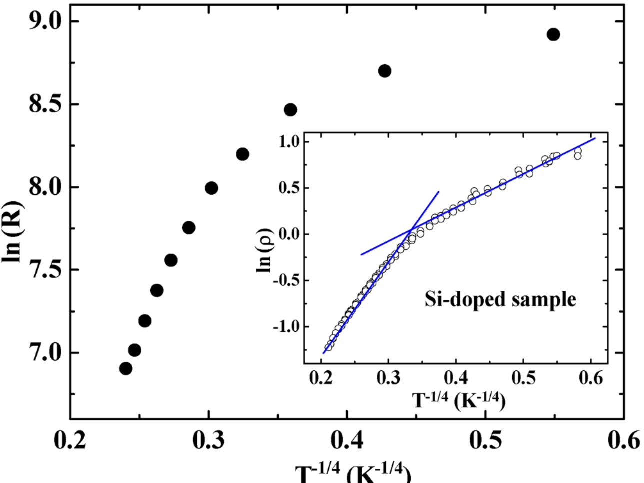

FIG. 4. Temperature dependence of the resistance R (in Ω) derived from the fit of the *I–V* data of Fig. 3(a), plotted in ln scale vs $T^{-1/4}$ (*Mott plot*): a linear trend in this plot indicates a VRH conduction mechanism, according to the Mott law (Ref. 23). Inset: temperature dependence of the resistivity (in Ω cm) in a Si-doped ε-Ga_2O_3 epitaxial layer similar to that used for fabrication of the investigated diodes (Ref. 24).

The temperature dependent I–V data were collected for a selected $200 \times 200\,\mu m^2$ diode structure. The results, reported in Fig. 3(a), show that a quite linear trend appears in the forward bias side of the I–V characteristics also at low temperatures: at RT, a resistance of 996 Ω was obtained from the linear fit of the I–V characteristics [see Fig. 3(b)]. By extending the same analysis to low temperature data, the temperature dependence of R_e is obtained, which is plotted in Fig. 4 in log scale versus $T^{-1/4}$ (*Mott plot*) to compare it with the typical two-slope linear trend of the in-plane resistivity observed in the *Mott plot* for ε-Ga_2O_3 Si-doped layers (the inset of Fig. 4). Such behavior is consistent with two distinct variable range hopping (VRH) mechanisms of transport, prevailing at low and high temperatures, respectively.[23,24] Despite the fact that the R_e data are not sufficiently dense to ascertain the linearity of the trends, especially at low temperatures, the similarity between the curves in the figure and in the inset suggests that the transport across the Ga_2O_3 channel is responsible for the resistance behavior of Fig. 4.

A rough estimation of such resistance can be given by conduction channels shown by the sketch of Fig. 1(d), of length d and section wt: current flows along four channels of this type, one for each side of the square diode resulting in a contribution $\rho d/4\ wt$. However, part of the current may also flow toward the corners of the square shaped gap around the SnO area and an additional contribution is expected by the in-plane current flowing below the depleted junction volume, which is difficult to estimate. The inverse proportionality relationship with the linear dimension of the p–n junction reported in Fig. 2(b) suggests for the effective R_e^{teo} resistance a correction by the introduction of a factor K, i.e.,

$$R_e^{teo} = k\rho d/(4\,wt). \tag{1}$$

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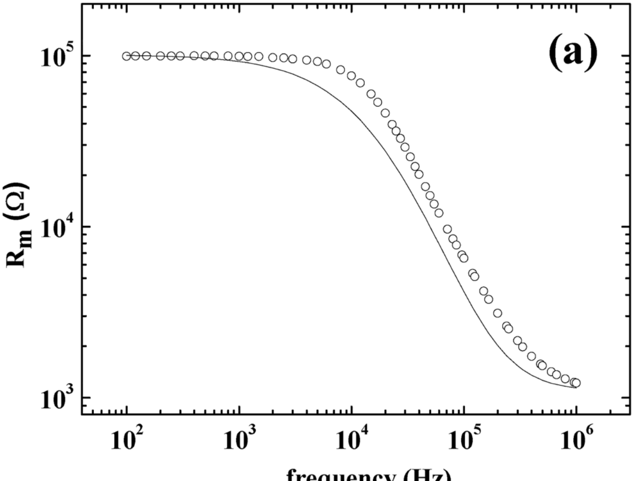
K factor can be obtained from the diode of the largest area by assuming the experimental value of R_e and the geometrical parameters of Table I. If the resistivity ρ is taken equal to the value $0.5\,\Omega\,\mathrm{cm}$, $\rho d/4\,wt = 139\,\Omega$ and then $K \approx 7.5$. A simulation of the real distribution of the in-plane current flux could enable the design of the optimal geometry to minimize the observed series resistance.

A test of the reliability of the equivalent circuit of Fig. 1(c) is given by a preliminary RT impedance spectroscopy investigation, whose results are shown in Fig. 5. The data were obtained at zero bias with an oscillation level of 5 mV. Here, the continuous lines correspond to a simulation of the real part, $Re(Z)$, and imaginary part, $Im(Z)$, of the impedance Z, defined for the equivalent circuit of Fig. 1(c). In this simulation, the values $R_e = 1100\,\Omega$, $R_d = 10^5\,\Omega$, and $C_d = 7.5 \times 10^{-11}$ F were inserted in the formulas

$$Re(Z) = R_m = \frac{R_e + R_d + R_e(\omega C_d R_d)^2}{1 + (\omega C_d R_d)^2} = R_e + \frac{R_d}{1 + (\omega C_d R_d)^2},$$
$$Im(Z) = \frac{1}{\omega C_m} = \frac{\omega C_d R_d^2}{1 + (\omega C_d R_d)^2}, \tag{2}$$

where R_m and C_m represent the measured values of resistance and capacitance in a series-circuit configuration. As the dissipation factor (D-factor) resulted in lower unity only above 10 KHz,[34] the evaluation of R_e, R_d, and C_d parameters from the best fit of the data of Fig. 5 over the whole frequency range is to be considered unreliable. To confirm the validity of the equivalent circuit of Fig. 1(c), we adopted the following procedure: the leakage resistance R_d was selected consistent with the slope of the approximately linear fit of the reverse I–V in Fig. 3(b) (inset: line accompanying the data for reverse bias). The capacitance value C_m, taken at high frequency (where D-factor is lower than unity), is expected to tend to the depletion capacitance C_d. With these choices, the value required for R_e to fit the experimental data well approaches the value obtained from the fit of the forward I–V data, which makes the procedure self-consistent.

An attempt to decouple the R_e contribution from the junction one can then be performed by subtracting from each experimental voltage value the product IR_e, where I is the experimental current. In this operation, the R_e value was iteratively increased until a linear trend of the log(I)-versus-voltage characteristics was obtained. Such a condition was reached when taking the value $R_e = 950\,\Omega$. At this point, one can tentatively derive the "real" I–V



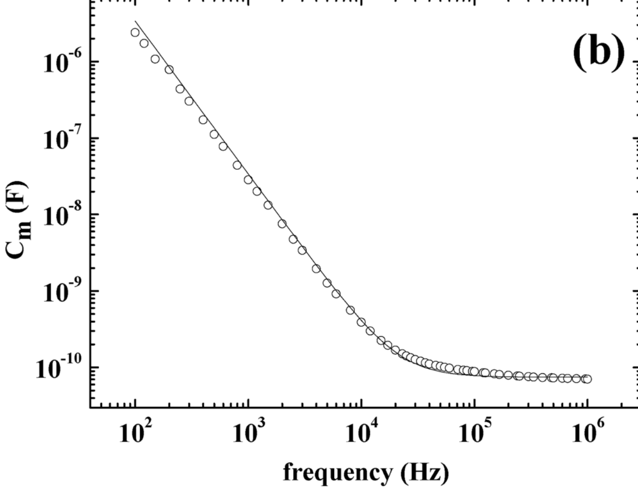


FIG. 5. Frequency dependence of experimental resistance (a) and capacitance (b) obtained by impedance spectroscopy at RT, considering a series-circuit measurement configuration.

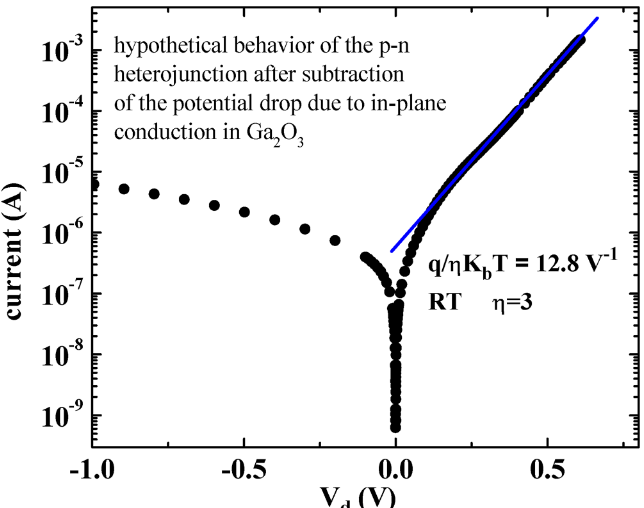


FIG. 6. Current–voltage characteristics of the diode, where $V_d = V - IR_e$, with V and/the experimental values of voltage and current, and R_e derived following the iterative procedure described in the text. K_b is the Boltzmann constant, q the electron charge, and η the ideality factor of the diode.

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characteristics of the diode, as shown in Fig. 6. An ideality factor of about 3 is obtained after such correction, as for a tunneling transport mechanism across the junction. With respect to the SnO/β-Ga_2O_3 heterojunction of Ref. 31, the diode on ε-Ga_2O_3 seems to be less performing. However, the present results are encouraging concerning the possibility to fabricate *p*–*n* junctions based on ε-Ga_2O_3.

IV. SUMMARY AND CONCLUSIONS

SnO/ε-Ga_2O_3 *p*–*n* diodes with planar geometry and different dimensions were investigated, focusing the analysis on the temperature dependence of the current–voltage characteristics. A significant series resistance due to the in-plane conduction through the Si-doped ε-Ga_2O_3 layer up to the corresponding ohmic contact was observed. The similarity between the temperature dependences of the diode series resistance and the ε-Ga_2O_3 resistivity corroborates the idea of a dominant effect of series resistance on the junction performance. The behavior of $\ln(\rho)$ versus $T^{-1/4}$ is linear with two well identified slopes. The linearity of this plot versus $T^{-1/4}$ indicates a transport via variable range hopping, possibly connected with the columnar domain structure of the ε-Ga_2O_3 polymorph.

A simple equivalent circuit is presented to describe the experimental behavior of the SnO/ε-Ga_2O_3 *p*–*n* junction. The derived series resistivity values are supported by preliminary impedance spectroscopy investigation.

Increasing the in-plane conductivity of the layer by preventing or limiting the domain formation is a way for improving the performance of diodes with planar geometry. Also, the optimization of the diode geometry can help to minimize the observed series resistance, however, keeping in mind that capacitance also depends on diode geometry and must, therefore, be simultaneously optimized.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] J. Zhang, J. Shi, D.-C. Qi, L. Chen, and K. H. L. Zhang, APL Mater. **8**, 020906 (2020).
[2] J. Y. Tsao *et al.*, Adv. Electron. Mater. **4**, 1600501 (2018).
[3] H. von Wenckstern, Adv. Electron. Mater. **3**, 1600350 (2017).
[4] M. Higashiwaki and S. Fujita, *Gallium Oxide: Materials Properties; Crystal Growth; and Devices*, Springer Series in Materials Science Book 293 (Springer Nature, Switzerland, 2020).
[5] S. Pearton, F. Ren, and M. Mastro, *Gallium Oxide-Technology: Technology; Devices and Applications*, Metal Oxides Series—Series Editor Ghenadii Korotcenkov (Elsevier, Amsterdam, The Netherlands, 2019).
[6] S. J. Pearton, J. Yang, P. H. Cary, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, Appl. Phys. Rev. **5**, 011301 (2018).
[7] M. Bosi, P. Mazzolini, L. Seravalli, and R. Fornari, J. Mater. Chem. C **8**, 10975 (2020).
[8] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, J. Appl. Phys. **110**, 063720 (2011).
[9] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Appl. Phys. Lett. **106**, 032105 (2015).
[10] T. Onuma, S. Fujioka, T. Yamaguchi, M. Higashiwaki, K. Sasaki, T. Masui, and T. Honda, Appl. Phys. Lett. **103**, 041910 (2013).
[11] J. B. Varley, A. Janotti, C. Franchini, and C. G. Van de Walle, Phys. Rev. B **85**, 081109 (2012).
[12] J. L. Lyons, Semicond. Sci. Technol. **33**, 05LT02 (2018).
[13] A. J. Green *et al.*, APL Mater. **10**, 029201 (2022).
[14] Z. Guo *et al.*, Appl. Phys. Lett. **106**, 111909 (2015).
[15] P. Mazzolini, A. Falkenstein, C. Wouters, R. Schewski, T. Markurt, Z. Galazka, M. Martin, M. Albrecht, and O. Bierwagen, APL Mater. **8**, 011107 (2020).
[16] A. Fiedler, R. Schewski, M. Baldini, Z. Galazka, G. Wagner, M. Albrecht, and K. Irmscher, J. Appl. Phys. **122**, 165701 (2017).
[17] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, Appl. Phys. Lett. **100**, 013504 (2012).
[18] R. Schewski *et al.*, APL Mater. **7**, 022515 (2019).
[19] R. Fornari *et al.*, Acta Mater. **140**, 411 (2017).
[20] I. Cora, F. Mezzadri, F. Boschi, M. Bosi, M. Čaplovičová, G. Calestani, I. Dódony, B. Pécz, and R. Fornari, CrystEngComm **19**, 1509 (2017).
[21] M. Kneiß, D. Splith, P. Schlupp, A. Hassa, H. von Wenckstern, M. Lorenz, and M. Grundmann, J. Appl. Phys. **130**, 084502 (2021).
[22] H. Nishinaka, O. Ueda, D. Tahara, Y. Ito, N. Ikenaga, N. Hasuike, and M. Yoshimoto, ACS Omega **5**, 29585 (2020).
[23] A. Parisini, A. Bosio, V. Montedoro, A. Gorreri, A. Lamperti, M. Bosi, G. Garulli, S. Vantaggio, and R. Fornari, APL Mater. **7**, 031114 (2019).
[24] A. Parisini, A. Bosio, H. J. von Bardeleben, J. Jimenez, S. Dadgostar, M. Pavesi, A. Baraldi, S. Vantaggio, and R. Fornari, Mater. Sci. Semicond. Process. **138**, 106307 (2022).
[25] H. W. Xue, Q. M. He, G. Z. Jian, S. B. Long, T. Pang, and M. Liu, Nanoscale Res. Lett. **13**, 290 (2018).
[26] H. Zhou *et al.*, IEEE Electron Device Lett. **40**, 1788 (2019).
[27] Y. Wang *et al.*, IEEE Electron Device Lett. **41**, 131 (2020).
[28] H. Qian *et al.*, Vacuum **200**, 111019 (2022).
[29] S. Li *et al.*, Sci. China Technol. Sci. **65**, 704 (2022).
[30] J. Dai, S. Li, Z. Liu, Z. Yan, Y. Zhi, Z. Wu, P. Li, and W. Tang, J. Phys. D: Appl. Phys. **54**, 215104 (2021).
[31] M. Budde, D. Splith, P. Mazzolini, A. Tahraoui, J. Feldl, M. Ramsteiner, H. von Wenckstern, M. Grundmann, and O. Bierwagen, Appl. Phys. Lett. **117**, 252106 (2020).
[32] See the supplementary material at https://www.scitation.org/doi/suppl/10.1116/6.0001857 for structural information on the SnO(001)/ϵ-Ga_2O_3 heterostructure on the *c*-Al_2O_3 substrate.
[33] M. Budde *et al.*, Phys. Rev. Mater. **4**, 124602 (2020).
[34] O. Bierwagen, T. Nagata, T. Ive, C. G. Van de Walle, and J. S. Speck, Appl. Phys. Lett. **94**, 152110 (2009).

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