Power GaN FET boards thermal and electromagnetic optimization by FE modeling

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P. Cova*, N. Delmonte, D. Santoro

Department of Engineering and Architecture, University of Parma
Parco Area delle Scienze 181/a, 43124, Parma, Italy

Abstract

This work deals with optimization of boards with commercial discrete power GaN FETs in applications where natural air convection is a strict constraint. In these cases, both thermal and electromagnetic behaviours are critical reliability issues for the board design, and they are modeled by Finite Element (FE) analysis, starting from literature description of the device structure, and measurements on a simple test circuit.

For improved accuracy and more realistic modeling, verification and validation simulation steps are introduced, in order to evaluate the relevant error parameters for different FEM solutions.

The results obtained demonstrate a good fitting with experimental and make it possible to improve board thermal characteristic. The electromagnetic simulations allow the evaluation, and possibly the reduction, of parasitic inductances for different layouts.

Then, the proposed approach enables thermal and electromagnetic optimization of the layout design by simple FEM simulations, without any preliminary prototype, with time and cost saving.

1. Introduction

To exploit the excellent thermal and frequency performance of discrete GaN FETs, an accurate design of packaging and board layout is necessary. Both these aspects are related to reliability: higher temperatures reduce the device lifetime; parasitic inductances can lead to overvoltages and spurious gate signals, dangerous for the device.

The accuracy of the physical modeling in power electronic devices, especially GaN based, becomes more and more important due to the complexity and thermal characteristics of commercially available devices [1]–[4]. Due to their unique electrical and thermal capabilities/characteristics compared to Si counterparts, these devices are quite attractive, enabling a considerable reduction of the size of passive components and improvement of the efficiency [5]–[7]. Unfortunately, the increase of power density requires more efforts during thermal management design. Many times, the thermal resistances given by manufacturers are not enough to well design a circuit from the thermal point of view. Furthermore, the lack of information about the structure of the device does not allow to set accurate models useful for a careful design. For this reason, the typical workaround is to oversize thermal components, wasting materials and space. This work aims at reducing the oversizing design of the heat spreading solutions by means of a high accurate physical model. As an emerging technology, power GaN controlled switches only recently became available on the market. Thermal and electromagnetic design are important issues for the newest devices, due to higher frequencies and power densities [4]. This paper addresses small low power DC/DC converters, to be used without fans or liquid based heat sinks (e.g. for portable applications, or converters in close environments such as standard electrical boxes, outlets and sockets for distribution networks in buildings).

Unfortunately, closed cases and boxes without forced air or liquid cooling, are characterized by low heat transfer coefficients, therefore the task to find the best solution for a reliable operative nominal condition is not easy. The near chip scale package of the devices allows a vertical thermal flow. From the low voltage commercial available GaN devices [5], the GaN Systems GS61004B, with promising electrical and thermal features, has been taken in to account for a deep thermal analysis. The GaN_{PX} package of GaN System has been designed for an improved thermal performance with the lowest possible inductance, as partially shown in [8]. If compared to similar devices of other competitors (e.g. EPC's eGaN FETs), there is a lack in electro-thermal models available in literature. One of the goals of this work is to fill this lack. The EPC's FETs have been studied more thoroughly. For example, a thermal evaluation of the EPC2021 has been done in [4] and an Electro-Thermal Model of EPC2010 GaN FET has been evaluated in [3].

The layout optimization is not an easy task, since increasing the area of copper pads and traces improve heat removing, but also can increase parasitic inductances, and then, some preliminary prototypes are often needed to reach the target.

In this work, for an easier design of thermal cooling structures, a finite element method approach has been adopted for the heat transfer problem together with electromagnetic modelling of the whole device-package-board assembly. This, regarding the transistor taken as reference, can be considered the main novelty of this work with respect to the state of the art.

* Corresponding author. paolo.cova@unipr.it
Tel: +39 0521 905818; Fax: +39 0521 905822

2. Applied method

Here we describe the steps that have been taken in this work following a well-known method, where the finite element modeling is validated by means of measurements performed on a device or circuit used as benchmark.

In Fig. 1 the workflow of the modeling and finite element analysis is shown. The method allows to highlight the improvements which can be obtained from the board layout changes. Once chosen the power device to use as controlled switch in a power converter, it is possible to search all the information needed for the model (geometries and materials physical properties) with direct inspections, literature review, and state of the art analysis. In parallel, a simple circuit to use as reference can be designed and produced. The experimental tests made with this reference circuit can be used to search for the values of unknown, or not well known, parameters needed in the finite element model of this circuit (following the procedure illustrated in [9]. When the model is set, it can be verified (e.g. changing the mesh) and validated comparing the simulation results with measurements. Once the model has been validated, different solutions of the same circuit can be simulated and compared to find the optimum.

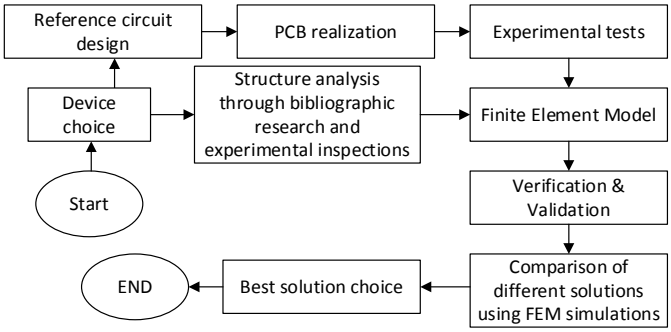

Fig. 1. Workflow of the modeling and finite element analysis to optimize a thermal design.

Here this method has been applied to the thermal design of a switching converter with power GaN transistor.

Another analysis, which can be done with this method, is the electromagnetic one, to estimate some electrical parasitic elements of the PCB. In this work, a preliminary electromagnetic modelling is presented, just to show the interference between the thermal solutions and the electrical ones in a PCB design.

3. Device analysis

As stated above, the device used in this work is the GS61004B (Fig. 2) produced by GaN Systems. Due to the innovative package and previous experiences with GaN based package-free transistors [10], the choice has been taken for an accurate thermal characterization of a 100 V transistor, considering a future development of a low power DC/DC converter in closed environments, without fan or liquid cooling. In particular, the model is the smallest and less current holder of the commercial range, with a maximum of 45 A.

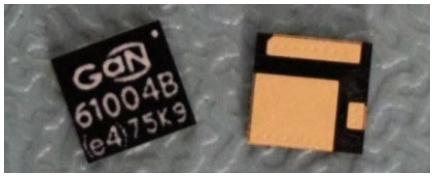

Fig. 2. Photo with two GaN Systems' GS61004B: top view (left); bottom view (right).

To set an accurate physical model of the transistor, a bibliographic research was conducted. A presentation of the Embedded Packaging GaN$_{PX}$ of GaN Systems' products [8] shows a cross-section and an exploded view of the GS61006P transistor, brother of the one chosen, with the same layers stack, and a larger area for a greater maximum current rate. In order to assure the as much as possible higher accuracy of the model, an inspection of the device was carried out, lapping it from the top layer by layer, to obtain multiple planar views.

The structure of the GaN based transistor (Fig. 3) does not have specifically inserted parts for thermal dissipation; the most important thermal flow goes toward the source and drain connection pads. For this reason, the layout of the board has a fundamental role to maximize the heat flow and minimize the temperature gradient for a more reliable assembly.

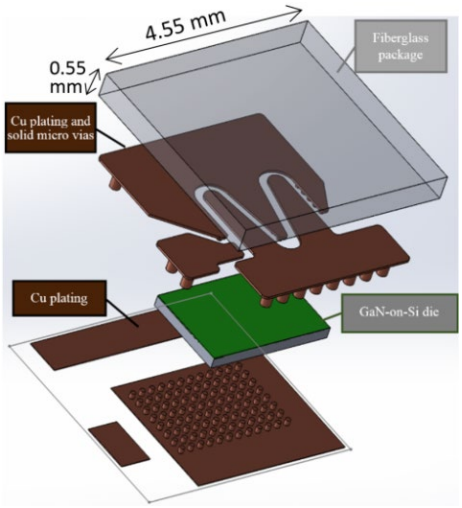

Fig. 3 - 3D geometry of the GaN$_{PX}$ package structure: a) perspective view with transparent package; b) exploded view.

4. Experimental setup

As a fundamental step of the applied method, a reference circuit has to be designed and a PCB must be produced for experimental tests. For a laboratory implementation, it is better to design the simplest possible circuit to reduce problems due to manual assembly (e.g. soldering variations). This is advantageous also for the model fitting and for the accuracy of measurements.

Fig. 4 shows the schematic diagram of the test bench made. Here a DC biasing of the FET has been chosen, because it is easier to set, with a few basic components, and needs a simpler layout than a solution with a PWM control. On the

power loop, a 10 Ω power resistor has been inserted as load, and used for drain current and V_{DS} measurements. To evaluate gate current and V_{GS}, another voltmeter has been used, which measures the voltage across the gate resistor. For the infrared thermography two different cameras has been used: a Flir One Pro for Android for fast captures, and a Flir A325 for a continuous monitoring.

The PCB layout has been drawn without taking care of the heat spreading but considering the simplest possible structure, in order to more accurately replicate it with CAD programs. In Fig. 5 the fabricated PCB is shown.

Different electrical conditions have been tested and recorded at the stationary condition, once a stable temperature on the top device surface was reached. The one used for the 3D FE model fitting had a 7.73 V gate to source voltage, a 10 mA current on the gate resistor, whereas the drain to source voltage and the drain current were 4.17 V and 0.45 A, respectively. Therefore, a gate and drain power dissipation of 23 mW and 0.868 W, respectively, can be considered (total dissipated power P_D = 0.891 W). With this electrical condition and a room temperature of 23.4 °C, a surface device temperature of 101.5 °C has been measured, as shown in Fig. 6. For a greater accuracy and a uniform emission coefficient, the board has been matt painted and the FLIR thermal imager has been positioned at a distance of around 30 cm from the circuit. In Fig. 7, the test bench is shown during a test, with the two voltmeters: Fluke 83 and Protek 506, and two different DC power suppliers: an Agilent E3647A for the gate voltage and a Hewlett Packard 6684A for the drain-source biasing. To avoid large variations of the power resistor resistance, it was mounted on a large heatsink.

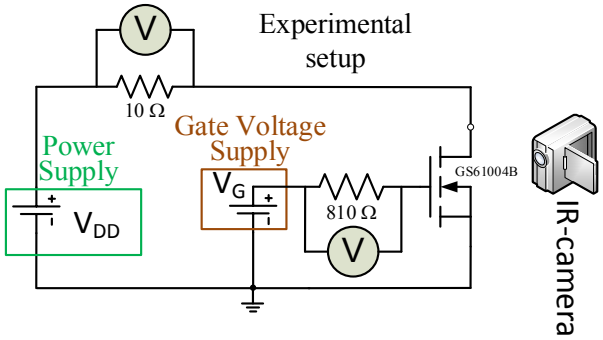

Fig. 4. Schematic diagram of the test bench with reference circuit.

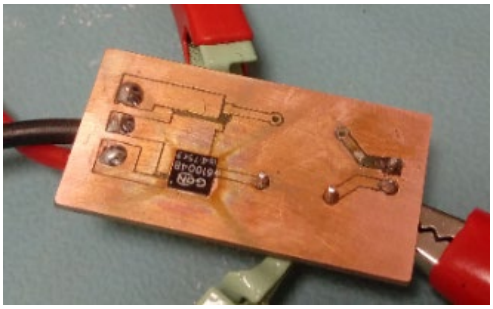

Fig. 5. The reference PCB. It was covered with an optically transparent matt paint with a known emission coefficient (ε = 0.96).

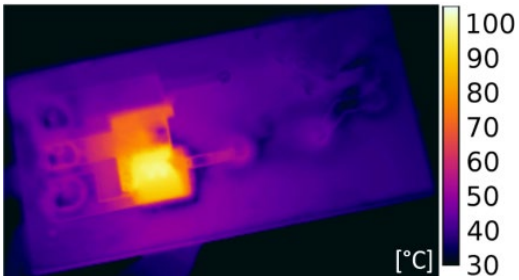

Fig. 6. IR photo of the reference circuit under test at steady state with P_D = 0.891 W at T_{amb} = 23.4 °C.

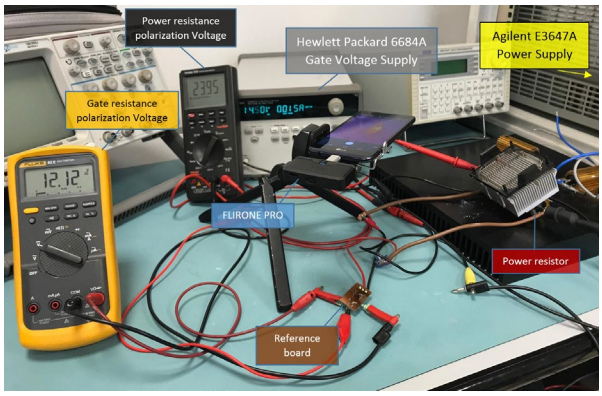

Fig. 7 - Experimental setup.

5. FE Modeling

In this Section, the models set for thermal optimization are described together with the ones set for the electromagnetic analysis to evaluate the parasitics parameters of the copper tracks drawn. In this case the adopted models has been considered validated by previous works [11], [12]. Through COMSOL Multiphysics, simply geometries can be modified and for electromagnetic simulation a structure defeaturing can be obtained.

A. Thermal modeling

The proposed finite element model considers the whole 3D domain of the reference PCB for a detailed thermal distribution, because it does not have any kind of symmetry. The geometries of the device and the board has been drawn with the best possible accuracy, only approximating the epitaxial layers of Gallium Nitride that have been considered as a unique layer of GaN. Using COMSOL Multiphysics 5.3, finite element simulations with the *Heat Transfer in Solids* study, the heat source has been defined with a rate of 0.891 W uniformly generated in the volume of the GaN layer. Regarding the boundary conditions, considering negligible the heat flows of the board edges, they have been set as adiabatic walls, while at the bottom and top surfaces two different heat fluxes due to convection have been set. Physical properties as heat capacity at constant pressure and material density of copper, solder, FR4, Silicon and GaN have been set by the library of COMSOL, except for the thermal conductivities of the GaN and the Si layers set as the following temperature dependent equations [13] [14]:

$$k_{GaN} = 160 \cdot \left(\frac{300}{T}\right)^{1.4} \quad k_{Si} = 148 \cdot \left(\frac{300}{T}\right)^{1.65} \quad \left[\frac{W}{m \cdot K}\right]$$

A physics-controlled extra fine mesh (the highest density automatic unstructured meshing in COMSOL) has been used, then compared with other meshing densities for verification and validation steps. By the use of this high meshing densities, almost 3 million degree of freedom were achieved, resulting in the use of 3 GB virtual memory and almost 2.5 GB of physical memory. Differently, normal to fine meshes use about 200 thousand degree of freedom, much more easy and faster to be simulated. By the use of a dual Intel Xeon E5-2600 v4 processor and 125 GB RAM computer, the simulation times range from about 2 to 5 minutes.

At the bottom surfaces of the board, a low convection rate can be set. In this case the heat transfer coefficient has been set as h_{bottom} = 4 W/m^2·K, while the heat flux on the top of the board has been used as the fitting parameter.

With the COMSOL natural air convection coefficient equation [15] for top horizontal surfaces, h_{top} has been computed as shown in Fig. 8. Unfortunately, the natural air convection during the tests cannot be controlled to be equal to the one evaluated by COMSOL using the equation in [13], and this has resulted in outdistanced simulated and measured temperatures. As usually, with a real natural air convection, h_{top} is unknown, and it can be used as fitting parameter. Therefore, simulations have been carried out searching for the value of h_{top} which gives the best approximation with respect to the measured temperatures.

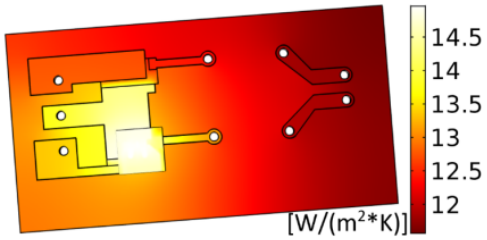

Fig. 8. Heat transfer coefficient evaluated at the top surfaces of the reference board by COMSOL for a simulation with natural air convection with P_D = 0.891 W at T_{amb} = 23.4 °C.

B. *Electromagnetic modeling*

Another FE model has been set for the evaluation of the board's parasitic elements. In this work, just a preliminary electromagnetic model has been simulated, only to compare two different layouts taken as an example. The first layout were used for FE model fitting with measurements. Then, a second layout was designed with larger tracks to relax thermal dissipation, with the same 35 µm TOP layer copper thickness and 1.5 mm FR4/Aluminum PCB substrate.

The two layouts were simplified with a geometry defeaturing for a coil analysis of the power loop. Fig. 9 shows the geometries used for these FE models. The FET has been replaced by a short copper track between the drain and the source pads.

A *Magnetic Field* study of COMSOL has been used for a frequency analysis on a 250 kHz – 10 MHz range, with 1 µV voltage stimulus. Relative permeability, electrical conductivity and relative permittivity have been set by the COMSOL's library. A sphere has been drawn to define the magnetic field exhaustion which becomes infinitesimal within a finite space as done in [16].

Electromagnetic simulations haven't been simulated with the highest meshing densities. Though, almost 1.5 million degree of freedom were achieved, resulting in the use of 3.5 GB virtual memory and almost 3 GB of physical memory, which were simulated in almost 6 minutes.

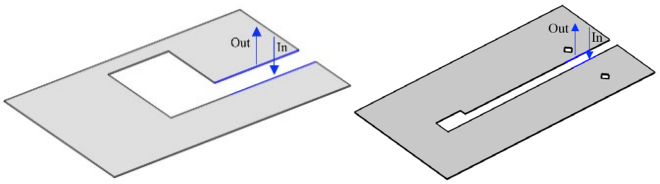

Fig. 9. 3D geometries of the copper tracks analyzed: reference board (left); board with thermal improvement (right). The two small surfaces of the terminals where the current has been simulated to enter and exit are highlighted in blue.

6. Results

An important step of the method here applied is the analysis of results for the model validation. At the end, the comparison of models of different solutions has to be done carefully considering the limitations of FEM adopted.

C. *Thermal analysis*

The thermal simulation results of the reference board have been compared to the experimental measurements by tuning the fitting parameter here chosen (convection coefficient on the top surfaces of the reference board). From experimental, a maximum temperature of 101.5 °C were expected on the device surface, as shown in Fig. 6.

With an extremely fine mesh, h = 34 W/m^2·K, T_{amb}=23.4 °C, and P_D = 0.891 W, it has been obtained the simulated thermal map in Fig. 10, having a good matching with the one obtained by infrared measurements of Fig. 6 at the same operating conditions.

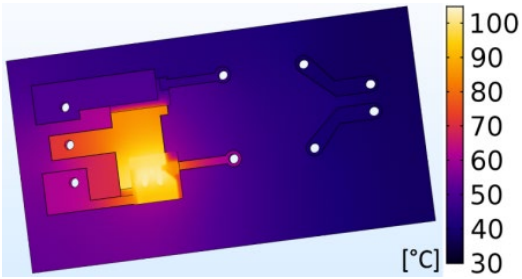

Fig. 10. Simulated thermal map with extremely fine mesh, h = 34 W/m^2·K, T_{amb} = 23.4 °C, and P_D = 0.891 W.

The physical properties of the materials are known with high accuracy, thus the physics-controlled meshing and the refining applied by the FE simulator played an important role during the verification step. For this reason, the temperatures

of 5 points on the device top surface, as shown in Fig. 11, have been taken into account to verify how the size of the mesh elements affects the simulation results. Fig. 12 shows the measured and simulated temperature variations versus the mesh sizing applied by COMSOL with different default densities. As it can be expected in FE simulations, the results are limited by the meshing degree in the multi-scale model. Thus, the standard FE method of conforming meshes can be improved for example by homogenization concepts, as well as nonmatching grid techniques, as shown in [17].

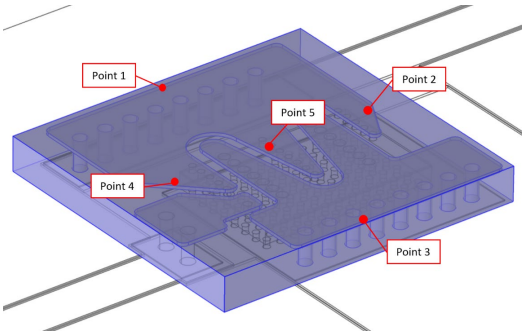

Fig. 11. Points of interest for the fitting and the validation of the FE thermal model of the GaN FET. All the five points are on the top surface of the package.

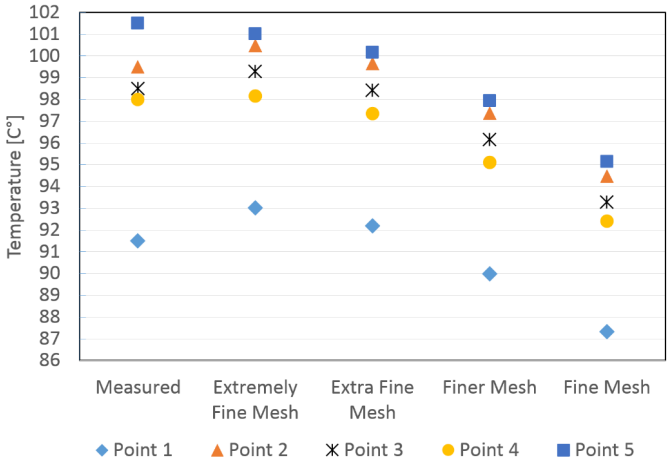

Fig. 12. Measured and simulated temperatures in 5 points of interest of the reference board with h_{top} = 34 W/m^2·K, T_{amb} = 23.4 °C, and P_D = 0.891 W.

In this work the PCB has been made by a CNC milling machine. Therefore, the first step to fabricate the PCB is the isolation of the copper traces using one or two mill tools with different diameters. After the isolation, another optional step is the rub-out of the exceeding copper. Depending on the width of the isolation the exceeding copper, which will be electrically floating, can be useful or not for the heat spreading. Here the isolation has been made using a milling tool with a 0.2 mm diameter, thus the isolation is quite smaller than the thickness of the FR4 substrate (1.6 mm). Then the heat can flow more easily toward the closest floating copper, than to the bottom surface of the FR4 layer. In other words, the lateral heat spreading is enhanced by the floating copper, if compared to that in a rubbed-out PCB.

By applying a board rub-out, the heat tends to flow towards the air mainly through the electrical tracks. This results as a thermal resistance between the FET's case and the ambient greater than the same one without the rub-out. Therefore, with the same dissipated power and the same ambient temperature, the steady state junction temperature will be greater with the rub-out, as confirmed by the simulation (Fig. 13). Compared with the adopted solution, an increase of almost 50 °C is obtained.

Starting from the reference board, possible improvements have been simulated. To maximize the power dissipation, a second version of the board with larger drain and source pads has been designed (Fig. 14).

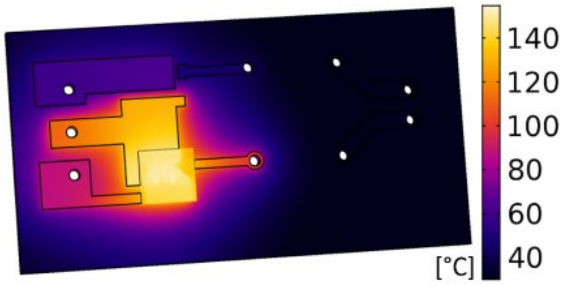

Fig. 13. Simulated thermal map of the rubbed-out reference board at the same conditions of Fig. 10.

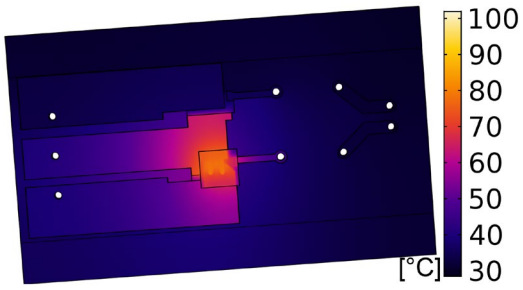

Fig. 14. Simulated temperatures of the second version board operating at the same conditions of Fig. 10.

A further solution to improve the thermal management has been simulated considering an Insulated Metal Substrate (IMS) instead the FR4. In Table 1, all the thermal simulation results are reported. To provide a comparison between a two-layer and four-layer layout, the second board has been simulated also adding two interleaved 35 µm copper layers, with an appreciable thermal improvement. As can be seen the best solution is the one with the metal substrate (1.5 mm thick aluminum), where the maximum temperature drops by 50 % or more.

As already mentioned, in this work the concern is on the applications with low power DC/DC converters in close environments as standard electrical boxes, outlets and sockets. Thus, some other models with the two versions of boards here presented have been set considering them operating in the worst condition of a still-air environment of a 7 x 6 x 3 cm^3 box mounted in a thermally isolated wall with a room temperature of 40 °C (Fig. 15).

Table 1
Simulated maximum temperatures for different solutions with T_{amb} = 23.4 °C, and P_D = 0.891 W/FET.

	Natural air convection		Forced air convection	
	without rub-out	with rub-out	without rub-out	with rub-out
reference board	101.5 °C	150.9 °C	76.4 °C	97.7 °C
reference board (2 GaN FETs)	139.8 °C	202.6 °C	92.5 °C	117.9 °C
reference board (IMS)	53.6 °C	54.4 °C	-	-
v.2 board	101.5 °C	116.7 °C	78.2 °C	97.4 °C
v.2 board with a 4 layers layout	72.3 °C	77.6 °C	57.6 °C	61.7 °C
v.2 board with 2 GaN FETs	102.1 °C	125.2 °C	72.7 °C	83.1 °C
v.2 board (IMS)	39.1 °C	43.7 °C	-	-

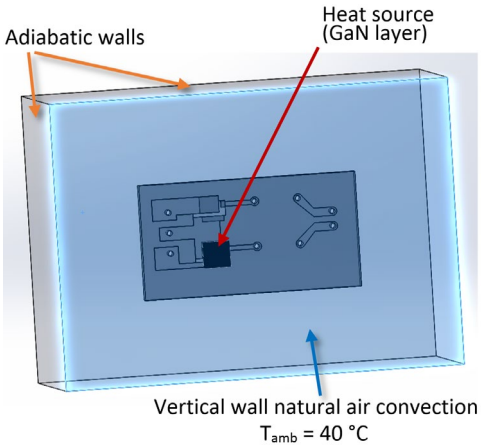

Fig. 15. 3D geometry of a board in a wall electrical box, with boundary conditions and the heat source.

In these cases, a dissipated power of around 0.9 W gives maximum temperatures well above the datasheet maximum operating junction temperature of 150 °C. Then, considering solutions with IMS, lowering P_D to 0.35 W, the maximum simulated temperatures resulted 124.5 °C and 99.5 °C, for the reference board and the second version layouts, respectively.

D. Electromagnetic analysis

Fig. 16 and Fig. 17 show the current density simulated with different frequencies in the reference and the second version boards, respectively. It can be easily noticed that the skin effect becomes more evident by increasing the frequency. The current distribution changes, therefore the resistance increases and inductance decreases, because of the different produced magnetic field.

The results obtained by the *Magnetic Field* study of COMSOL Multiphysics (stray inductance and resistance of the power loop copper tracks) can be related to the thermal behavior. In Table 2, the electromagnetic simulation results are reported. As it can be noticed, the worst cases of parasitics are recorded for the second version board. As expected:

- in both cases the resistance values increase due the skin effect, while the inductance decreases with the frequency increasing;
- parasitics of the second layout, with a wider and longer copper area, have a greater dependence to the frequency.

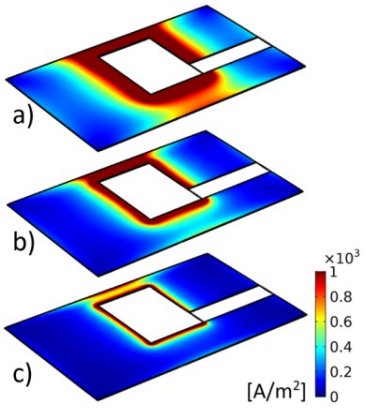

Fig. 16. Frequency domain simulated current density in the power loop tracks of the reference board with a 1 µV voltage stimulus and different frequencies: a) 250 kHz; b) 500 kHz; c) 1 MHz.

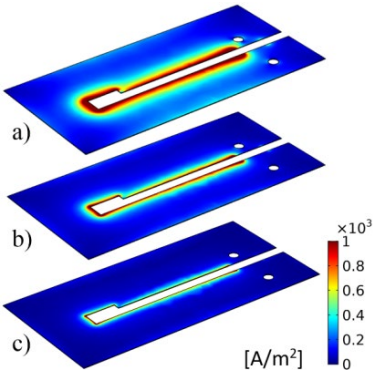

Fig. 17. Frequency domain simulated current density in the power loop tracks of the v.2 board with a 1 µV voltage stimulus and different frequencies: a) 250 kHz; b) 500 kHz; c) 1 MHz.

Table 2
Simulated parasitics values.

	Inductance [nH]			Resistance [mΩ]		
	250 kHz	500 kHz	1 MHz	250 kHz	500 kHz	1 MHz
Ref. board	7.01	6.83	6.67	5.07	5.58	6.34
v.2 board	10.93	10.31	9.87	6.35	7.77	9.64

7. Conclusions

The analysis shown can be extended to time dependent studies, which includes the thermal capacitance to complete the thermal study for this kind of circuits with GaN devices. It is worth to be noticed that, once developed the thermal model of a PCB or a power module, using COMSOL Multiphysics or other similar CADs, it can be easily coupled with a structural mechanic study, for reliability numerical analysis. Considering the GaN devices here presented, which have relatively new inner structures and unconventional pins or pads, the mechanical aspects has not yet well studied and presented in literature.

The method shown in Fig. 1, which results in accurate models, makes evident that it is useful for a comparison of different solutions and to optimize the thermal design,

verifying as well as the electromagnetic behavior. Here the cumbersome optimization step has not been presented, to focus on the modeling steps (setup, verification & validation, application). As a short example of work to do for the optimization, some different solutions have been compared. It is worth to note that the optimal solution depends on the thermal and frequency requirements, then the designer will use this approach finding the best trade-off between the two performance in its specific application.

The only drawback of the applied method is the time needed to design and build a prototype, and to setup ad-hoc test benches for a good verification and validation of the modeling, but, once done this, the presented approach allows the thermal and electromagnetic optimization of the layout design by simple FEM simulations, with time and cost saving.

We applied the method to analyze a GaN power device recently available on the market, not yet deeply studied from the thermal point of view. We focused on the thermal problem for applications where the heat spreading can take place in not favorable conditions, for which the method become very useful and accurate. The simulations of power circuits with the GaN transistor chosen in worst conditions, have shown that the thermal management cannot be simple with output power rates of several dozens of Watts, because the temperature becomes higher than the datasheet maximum operating junction temperature.

The transistor chosen does not have a flange for heat sink, therefore the heat flows mainly through the bottom electric contacts, and this forces to draw large pads and/or copper traces. The electromagnetic analysis on a solution proposed to improve the heat spreading, has shown that a trade-off between thermal and electrical performances is necessary, and that the low stray inductance of the device is easily canceled by the greater inductance due to larger copper traces.

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