Comprehensive control system for parallelable 60Hz-2MVA harbor AC/AC converters

Comprehensive Control System for Parallelable 60Hz-2MVA Harbor AC/AC Converters

Paolo Cova, Andrea Toscani, Carlo Concari, *Member, IEEE*, Giovanni Franceschini, Marco Portesine

***Abstract* – A high performance parallelable 2 MVA, 50/60 Hz AC/AC frequency converter for harbor applications was designed and built. A specific comprehensive digital control system was set up, in order to obtain optimal current sharing among two or more parallel power converters. The control, based on a master-slave strategy, also guarantees good system availability in case of faults, even when the master is affected, by switching off the faulty converter and assuring continuous system operation under power derating.**

The control system was designed using MATLAB/ Simulink/PLECS tools, and tested with reduced-scale prototypes. After fine tuning a good agreement between prototype measurements and simulations was obtained. The full-size system, composed of two 2 MVA converters, was then fabricated and tested, demonstrating performances compliant with the requirements and aligned with simulations and measurements performed on the prototypes.

***Index Terms* -- Frequency conversion, AC/AC, DSP, feed forward, static power conversion, paralleled converters, PWM synchronization, redundancy, current sharing.**

I. INTRODUCTION

Frequency conversion is required in many high power applications [1]. For years, solid-state converters have been replacing electromechanical systems in applications ranging from wind power generation [2] to line frequency conversion [3], [4].

This work addresses a frequency converter for harbor applications, able to supply large ships during their docking time. Such application has strict requirements regarding voltage regulation, total harmonic distortion (THD), dynamic behavior and capability of driving unbalanced loads, together with high reliability and maintainability. A further requirement is the modularity: two or more converters (identical in hardware and software) must be able to operate in parallel, automatically share output current and disconnect malfunctioning ones.

Many papers address the parallel operation of power converters [5]-[17]. Modularity allows for enhanced reliability and easy addition of power capacity when needed; interleaved paralleled converters are able to reduce the output current ripple [5]. One of the most widespread solutions for modular parallel operation is the master/slave architecture in which the master directs the simultaneous operation of the other (slave) converter(s) [5]-[8]. The master can be one of the converters or a supervising controller. From its special position in the system it can measure the whole load current, therefore it is easy for the master to enforce the current sharing policy [5], [7]-[8]. On the other hand, the traditional master/slave architecture has poor inherent fault tolerance, since the master constitutes a single point of failure for the entire system. This problem has been solved in our proposal by making all converters (master and slaves) equal in hardware and adding the possibility to reassign the master function at runtime, as described in Section IV.A.

Another solution to enhance reliability is to avoid distinction between master and slaves and address parallel operation with some form of droop control. With droop control, multiple converters can work in parallel and reach a stable current sharing operating point [9]-[14]. Droop control is even more attractive from the reliability point of view, because it can be operated without the need for dedicated communication channels among the converters [9]-[12]. The main drawbacks of droop control are its low control bandwidth and the inherent imprecision in the regulation of the grid parameters (voltage, frequency). Features of the current or voltage waveforms need to be carefully tuned or artificially introduced. Performance can be enhanced by allowing some form of communication, even low-bandwidth, among the converters [13]-[14].

Other proposals employ current sensorless operation in order to achieve better reliability, at the expense of poor regulation and circulating currents, especially at low load [15]. A possible solution is to supersize one of the converters so that it can potentially handle the whole parallel current for limited amounts of time [16] but this, in turn, results in a reduction of the overall system reliability, but it is impractical in case of MVA-class converters.

An interesting modular solution based on consensus-voting protocols has been proposed in [17]; in this case, the main drawback is related to the need for a totally connected network with an inherent spanning tree and a balanced Laplacian connection matrix, which might go missing in case of fault, making this solution rather vulnerable.

This paper presents a comprehensive fully digital control system for parallelable 50 Hz to 60 Hz, 2 MVA AC/AC converters for harbor application. The digital communication among the converters, needed to enforce load current splitting and convey timing and diagnostic information, is carried out through fiber-optic channels.

The system architecture is based on a master/slave concept with interchangeable master, which renders the system truly modular and more reliable than conventional master/slave. During parallel operation one of the

Manuscript received…; revised…; accepted…

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TII.2017.2776155, IEEE Transactions on Industrial Informatics

converters operates as master, the others operate as slaves. The master converter (Master in the following) generates the three-phase output voltage (voltage source inverter, VSI). The slave converters (Slaves in the following) act as current controlled voltage source inverters (CCVSI), splitting the load current evenly among themselves, then the system works as a balanced current divider. Moreover, the control is able to identify and switch off faulty converters, in order to maximize the availability of the system. In case of Master fault, its functions are transferred to another converter. The control algorithm was first developed and simulated in MATLAB/Simulink/PLECS environment, then a reduced current laboratory prototype, comprising one Master and one Slave, was built, and the control performances were verified by measurements on it. At the end, two 2 MVA converters were built and tested both in single and paralleled configuration, achieving a very good matching both with simulations and experimental results.

In the following, Section II describes the design of the system architecture and the control, while Section III reports the simulation results. Section IV shows the experimental results obtained both on the scaled prototype and the full-scale system, and conclusions are drawn in Section V.

II. System Achitecture and Control

The paralleled system architecture is illustrated in Fig. 1. The functions (Master and Slave) of the two converters are interchangeable, as they have the same hardware and software configuration. High-level control is performed by a PLC-based supervision system.

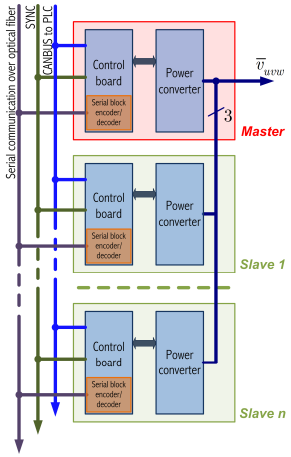

Fig. 1. Block diagram of the paralleled frequency converters.

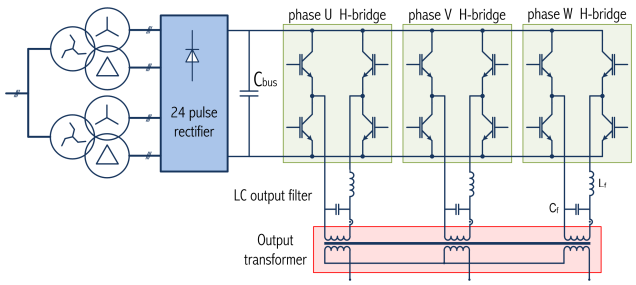

Fig. 2. Electrical scheme of each converter.

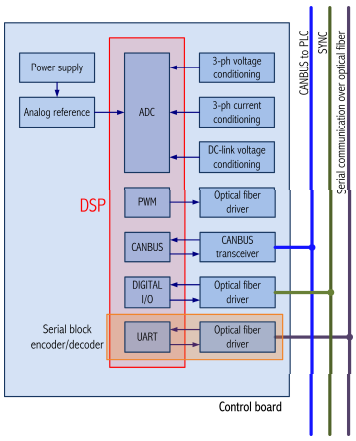

Fig. 3. Control board block diagram.

Different power converter architectures are suitable for frequency conversion according to the output power level, type of energy source and load, and specific application [1], [18]-[19]. The system described in this paper is based on AC/DC/AC 50Hz/690Vrms → 60Hz/460Vrms converters, with requirements of 94% and 4%, in terms of total efficiency and output THD, respectively. The inverter stage is built using 1.7 kV IGBTs, working with a PWM frequency of 2.88 kHz. This frequency was chosen among even multiples of 3×60 Hz in order for the maximum number of harmonics to be naturally canceled. Among the possible switching frequencies, thermal simulations using the *Infineon Iposim* tool helped choose the highest possible one compatible with thermal requirements.

The input stage is made by two zig-zag to wye/delta three-phase input transformers, supplying a 24-pulse rectifier, which produces a 900 V DC-link. Fig. 2 shows the implementation of the inverter, with three H-bridges plus LC filters connected to the primary side of the output transformer. Further details about the converter topology and components sizing can be found in [20].

A. The control board

Every converter is controlled by a Freescale MC56F8365 Digital Signal Processor (DSP)-based control board, which is described in detail in [21], [22]. As illustrated in Fig. 3, the control board incorporates control and synchronization I/O signals, optical fiber drivers for PWM signals and high speed serial digital communication, analog transducers conditioning, and a CANBUS transceiver. Insulated and compensated Hall effect transducers are used for measuring DC-link voltage, phase voltages and currents. The DSP manages several handshake signals, in order to control parallel operation. 1.8 Mbit/s serial communication is used for communicating voltage, angle and set-points among Master and Slave(s), while time reference for PWM synchronization between them is provided by two digital I/O signals, to avoid frequency beat phenomena.The communication with the PLC-based supervision system is guaranteed by a low speed CANBUS node.

B. The control algorithm

The Master operates as a three-phase VSI, for which a 60 Hz rotating *d-q* axes reference frame was selected for

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voltage control [23]. Park's transformations are used, with internal generation of the angle θ for rotation matrices. A feed-forward corrective action was added to compensate the voltage drop across the output inductors and the DC-link voltage variations [24].

As shown in Fig. 4, the Master and Slave(s) share the load current equally, with the Slave(s) operating as CCVSI. In order to obtain this feature, the Master-generated output voltage enters the Slave(s) current loops as a voltage disturbance, as done in electric drives; a feed-forward corrective action is required for this reason. The three-phase voltages commanded by the Master voltage control loop are a good estimation of this voltage disturbance. A high-speed optical fiber asynchronous serial bus allows the communication between the Master and the Slave(s).

Data frame synchronization and error detection are mandatory, as the data frame contains several data blocks (Fig. 5), and it is done by the addition of a header containing a bit pattern that cannot occur in the other data blocks. An 8-bit CRC is used for error detection as part of the data frame. Independent crystals generate the clocks of each paralleled converter but, to avoid frequency beating, their PWM driving signals must be synchronized. This is a fundamental task; as shown in Fig. 4, this is obtained by a signal (SYNC) broadcast by the Master on a dedicated fiber-optic bus, which contains temporal information about the occurrence of the PWM reload events: the Slaves measure the time displacement between the reload events of the Master and their own and, by means of a dedicated algorithm, make the needed adjustments to their PWM frequency.

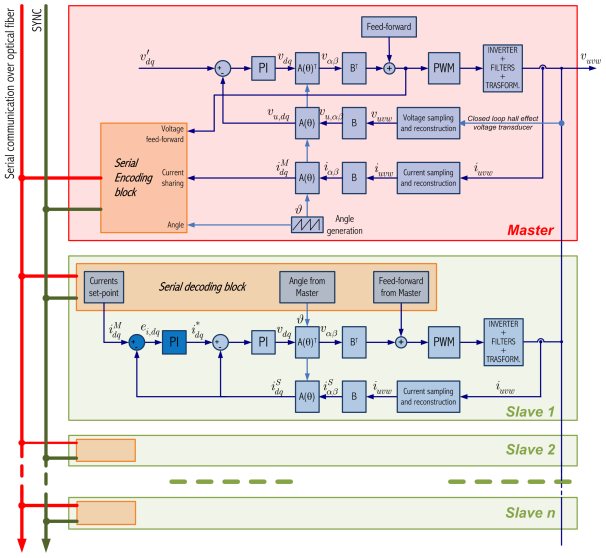

Fig. 4. Block diagram of the controls for parallel operation of one Master and one or more Slaves.

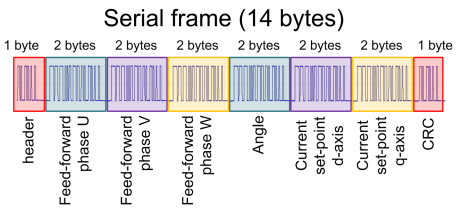

Fig. 5. 14-byte serial frame transmitted from the Master to the Slave(s).

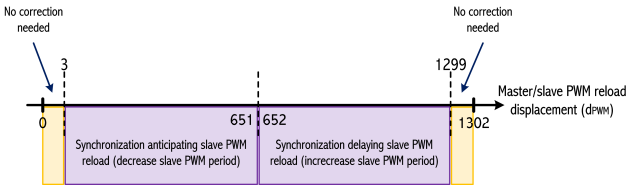

Fig. 6. Master and Slave(s) PWM synchronization details.

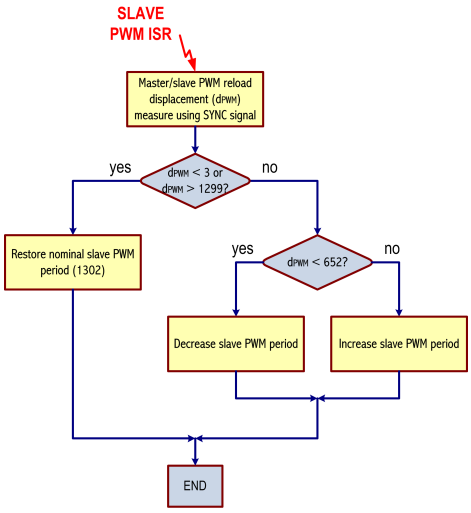

Fig. 7. Master and Slave(s) PWM synchronization algorithm.

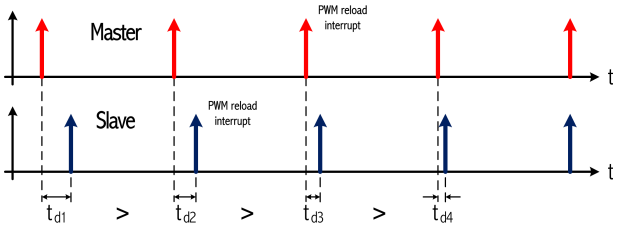

Fig. 8. Synchronization between Master and Slave(s) PWM signals.

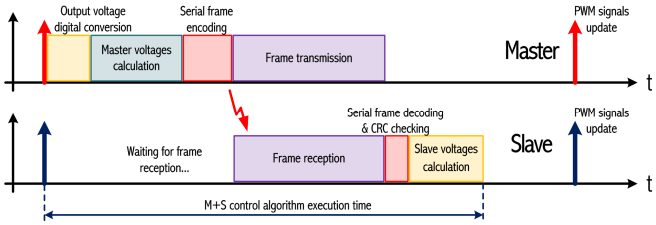

Fig. 9. Operations sequentially executed in a PWM period (347 µs).

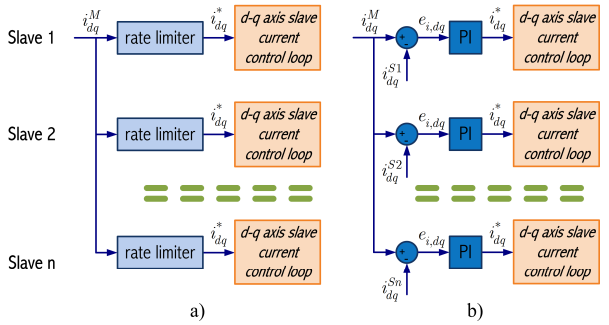

Fig. 10. The two tested current sharing strategies.

The measured displacement range is from zero to 1302 count pulses. The correction action needed to synchronize the PWM pulses of the converters depends on the displacement value (Fig. 6.). If the displacement is from

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3 to 651 count pulses the algorithm anticipates the Slave PWM reload (by a temporary decrease of its PWM period); vice versa, if the displacement is from 652 to 1299 count pulses, the algorithm delays the Slave PWM reload (by a temporary increase of its PWM period) as depicted in Fig. 7. This is the fastest way to perform the synchronization. When the displacement is less than 3 or greater than 1299 pulses the Master and Slave PWM are almost perfectly synchronized and no corrective action is necessary. The temporal evolution of the effects of the algorithm on the PWM reloads, in case of displacement lower than 652 pulses, is shown in Fig. 8.

During each PWM period the sequence of operations illustrated in Fig. 9 is executed: voltages calculation (M); data frame encoding and transmission (M); received data frame decoding and CRC check (S); voltages calculation (S); PWM signals update (M and S, at the same time).

The Master sends its currents (i_{dM}, i_{qM}) in the *d-q* reference frame and the angle θ for rotation matrices to the Slave(s). Based on this, each Slave controls a *d-q* reference frame current loop, as visible in Fig. 4 for Slave 1. This procedure allows a simple management scheme: the length of the communication frame is constant, regardless of the number of Slaves; moreover, since set-points are constant in steady-state conditions, a PI regulator is enough to cancel the steady-state error.

Using the same control parameters as in the simulation led to suboptimal results, due to non-idealities and other inherent differences between the model and the real converter. The regulators were therefore tuned using the heuristic Ziegler-Nichols tuning method [25].

C. Current sharing

To get an equal current sharing among two or more paralleled converter, two strategies, as illustrated in Fig. 10, were tested. The solution of Fig. 10(a) does not require any regulator. In parallel operation, the Master transmits to the Slave(s) its output current; Slave(s) use it as the input of a rate limiter, whose output is the Slave(s) current set-point.

Since the sum of the currents of all the parallel converters is equal to the total load current, an increase of a Slave current corresponds to a reduction of the Master output current, which in turn reduces the Slave current set-point; this loop continues until Master and Slave currents are equal. Fast load transitions are managed by the Master alone, since the rate limiter slope is properly tuned in order to avoid oscillations during current sharing transients.

The solution of Fig. 10(b) exploits a PI regulator to improve transient behavior, as in [5]. Each slave receives the Master output current as its set-point, comparing it with its own output current. The PI regulator forces the error $e_{i,dq}$ between Master and Slave currents to zero and, so doing, constrains the two currents to be the same. All the above considerations can be extended to the case of an arbitrary number of Slaves; Fig. 10(b) shows the outcome in case of one Master and two Slaves.

Solutions (a) and (b) were tested both on the prototype and the actual system. Since solution (b) exhibited the best performance, as will be shown in the next Section, it was adopted in the actual controller.

III. Simulation Results

The control was developed under MATLAB/Simulink/ PLECS environment [20]: Fig. 11 shows the single converter control architecture.

The step response was analyzed in order to test the dynamic behavior of the control. As shown in Fig. 12, the v_d step response has a rise time t_{rise} lower than 25 ms, which is compliant with the requirements. The response of the system to a load variation from zero to the rated value (2 MVA) was also simulated: Fig. 13(a) shows the output power on a resistive load; Fig. 13(b) shows the corresponding output voltages, where a small distortion is visible, compensated in less than 5 ms. The system response in case of overload was also simulated. Fig. 14(a) shows the active (P) and reactive (Q) power at system turn-on in case of 100% overload, while Fig. 14(b) shows the output voltages at the same conditions.

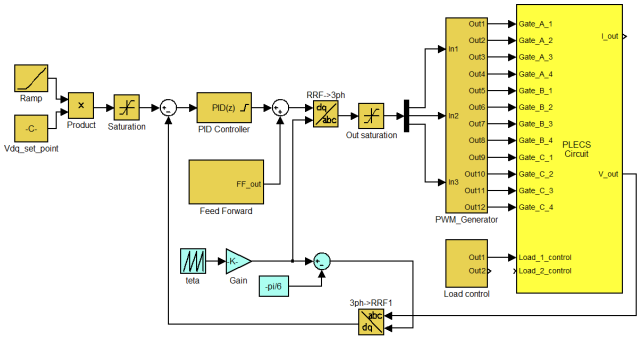

Fig. 11. Single converter control, implemented in MATLAB/Simulink.

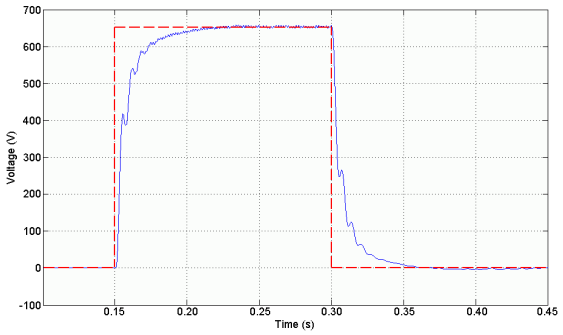

Fig. 12. Output voltage response for a v_d step.

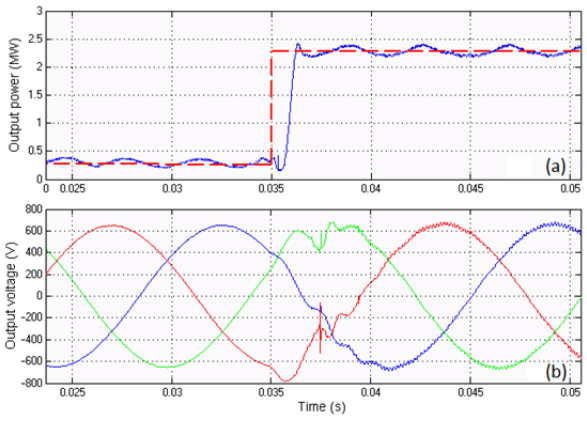

Fig. 13. Simulated output power on resistive load (a) and line to line output voltages (b) in case of load variation from zero to the rated value at t = 35 ms.

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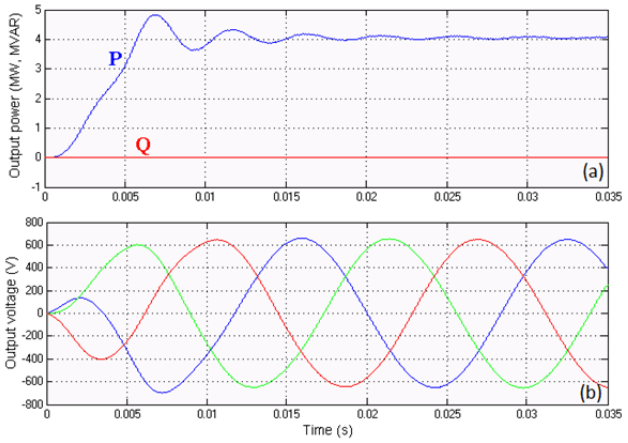

Fig. 14. System response in case of turn-on at 100% overload (load applied at t = 0): output power on resistive load (a) and line to line output voltages (b).

The behavior of the two described current sharing strategies was simulated. As shown in Fig. 15, with the solution based on the current limiter, oscillations appear in the three-phase current envelope, which give rise to overcurrent and system instability, especially at light load. On the contrary, the solution based on the PI controller works well in all tested load conditions (Fig. 16).

IV. MEASUREMENTS

A. Reduced-scale prototype

The reduced-scale prototype used to test the control board performance was composed by two identical converters with full-scale output voltage levels, but with rated current reduced by 1:500, and therefore a nominal power of 4 kVA each [20]. Tests were performed using the prototype both in single converter and Master+Slave configuration. A variable resistive-inductive load was used to assess the system's dynamic behavior. First of all, the response to voltage set-point steps was acquired, both at rated load and at no load, always obtaining a negligible steady-state error and good dynamic response, either with or without load disturbance, as shown in Fig. 17.

Output voltage harmonic distortion was also computed. Fig. 18 reports the prototype output voltage spectrum at rated load. The spectrum shows two spectral lines near the 2880 Hz switching frequency due to modulation (2880 ± 60 Hz), and near twice this frequency (5760 ± 60 Hz).

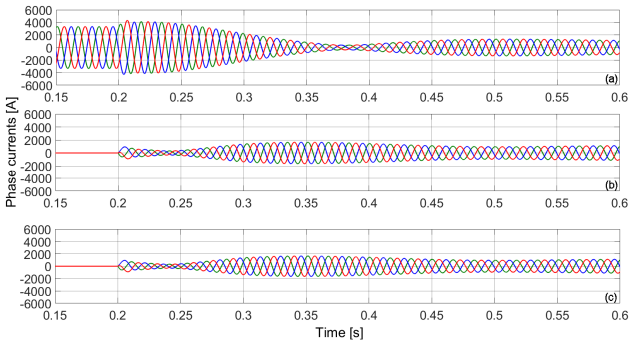

Fig. 15. Slave insertion (at t = 0.2 s) simulation of Master (a) and Slaves (b), (c) output currents, using current sharing control based on rate limiter.

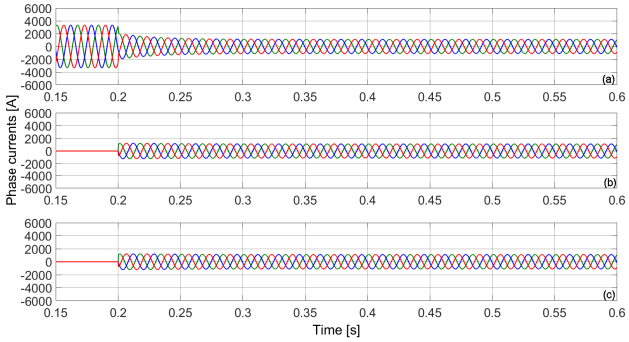

Fig. 16. Slave insertion simulation (at t = 0.2 s) of Master (a) and Slaves (b), (c) output currents, using current sharing control based on PI controller.

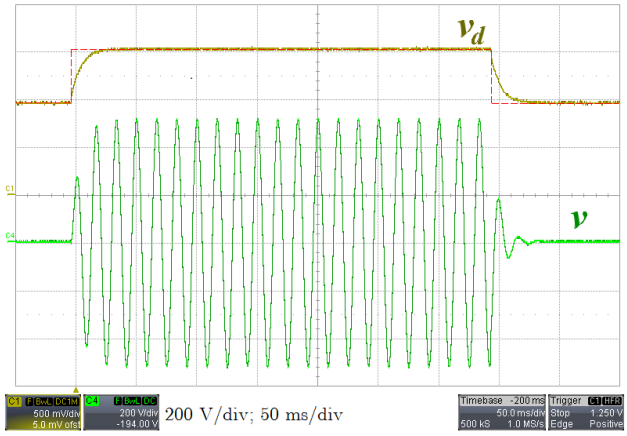

Fig. 17. System response. d-axis voltage v_d and line to line output voltage v.

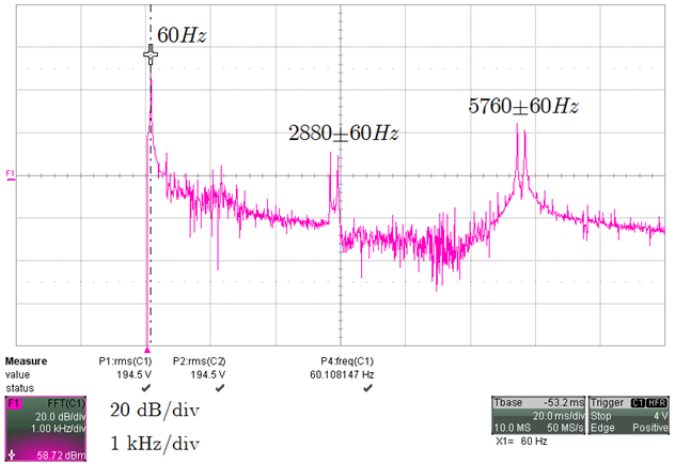

Fig. 18. Line to line output voltage spectrum for the reduced-scale prototype at rated load in single operation.

Fig. 19. shows the undistorted output voltages with precise nominal amplitude and the correct displacements (120 degrees from each other). All the spectral components are about 40 dB lower than the fundamental at 60 Hz, and the THD was less than 1% in all load conditions (computed with a MATLAB script starting from data of Fig. 19.).

Fig. 20 shows the load transient rejection with a fixed voltage set-point of the rated value: the effects of the load variation on the voltage control complies with the specifications.

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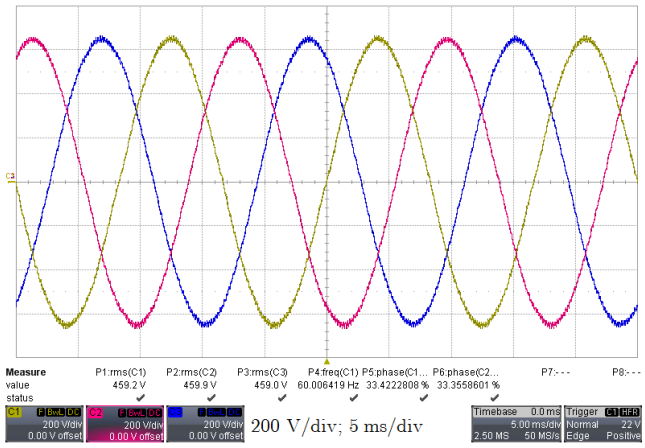

Fig. 19. Line to line output voltages waveforms.

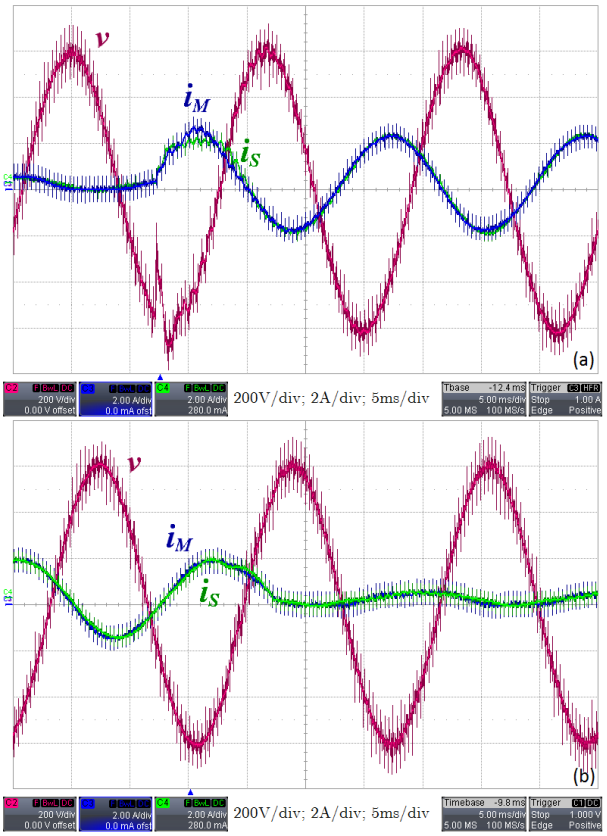

Fig. 20. Load transient from zero to rated value (a), and vice versa (b). *v*: line to line output voltage, i_M: Master output current, i_S: Slave output current.

The transient during Slave turn-on, in case of current sharing strategy based on the rate limiter, is shown in Fig. 21: after less than 500 ms, a balanced current between converters is reached, without oscillations. As mentioned in the introduction, in case of Master fault, its functions are transferred by the supervising PLC to one of the Slaves, as described in Fig. 22. The PLC knows the operating history of all the converters and selects as Master the one with the least operating life. The off-line time of Fig. 22 is about 6 ms long, and it could be dramatically reduced if the converters were allowed to negotiate by themselves, bypassing the supervising PLC. Nevertheless the system specifications, for safety reasons, mandate that all the decisions making must be done with the intervention of the PLC.

B. *Full-size system*

After testing and setting up the control on the scaled prototype, until specifications were satisfied, two full size converters were built (Fig. 23) and tested, and measurements on the whole system were performed.

Since the rated current for each converter is 2500 A, with a maximum apparent power of 2 MVA, the measurements done on the prototype were not practically feasible in laboratory on the real system using a resistive load. The paralleled converters transient response for load variation between zero and 450 Arms was measured (Fig. 24), showing that the correct voltage waveform was recovered within 2 ms. A similar behavior was obtained in case of load release (from 280 Arms to zero), as shown in Fig. 25.

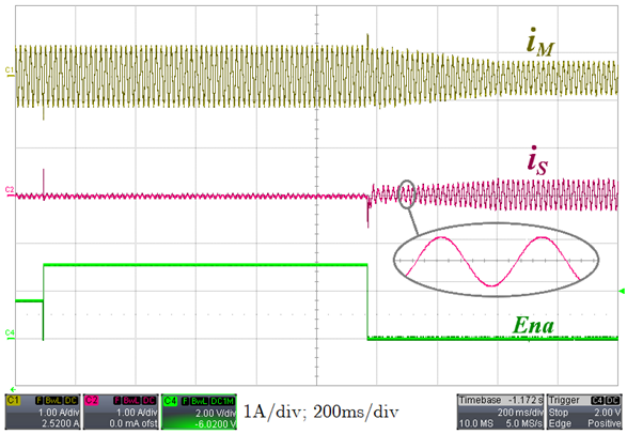

Fig. 21. Slave turn-on transient. i_M: Master output current, i_S: Slave output current , *Ena*: Slave enable signal (active low).

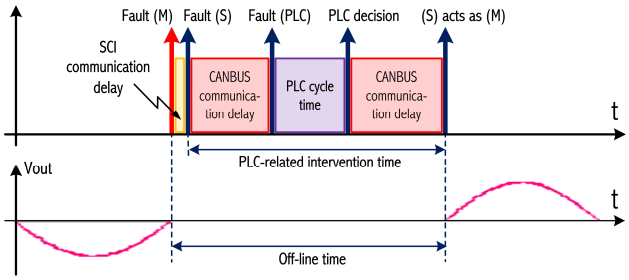

Fig. 22. Safety procedure in case of Master fault.

Fig. 23. Picture of one of the 2 MVA converters.

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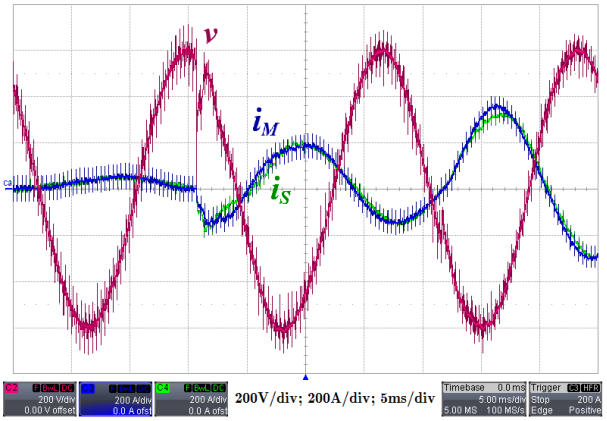

Fig. 24. Load transient from zero to about 450 Arms. v: line to line output voltage, i_M: Master output current, i_S: Slave output current.

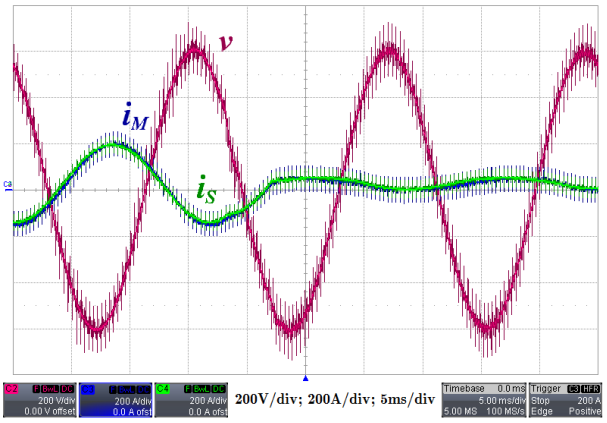

Fig. 25. Load transient from a total current of about 280 Arms to zero. v: line to line output voltage, i_M: Master output current, i_S: Slave output current.

The behavior of the system without load was the same as the prototype. The unbalanced conditions behavior was tested in depth, since it is very important for the application. Unbalanced load gives rise to asymmetric phase voltage drops and, consequently, a negative sequence voltage can appear, which can be seen as a 120 Hz disturbance in the *d-q* reference frame. The 120 Hz ripple in the output voltages depends on the gain of the voltage regulators at that frequency. To test the negative sequence rejection of the control, a 10% load asymmetry was introduced in one phase. The measurements of the output voltages (Fig. 26) show a ripple on the *q*-axis voltage of about 40 V peak-to-peak, corresponding to a damping of the disturbance by a factor of about three.

The PI strategy has been used for current sharing control in the actual system. In order to test its behavior near the nominal power, a pure inductive load was used, since this absorbs from the grid only the power converters losses. Moreover, this condition (i.e. without load damping) is the most critical from the point of view of oscillations. Output voltage and currents measured on the full-scale converter in Master+Slave configuration, with a current of about 2500 Arms, are reported in Fig. 27, showing stable operation and even current distribution between the converters.

The converter was installed in a harbor in southern Italy and used to supply a large ship to test the performance on a real application. Fig. 28 shows, as an example, output voltages and currents during a load variation from 500 Arms to 1000 Arms.

V. Conclusion

A comprehensive control system for modular harbor application AC/DC/AC frequency converters was presented. This architecture, based on a Master-Slave approach, guarantees high availability. The Master operates as a three phase VSI with a *d-q* reference frame voltage control, while Slaves act as CCVSIs with current control loops on a *d-q* reference frame plus a feed-forward contribution.

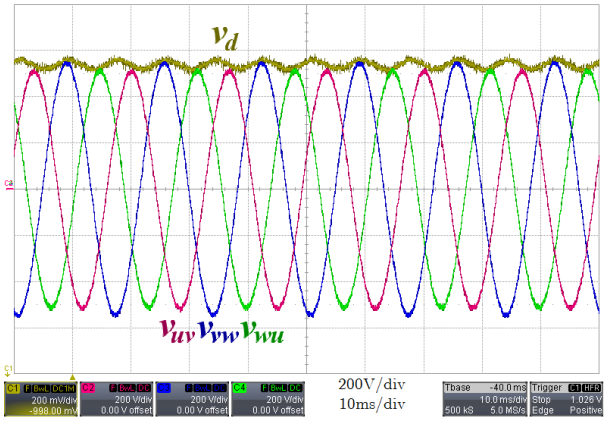

Fig. 26. Three-phase line to line output voltage (v_{uv}, v_{vw}, v_{wu}) and v_d in case of asymmetric load. Constant nominal voltage set-point.

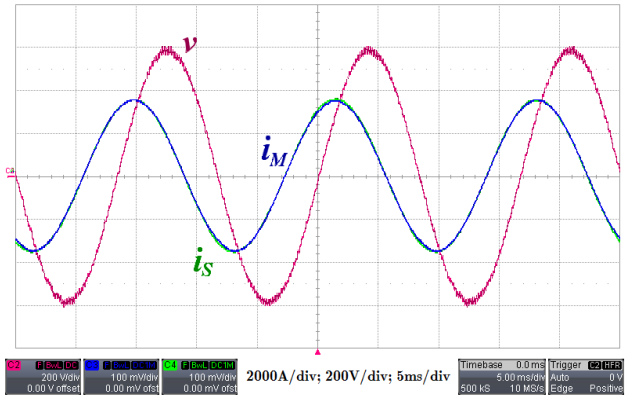

Fig. 27. Full-scale Master+Slave with pure inductive load. v: line to line output voltage, i_M: Master output current, i_S: Slave output current. Constant nominal voltage set-point.

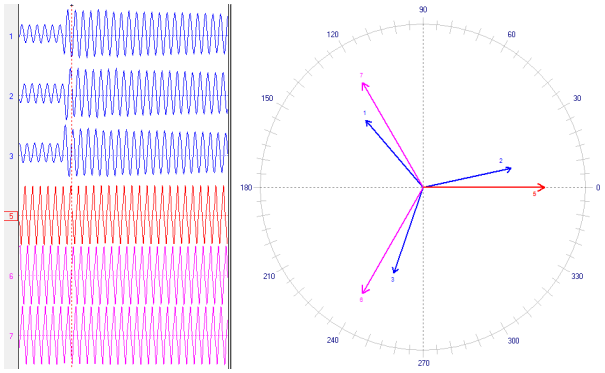

Fig. 28. Line currents (blue) and line to line output voltages (red) measured in harbor. Timescale traces (left); phasor diagram (right).

The control architecture was designed and simulated in the MATLAB/Simulink/PLECS environment and tested on a reduced-scale prototype. Measurements and control fine tuning were conducted on the prototype, in Master+Slave configuration, reaching good performance in terms of THD, dynamic response, and current sharing. The voltage control showed also good rejection to load disturbances, getting good output voltages even with a 100% load unbalance. Simulations and experimental results resulted on a good agreement.

Once the control was completely tuned on the prototype, two 2 MVA converters were built and tested. Measurements performed with pure inductive load near full load confirmed the good behavior of the control. Finally, the system was installed in a harbor and successfully tested supplying a large ship.

REFERENCES

[1] J. W. Kolar, T. Friedli, J. Rodriguez and P. W. Wheeler, "Review of Three-Phase PWM AC–AC Converter Topologies," *IEEE Trans. on Ind. Electronics*, vol. 58, no. 11, pp. 4988-5006, Nov. 2011.

[2] N. Singh and V. Agarwal, "Delta-Modulated AC–AC Converter for PM WECS," *IEEE Trans. on Ind. Informatics*, vol. 11, no. 6, pp. 1422-1434, Dec. 2015.

[3] F.A. Furfari, "The evolution of power-line frequencies 133 1/3 to 25 Hz", *IEEE Industry Applications Magazine*, vol. 6, no. 5, pp. 12–14, 2000.

[4] E. C. dos Santos, N. Rocha and C. B. Jacobina, "Suitable Single-Phase to Three-Phase AC–DC–AC Power Conversion System," *IEEE Trans. on Power Electronics*, vol. 30, no. 2, pp. 860-870, Feb. 2015.

[5] R. P. Singh and A. M. Khambadkone, "Current Sharing and Sensing in N -Paralleled Converters Using Single Current Sensor", *IEEE Trans. on Ind. Applications*, vol. 46, issue 3, pp. 1212–1219, May-Jun. 2010.

[6] L. Yuesheng, L. Da, S. Guiying and T. Yanbin, "Master-slave control strategy for input-series output-parallel connected flyback converters," *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, Hefei, 2016, pp. 907-911.

[7] B. M. H. Jassim, D. J. Atkinson and B. Zahawi, "Modular Current Sharing Control Scheme for Parallel-Connected Converters," *IEEE Transactions on Ind. Electronics*, vol. 62, no. 2, pp. 887-897, Feb. 2015.

[8] S. Chae, Y. Song, S. Park and H. Jeong, "Digital Current Sharing Method for Parallel Interleaved DC–DC Converters Using Input Ripple Voltage," *IEEE Trans. on Ind. Informatics*, vol. 8, no. 3, pp. 536-544, Aug. 2012.

[9] U. Borup, F. Blaabjerg and P.N. Enjeti, "Sharing of nonlinear load in parallel-connected three-phase converters", *IEEE Trans. on Ind. Applications*, vol. 37, issue 6, pp. 1817–1823, Nov.-Dec. 2001.

[10] H. C. Chiang, K. K. Jen and G. H. You, "Improved droop control method with precise current sharing and voltage regulation," *IET Power Electronics*, vol. 9, no. 4, pp. 789-800, 3/30/2016.

[11] G. Buticchi, M. Liserre, D. Barater, C. Concari, A. Soldati and G. Franceschini, "Frequency-Based Control of a Micro-grid with Multiple Renewable Energy Sources", in *Proc. IEEE ECCE 2014*, Pittsburgh, PA, USA, 14-18 Sept. 2014.

[12] A. van der Krans and K. Bouwknegt, "A control strategy for the redundant parallel operation of an ensemble of static ups systems of the parallel type", in *Proc. EPE 1991*, Florence, Italy, September 3-6 1991, pages 3–148 — 3–152.

[13] X. Wei, G. Zhu, J. Lu and X. Xu, "Instantaneous current-sharing control scheme of multi-inverter modules in parallel based on virtual circulating impedance," *IET Power Electronics*, vol. 9, no. 5, pp. 960-968, 4/20/2016.

[14] X. Lu, J. M. Guerrero, K. Sun and J. C. Vasquez, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy," *IEEE Trans. on Power Electronics*, vol. 29, no. 4, pp. 1800-1812, April 2014.

[15] J. A. Abu Qahouq, L. Huang and D. Huard, "Sensorless Current Sharing Analysis and Scheme For Multiphase Converters," *IEEE Trans. on Power Electronics*, vol. 23, no. 5, pp. 2237-2247, Sept. 2008.

[16] K. Sun, X. Wang, Y. W. Li, F. Nejabatkhah, Y. Mei and X. Lu, "Parallel Operation of Bidirectional Interfacing Converters in a Hybrid AC/DC Microgrid Under Unbalanced Grid Voltage Conditions," *IEEE Trans. on Power Electronics*, vol. 32, no. 3, pp. 1872-1884, March 2017.

[17] S. Moayedi, V. Nasirian, F. L. Lewis and A. Davoudi, "Team-Oriented Load Sharing in Parallel DC–DC Converters," *IEEE Trans. on Industry Applications*, vol. 51, no. 1, pp. 479-490, Jan.-Feb. 2015.

[18] N.A. Ahmed, "Three-phase high frequency AC conversion circuit with dual mode PWM/PDM control strategy for high power IH applications", *World Academy of Science, Engineering and Technology*, vol. 45, pp. 370–376, 2008.

[19] T. Ohkami, T. Fujimoto, H. Ito, S. Konno, T. Tanaka, K. Ito, M. Imura, S. Ota, M. Tobita, A. Kawaguchi, N. Kawakami, K. Takagi, K. Shimada, H. Aizawa, H. Kuroda,T. Kobayashi, M. Takechi, and K. Kato, "Development of 300 MW frequency converter", in *Proc. 2010 IEEE International Power Electronics Conf.*, pp. 2964–2969.

[20] A. Toscani, P. Cova, F. Bertoluzza, N. Pini, G. Franceschini, "Fault tolerant digital control of 2 MVA parallelable frequency converters for harbor applications", in *Proc. IEEE IECON 2012*, pp. 416–421.

[21] P. Cova, G. Franceschini, A. Toscani, "Development of synchronized control for multiple 2 MVA AC/AC converters", in *Proc. IEEE ENERGYCON 2012*, pp. 152–157.

[22] C. Concari, P. Cova, G. Franceschini, A. Toscani and F. Bertoluzza, "Improved control strategy for modular 2MVA AC/AC power converter," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 5294-5300.

[23] G. J. Retter, *Matrix and space-phasor theory of electrical machines*, Budapest, Akademiai Kiado, 1987, pp. 211–224.

[24] G. Buticchi, G. Franceschini, E. Lorenzani, "A DC offset current compensation strategy in transformerless grid-connected power converters", *IEEE Trans. on Power Delivery*, vol. 26, n. 4, pp. 2743–2751, Oct. 2011.

[25] J. G. Ziegler and N. B. Nichols, "Optimum settings for automatic controllers", *Trans. ASME*, vol. 64, pp. 759–768, 1942.

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