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A Method to Extract Lumped Thermal Networks of Capacitors for Reliability Oriented Design

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Abstract – In this work we propose a procedure based on finite element simulations to compute a lumped-parameter thermal model of capacitors. The extracted Foster or Cauer network coupled to the electrical model can be useful to evaluate the temperature of capacitors in circuit simulators as SPICE or Simulink. In this way, it is possible to evaluate the expected maximum operative temperature of the capacitor embedded in a circuit before its real application, avoiding unexpected failures since the prototyping stage. Here, we describe the workflow of the method and, finally, the proposed approach will be used for designing snubber capacitors for medium power (60 kW) high frequency AC/AC converter.

1. Introduction

Capacitors are widely used in power converters for different tasks. Snubbers and DC-links are typical power applications where capacitors play important roles. In fact, they ensure essential features of signal integrity, stability, or protection of devices composing the circuit.

A lot of works can be found in literature on the reliability of capacitors with different kind of dielectrics. This can be considered the most stringent constraint required in many applications (e.g., automotive, aerospace, high-energy physics experiments), keeping interest high on all the activities related to the reliability of capacitors. Indeed, in the power electronic circuits operation field, capacitors are among the devices that cause the most frequent system failures [1]. In harsh environments, as those of vehicles, where the ambient temperature can be high [2], or in circuits where capacitors have to be close to other power dissipating devices to satisfy some layout constraints (e.g. due to EMC or parasitic restrictions), even if the self-heating does not produce high temperature increase, the capacitor temperature can be higher than the maximum operative temperature declared by manufacturers to guarantee specific features and performances, as, for example, the Mean Time To Failure (MTTF).

Electronics designers often focus on the thermal management of transistors, diodes, or power modules, neglecting the proper cooling of devices with low self-heating as capacitors. Then, many times, this leads to experiencing high temperatures in capacitors, accelerating their aging up to get catastrophic failures within a brief span of time. Typically, the latter happens during early prototyping phases, causing delays and unexpected development costs.

In literature there are studies on the electro-thermal analysis to evaluate the mission profile of DC-link for power converters [3,4]. These works also proposed reliability-oriented procedures to optimize the DC-link design once known the hotspots. Other works, as the one shown by Wang et al. in [5] on film capacitors for RCD snubbers, are focused on the MTTF evaluation.

Here we propose a method to evaluate a thermal network which can be used for the procedures developed in [3,4]. This can be considered the main novelty of this paper.

Typically, for snubbers and DC-link applications, metallized film and electrolytic capacitors are used. Their aging is affected by the temperature. Although to greater degree this problem affects electrolytic capacitors [6], it cannot be neglected for metallized film ones [7-13].

Commonly, models used for capacitor lifetime prediction are based on the Arrhenius law for temperature-dependent stresses, both for metallized film (e.g. that proposed by Dakin in [14]) and electrolytic capacitors (e.g. that proposed by Jánó and Pitica in [15]).

The temperature-related aging of metallized plastic capacitors is basically modelled by an exponential Arrhenius law with the activation energy of a thermal process [3,16,17], that is a stress-dependent quantity. Experimentally, concurrent stresses typically cause slightly less degradations than those obtained from a simple multiplicative model, and the Arrhenius law can be generalized with the Eyring theory [18]. In this way, more factors than the temperature can be accounted for the lifetime estimation, adding an interaction term for each factor. Then, the interactions of thermal stress with other stress factors, such as for example the voltage V and relative humidity RH, are considered evaluating the useful life of the component (τ_{Eyring}) with the following equation [19]:

$$\tau_{Eyring} = AT^{\alpha} exp\left[\frac{E_a}{kT} + S_V\left(B_V\frac{C_V}{kT}\right) + S_{RH}\left(B_{RH}\frac{C_{RH}}{kT}\right)\right], \qquad (1)$$

where S_V and S_{RH} are functions of the supplementary stresses (voltage and relative humidity), respectively, k is the Boltzmann constant, T is the temperature in Kelvin, E_a is the activation energy, α, A, B_V, C_V, B_{RH}, and C_{RH} are constants to be heuristically determined, independent of time, temperature and stresses.

Moreover, different works can be found in literature where the metallized film capacitors lifetime is affected by the temperature and other stresses, mainly the electrical ones [20-23]. The same can be said about electrolytic capacitors, but the heuristic models can be different [15,24-26].

In practice, the most widely used empirical model to

evaluate the lifetime of capacitors contemplates the influence of temperature and voltage stress as shown in the following equation [3]:

$$L = L_0 \left(\frac{V}{V_0}\right)^{-n} exp\left[\left(\frac{E_a}{k}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right], \quad (2)$$

where: L and L_0 are the lifetime under the actual operating condition and reference testing condition, respectively; V and V_0 are the voltage applied during actual and reference tests, respectively; T and T_0 are the temperature in Kelvin measured during actual operating phase and reference test, respectively; n is the voltage stress exponent to be heuristically evaluated. The values of E_a and n are the key parameters to be determined in the above model in order to evaluate the capacitor lifetime, but the temperature has to be known. It can be measured or simulated.

The method here presented can be useful for reliability-oriented design of power systems because it gives a way to obtain a lumped-parameters thermal model of capacitors that usually is not available to the designers. Unfortunately, as above mentioned, the operating temperature affects the capacitors lifetime. Therefore, a thermal model, which can be easily coupled with the electrical model by designers, can be useful to estimate their operating temperature and lifetime [3,4]. It has been conceived to solve some problems occurred during the development of power converters. For example, the proposed method was applied for designing snubber capacitors to be used for a medium power (60 kW), high frequency AC/AC converter (Fig. 1) [27]. In this converter, the ripple due to line rectifying has not been filtered using large electrolytic capacitors, but only small fast capacitors have been used as snubber. These capacitors have been placed near the switching devices to filter voltage peaks due to switching. Film capacitors guarantees extended lifetime, reduced power losses, and small volume occupancy. This type of application is very critical and the proposed procedure has been very helpful to validate the design.

The capacitor dimensioning considers not only the self-heating, but also the heat transfer between the copper bus bars connected directly with the power devices (uncontrolled diode input rectifier and IGBTs) and the capacitor (Fig. 2). During early tests on the first prototype made without taking care of the capacitors heating, these devices failed shortly. Fig. 3 shows these capacitors after the early tests with clear damages. Fig. 4 shows another example of a capacitor failure. In this case, not only the melted metallized polypropylene tape coils can be seen, but also the copper strips and the resin, which is the blue filling of the package. This automotive DC-link was brought to failure in a test to determine its lifetime at a specific load.

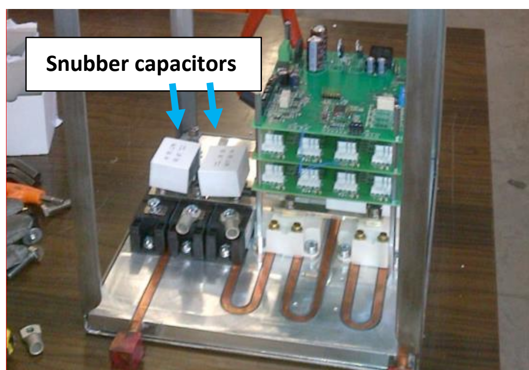

Fig. 1. The converter with a snubber designed using the proposed procedure.

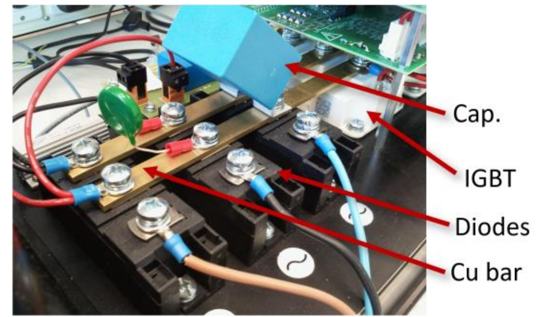

Fig. 2. Thermal coupling, via copper bars, between the snubber capacitor and other power devices of the converter (uncontrolled diode input rectifier and IGBTs).

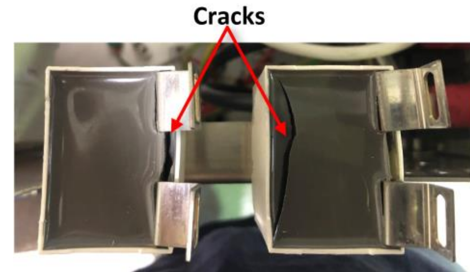

Fig. 3. Capacitors failed during the first test of the converter in Fig. 1: both packages are cracked, and the plastic film is damaged.

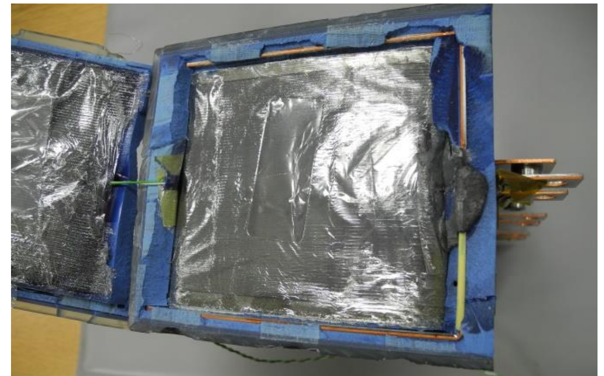

Fig. 4. Automotive DC-link failed during reliability tests (courtesy of TDK Electronics AG).

These examples demonstrate that the reliability of capacitors is always interesting to manufacturer who are innovating their products. Then, the method here presented to evaluate a compact thermal model for capacitor, can be useful not only for electronics designers. Clearly, during the capacitor development, the procedure can be changed because simulations can be replaced with measurements.

2. The Method

The proposed procedure is based on the use of Finite Element Analysis (FEA) to evaluate the temperature of capacitors both during a power step response, and normal operation. The aim of this FEA is the computation of temperature at inner points of the capacitor, where it is not possible to execute direct thermal measurements, because they are built without embedded temperature sensors. As a matter of fact, the temperature for lifetime analysis is the maximum one, and this is reached inside the capacitor, typically close to the center.

To obtain large capacitance by limiting the size, the

capacitor is multi-layered, putting in parallel many electrode-dielectric-electrode structures. Depending on the dielectric, the final structure can be a hexahedral stack, or wrapped to be housed in cylindrical cases, or wrapped and pressed to be contained in hexahedral cases. Anyway, the large number of thin layers leads to huge number of degrees of freedom in FEA, which limits the possibility to simulate a model with a 3D geometry like that of the real capacitor. Then, the questions are: what simplification can be made and whether the approximation due to it leads to acceptable errors in the simulation results? This is the typical validation problem of Finite Element Models (FEMs) and, generally, of all numerical models.

Fig. 5 shows the procedure applied in this work to overcome this problem, mainly for transient simulations. It considers the validation of the model with measurements on a reference capacitor executing ad-hoc tests [28]. In parallel to the measurements, it is possible to setup a Finite Element (FE) electro-thermal model with an accurate capacitor 3D geometry.

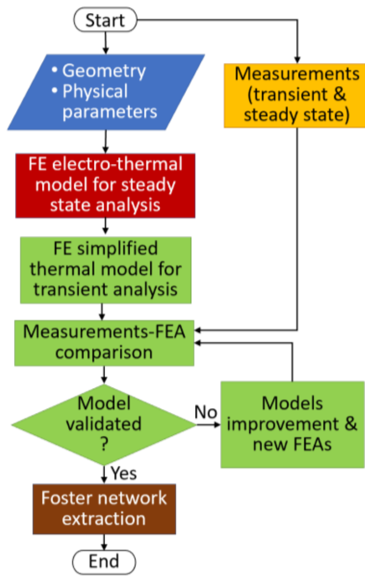

Fig. 5. Workflow of the proposed procedure.

When the capacitor is big, the accurate model can be replaced by a single electrode-dielectric-electrode structure with a limited area, because the coupled electro-thermal analysis is necessary to evaluate the dissipated power density to set a power step in the following transient analysis. In the thermal transient model, the geometry is simplified considering the domain of the stack, or the wound built to obtain a specific capacitance as a unique volume of homogeneous material (Fig. 6), whose thermal properties are evaluated as a weighted average of the properties of metal and dielectric layer as follows:

$$p_{hom} = (\rho_m V_m p_m + \rho_d V_d p_d)/(\rho_m V_m + \rho_d V_d), \quad (2)$$

where p_{hom}, p_m and p_d are the thermal properties (e.g. thermal conductivity or heat capacity) of the equivalent homogenous material, the metal of electrodes and the dielectric, respectively; ρ_m and ρ_d are the densities of the electrodes and the dielectric, respectively; V_m and V_d are the volumes of all electrodes and of the whole amount of dielectric layers, respectively.

Finally, once validated the model, a thermal network (e.g. Foster network or a multiple input network to account for mutual influence of other dissipating devices of the circuit) can be extracted considering the point at maximum temperature of the capacitor. The thermal network extraction can be done using previously validated methods (e.g. using optimization solvers to minimize the error between the measured or simulated thermal impedance and the one computed by the lumped-element network).

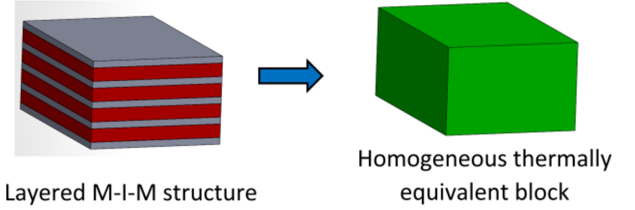

Fig. 6. Approximation of the Metal-Insulator-Metal (M-I-M) stack with a homogeneous thermally equivalent block for transient simulations.

3. Experimental Case Study

As case study, a metallized polypropylene (PP) capacitor with $C = 1$ µF, rated AC voltage of 305 V, maximum continuous DC voltage V_{DC} = 630 V, and maximum rating temperature $T_{\text{op,max}}$ = 105 °C, was chosen as test device to obtain the lumped-element thermal network. It was inspected to measure the thickness of metal (2 µm) and dielectric (10 µm) layers. The dissipation factor $tan\delta$ was measured by an LCR meter at 100 kHz. This frequency has been set during electro-thermal characterization, carried out with an ad-hoc test bench to have a sinusoidal voltage applied to the capacitor with the classic RLC series circuit in Fig. 7, where C is the Device Under Test (DUT).

The square wave generator E has been realized as shown in Fig. 8 using a half-bridge with power GaN FET TPH3212PS from Transphorm. These transistors have an on-resistance of about 70 mΩ, which can be assumed as the resistance of the RLC series. Then its damping ratio is negligible.

Fig. 9 shows the test bench realized, while Fig. 10 shows the traces of the drain-source voltage of the half-bridge pull-up transistor (cyan), the gate-source voltage of the same transistor (blue), and the capacitor voltage v_c(t) (green) acquired by the oscilloscope with a frequency of 100 kHz and an amplitude of 8 V of the sinusoidal component of $v_c(t)$.

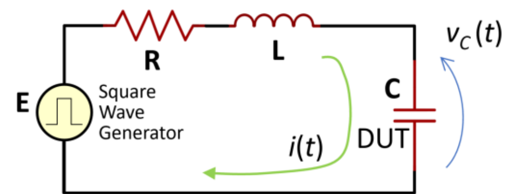

Fig. 7. Schematic of the circuit used for electro-thermal characterization.

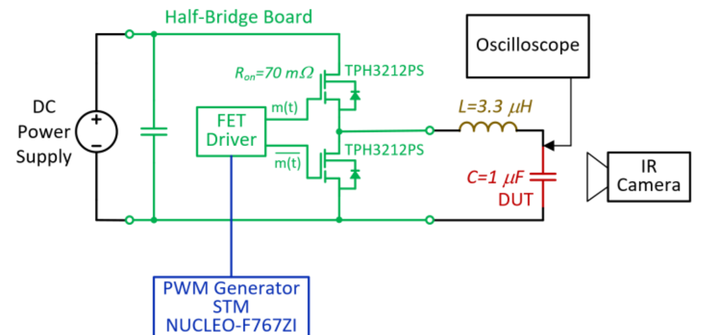

Fig. 8. Test bench schematic diagram.

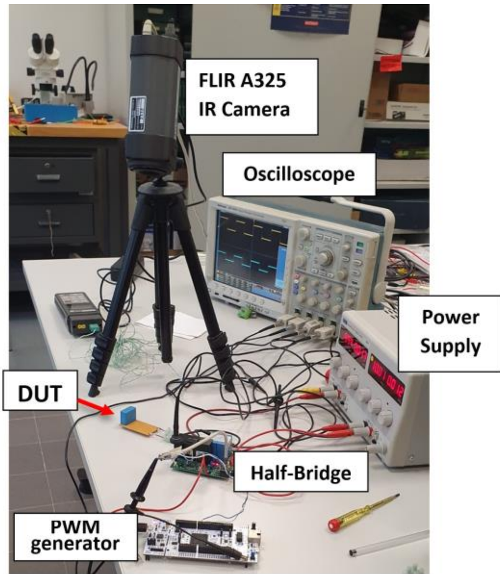

Fig. 9. Test bench used for electro-thermal characterization.

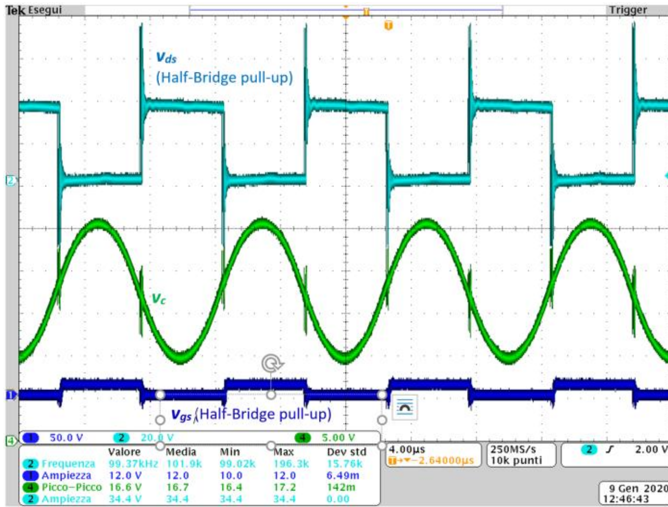

Fig. 10. Measurement of the capacitor voltage during a test with a peak-to-peak amplitude $V_{pp} = 16$ V sinusoidal ripple at 100 kHz.

4. Modeling and Validation

There are different ways to model a capacitor. For example, in SPICE it can be modeled with lumped elements as in Fig. 11. Here, C is the capacitance, R_s, and L_s are the Equivalent Series Resistance (ESR) and the Equivalent Series Inductance (ESL), respectively, while R_p is the insulation resistance, R_d is the resistance representing the dielectric loss due to dielectric absorption and molecular polarization, and C_d is the capacitance due to the inherent dielectric absorption [29].

Typically, a simplified capacitor model is used, composed only by C and R_s and the dissipation factor representing the capacitor losses is $\tan\delta = \omega R_s C$.

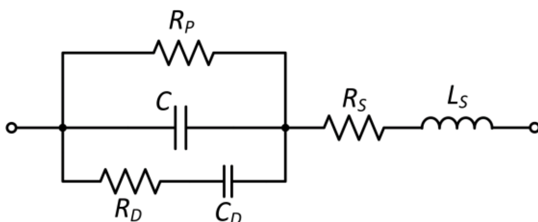

Fig. 11. Lumped element model of a capacitor.

In SPICE simulations, the temperature can be evaluated by adding a lumped-parameter network modeling the thermal behavior with the power dissipated by the capacitor.

As noticed in [5], the values of the elements of Fig. 11 are dependent by the operating conditions (e.g. frequency, voltage, frequency, temperature, and time), and, when this dependence is not considered, the analysis of electro-thermal stresses may be not carried out properly. Therefore, many times the lifetime prediction is quite different to the real one. The thermal behavior fully coupled to the electrical one is almost impossible to calculate easily. Simulations can be the solution to this problem.

In order to compute a thermal network of a capacitor, it can be modelled within a 3D physical simulator. In this case, the capacitor taken as reference to show how the proposed method can be applied, was modeled by COMSOL Multiphysics 5.3. The geometry for the electro-thermal stationary study was drawn without terminals, and the wrapped metalized layers were modeled as a simpler stack. Due to the symmetries, it was possible to study a quarter of the whole capacitor. The measured dissipation factor was set as the dielectric *tanδ*. The electrical model was completed applying alternatively to the dielectric layers a ground and a sinusoidal voltage as shown in Fig. 12.

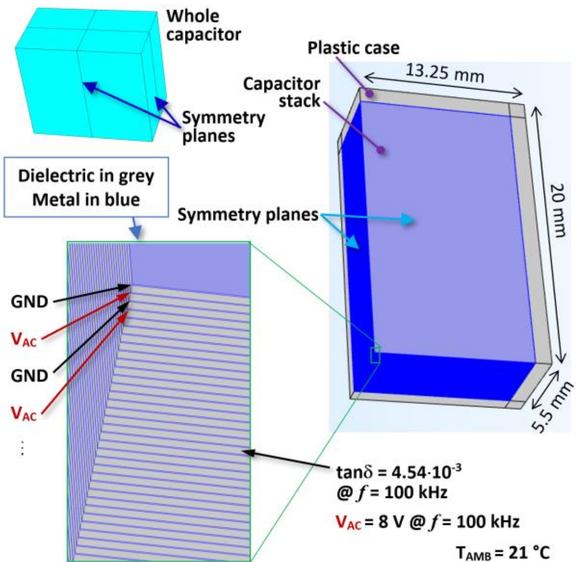

Fig. 12. FE model of the capacitor for electro-thermal analysis.

For the Heat Transfer physics in COMSOL, the boundary conditions were set as natural air convection with different values at the vertical and horizontal surfaces.

The Electric Current physics module of COMSOL requires a fine meshing to have a negligible discretization error on the simulation result. In this case, the matching between the steady state simulation results and measurements is good, but for a transient study this fully coupled electro-thermal model is quite expensive in terms of computing power. Thus, we applied further approximations on the model as shown in Fig. 6, and using the heat generated in the steady state study, a transient simulation with a power step was carried out. As can be seen in Fig. 13, showing thermal maps at the end of the transient, the match with measurements is good. Fig. 14 shows the temperatures measured and simulated in the point of the marker depicted in Fig. 13 (top-left). Here, it can be seen that also during the transient the matching is good, and at steady state the difference is less than 0.3°C.

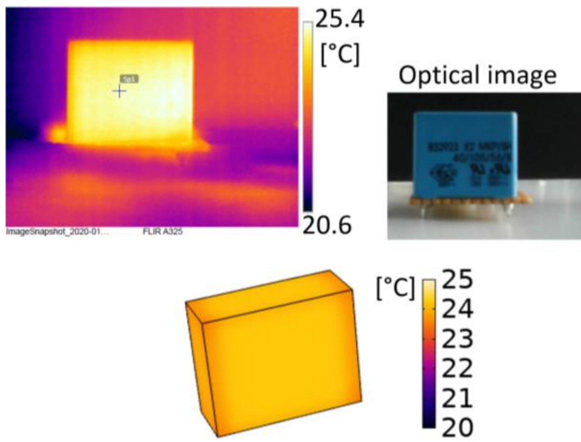

Fig. 13. Measured (top-left) and simulated (bottom) external thermal map at the end of transient (steady state) with $V_{AC} = 8$ V, $f = 100$ kHz.

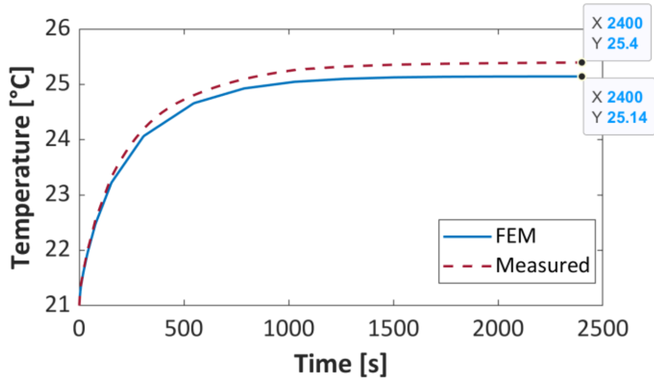

Fig. 14. Simulated and measured temperatures at the point of the marker in Fig. 13 (top-left) during a power step response with $V_{AC} = 8$ V, $f = 100$ kHz.

Obviously, in the center of the capacitor taken as reference (Fig. 13 top-right) where the maximum temperature can be expected, it is not possible to measure the temperature. Then, the FEM simulation can be assumed as a sort of indirect measurement.

Once the thermal power step response is obtained, it is possible to extract the Foster network of Fig. 15 following the procedure in [30]. This models the DUT of the test bench in Fig. 8, then the ground is the ambient temperature and P_d is the dissipated power during the power step. There is only one point with physical meaning, the center of the capacitor where the temperature is T_{center_cap}. The 3D heat flow of this capacitor cannot be modelled with a Cauer network, with the inner nodes related to its different points of the structure. Therefore, even if the network of Fig. 15 is translated into a Cauer one, a single stage has not a physical relationship with a part of the capacitor. In other words, apart the center, even a Cauer network will not add any more nodes to evaluate the temperature of other points of the capacitor.

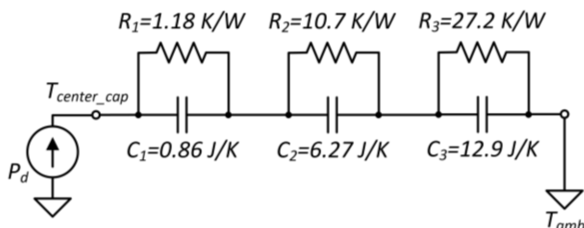

Fig. 15. Foster's network extracted for the capacitor taken as reference.

In this case, 3 stages are the result of a trade-off between network complexity and good matching with the simulated thermal impedance. As shown in Fig. 16, the maximum relative error on the thermal impedance during the power step response is around 3 %. The error has been evaluated only when the temperature increase is greater than 0.15°C, otherwise the relative error is ill-conditioned because it is defined as follows:

$$Relative\ Error = \left|\frac{Z_{th_FEM} - Z_{th_Foster}}{Z_{th_FEM}}\right| \cdot 100, \quad (3)$$

where Z_{th_FEM} and Z_{th_Foster} are the thermal impedances evaluated by the FEM simulation and by the Foster network, respectively. Each thermal impedance is evaluated as follows:

$$Z_{th}(t) = \frac{P_d(t)}{T_{center_cap}(t) - T_{amb}}, \quad (4)$$

where $P_d(t)$ is the dissipated power during the power step, and T_{amb} is the ambient temperature, kept constant during the power step response.

Taking into account the mutual influence of the power electronic devices nearby the capacitor, it can be considered a different lumped-element thermal network with multiple inputs (heat sources influencing the temperature of the point of interest) and single output (the maximum temperature of the capacitor, in this case). A way to extract this kind of network is shown in [31].

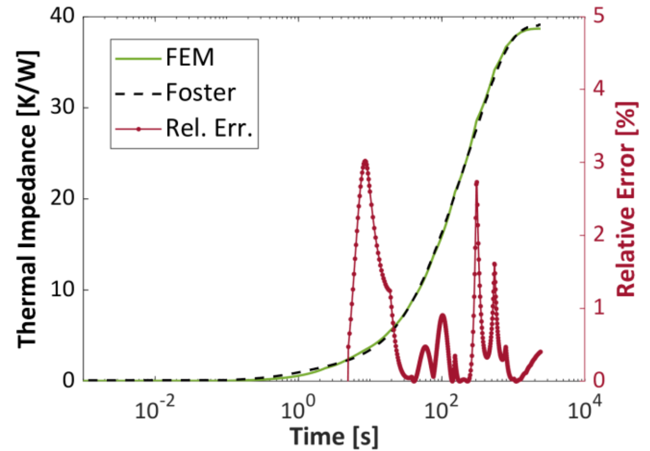

Fig. 16. Simulation results of FEM and Foster network thermal impedances between the center of the capacitor and the ambient, and the relative error between them during a power step response with $V_{AC} = 8$ V, $f = 100$ kHz.

4. Conclusions

A FEA-based method to evaluate the temperature of capacitors has been presented. A metallized polypropylene capacitor was used as case study, and the applied method has been proved to be a useful tool to obtain a thermal model to couple with electrical SPICE simulations. In this way, these simulations, also giving information on the operative temperature of capacitors embedded in the circuit under development, allow to carry out lifetime analysis of these devices and to optimize the circuit design achieving proper robustness margin and cost-effectiveness.

The method can be interesting for electronic designers, who don't know the thermal performance and properties of capacitors, and who are not aware of the failure modes and

mechanisms as manufacturers are (they know almost everything about their capacitors, but a lot of information are kept confidential).

Determining the temperature of the capacitors since the design phase is important from the circuit reliability point of view. The problem is how to calculate the temperature of capacitors when the heat generated by themselves as well as the heat from other components is not known a priori. Obviously, it's possible to wait for the results of the electrical simulations to calculate the temperature using an extracted thermal network, but the inclusion of this network in a SPICE model is convenient to perform this calculation simultaneously with the electrical simulations. Furthermore, the temperature affects the electrical parameters by changing the electrical behavior, which in turn changes the thermal behavior. If this coupling must be considered to evaluate the actual temperature with greater accuracy, it is necessary to develop models for simulations providing trustworthy results.

References

[1] S. Yang et al., "An industry-based survey of reliability in power electronic converters", IEEE Trans. Ind. Appl., vol. 47, n. 3, pp. 1441–1451, 2011.

[2] J. Watson, G. Castro, "A review of high-temperature electronics technology and applications", Journal of Materials Science: Materials in Electronics, vol. 26, pp. 9226–9235, 2015.

[3] H. Wang, F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters — An Overview", IEEE Transactions on Industry Applications, vol. 50, n. 5, pp. 3569-3578, 2014.

[4] J. M. Lenz, J. R. Pinheiro, "Mission Profile Impact on Capacitor Reliability in PV Single-Stage Inverters", Proc. 7th Int. Conf. on Renewable Energy Research and Applications, pp. 976-981, 2018.

[5] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, F. Blaabjerg, "Lifetime Estimation of DC-Link Capacitors in Adjustable Speed Drives Under Grid Voltage Unbalances", IEEE Transactions on Power Electronics, vol. 34, n. 5, pp. 4064-4078, 2019.

[6] A. Gupta, P. Yadav, D. De Voto, J. Major, "A Review of Degradation Behavior and Modeling of Capacitors", Proceedings of the ASME 2018 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems. San Francisco, California, USA. August 27–30, 2018.

[7] R. Parvari, M. Zarghani, S. Kaboli, "RCD snubber design based on reliability consideration: A case study for thermal balancing in power electronic converters", Microelectronics Reliability, vol. 88–90, pp. 1311-1315, 2018.

[8] P. Mach, M. Horak, C. Stancu, "Thermal Ageing of Polypropylene Film Capacitors", 38th International Spring Seminar on Electronics Technology: pp. 272-276, 2015.

[9] M. Makdessi, A. Sari, P. Venet, P. Bevilacqua, C. Joubert, "Accelerated Ageing of Metallized Film Capacitors under High Ripple Currents Combined with a DC Voltage", IEEE Transactions on Power Electronics, vol. 30, n. 5, pp. 2435-2444, 2015.

[10] M.H. El-Husseini, P. Venet, A. Al-Majid, M. Fathallah, G. Rojat, J.A. Ferreira, "Manufacturing technology effect on current pulse handling performance of metallized polypropylene film capacitors", Journal of Physics D: Applied Physics, vol. 36, n. 18, pp. 2295-2303, 2003.

[11] Cavallini, A., Fabiani, D., Mazzanti, G., and Montanari, G.C. "Models for Degradation of Self-healing Capacitors Operating under Voltage Distortion and Temperature", Proceedings of the 6th International Conference on Properties and Applications of Dielectric Materials: pp. 108-111. June 2000.

[12] F. Lin, X. Dai, J. Li, Z. Yao, N. Wang, "On the failure mechanism of metallized polypropylene pulse capacitors", Conference on Electrical Insulation and Dielectric Phenomena, Annual Report, vol. 2, pp. 592-595, 2000.

[13] A. Borghetti, C.A. Nucci, G. Pasini, S. Pirani, M. Rinaldi, "Tests on self-healing metallized polypropylene capacitors for power applications", IEEE Transactions on Power Delivery, vol. 10, pp. 556-561, 1995.

[14] T. W. Dakin, "Electrical Insulation Deterioration Treated as a Chemical Rate Phenomenon", Transactions of the American Institute of Electrical Engineers, vol. 67, n. 1, pp. 113-122, 1948.

[15] R. Jánó, D. Pitica, "Accelerated Ageing Tests of Aluminum Electrolytic Capacitors for Evaluating Lifetime Prediction Models", Acta Technica Napocensis - Electronics and Telecommunications, vol. 53, n. 2, pp. 36-41, 2012.

[16] R. Gallay, "Metallized Film Capacitor Lifetime Evaluation and Failure Mode Analysis", Proceedings of the CAS-CERN Accelerator School: Power Converters, pp. 45-56, 2014.

[17] L.A. Escobar, W.Q. Meeker, "A Review of Accelerated Test Models", Statistical Science, vol. 21, n. 4, pp. 552–577, 2006.

[18] S. Glasstone, K. J. Laidler, H.E. Eyring, "The Theory of Rate Processes", McGraw Hill, New York. 1941.

[19] H. Endicott, B. Hatch and R. Sohmer, "Application of the Eyring Model to Capacitor Aging Data", IEEE Transactions on Component Parts, vol. 12, n. 1, pp. 34-41, 1965.

[20] L. Simoni, "General Equation of the Decline in the Electric Strength for Combined Thermal and Electrical Stresses", IEEE Transactions on Electrical Insulation, vol. 19, n. 1, pp. 45-52, 1984.

[21] B. Hemalatha, T.S. Ramu, ''Insulation Degradation under Multifactor Stress", Fifth International Symposium on High Voltage Engineering. August 1987.

[22] G.C. Montanari, L. Simoni, "Aging Phenomenology and Modeling", IEEE Transactions on Electrical Insulation, vol. 28, n. 5, pp. 755-776, 1993.

[23] A. Albertini, M.G. Masi, G. Mazzanti, L. Peretto, R. Tinarelli, "Toward a BITE for Real-Time Life Estimation of Capacitors Subjected to Thermal Stress", IEEE Transactions on Instrumentation and Measurement, vol. 60, n. 5, pp. 1674-168, 2011.

[24] H. Gualous, R. Gallay, G. Alcicek, B. Tala-Ighil, A. Oukaour, B. Boudart, P. Makany, "Supercapacitor Ageing at Constant Temperature and Constant Voltage and Thermal Shock", Microelectronics Reliability, vol. 50, n. 9, pp. 1783–1788, 2010.

[25] S.G. Parler, "Deriving life multipliers for electrolytic capacitors", IEEE Power Electronics Society Newsletter, vol. 16, n. 1, pp.11–12, 2004.

[26] A. Dehbi, W. Wondrak, Y. Ousten, Y. Danto, "High Temperature Reliability Testing of Aluminum and Tantalum Electrolytic Capacitors", Microelectronics Reliability, vol. 42, n. 6, pp. 835-840, 2002.

[27] A. Soldati, A. Toscani, P. Cova and G. Franceschini, "Design and Control of High-Density High-Voltage Smart Converter for Food Ohmic Heating", IEEE Transactions on Industry Applications, vol. 55, n. 6, pp. 7712-7725, 2019.

[28] P. Cova, N. Delmonte, "Thermal modeling and design of power converters with tight thermal constraints", Microelectronics Reliability, vol. 52, pp. 2391-2396, 2012.

[29] B.W. Williams, "Principles and Elements of Power Electronics: Devices, Drivers, Applications, Passive Components. Glasgow", U.K.: Univ. Strathclyde, 2006, ch. 26.

[30] A. Matallana, E. Robles, E. Ibarra, J. Andreu, N. Delmonte, P. Cova, "A methodology to determine reliability issues in automotive SiC power modules combining 1D and 3D thermal simulations under driving cycle profiles", Microelectronics Reliability, vol. 102, paper n. 113500, 2019.

[31] M. Bernardoni, N. Delmonte, D. Chiozzi, P. Cova, "Non-linear thermal simulation at system level: Compact modelling and experimental validation", Microelectronics Reliability, vol. 80, pp. 223-229, 2018.