A Low-Power Sigma-Delta Modulator for Healthcare and Medical Diagnostic Applications

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***Abstract*—This paper presents a switched-capacitor Sigma-Delta modulator designed in 90-nm CMOS technology, operating at 1.2-V supply voltage. The modulator targets healthcare and medical diagnostic applications where the readout of small-bandwidth signals is required. The design of the proposed A/D converter was optimized to achieve the minimum power consumption and area. A remarkable performance improvement is obtained through the integration of a low-noise amplifier with modified Miller compensation and rail-to-rail output stage. The manuscript also presents a set of design equations, from the small-signal analysis of the amplifier, for an easy design of the modulator in different technology nodes. The Sigma-Delta converter achieves a measured 96-dB dynamic range, over a 250-Hz signal bandwidth, with an oversampling ratio of 500. The power consumption is 30 μW, with a silicon area of 0.39 mm^2.**

***Index Terms*—Analog-digital conversion, Sigma-Delta A/D converters, medical diagnostic, healthcare devices, switched-capacitor circuits, low-voltage, low-power, operational amplifiers.**

I. Introduction

In the last decade there has been an increasing interest and a growing demand of medical devices for the acquisition and processing of biopotentials, such as electroencephalogram (EEG) and electrocardiogram (ECG) signals. Electronic data acquisition systems can be used also in several other applications for the medical analysis and diagnostic context, such as the Polymerase Chain Reaction (PCR), for the identification and quantifications of viral nucleic acids, micro-organisms, and pathogens [1], [2], the photometry in clinical lab diagnostic [3], and the electrochemistry based on electrochemical cells and an electronic potentiostat for blood analysis [4], [5]. The large part of these applications would greatly benefit from portability of the devices. This requires the minimization of the power consumption of the electronic circuitry to maximize the battery lifetime. Moreover, the same low supply voltage for both analog front-end and digital back-end can be beneficial for these purposes, allowing also a drastic simplification of the power management, with a smaller silicon area [6], [7].

Analog-to-Digital Converters (ADCs) play a fundamental role in the signal acquisition systems. Indeed, they impact significantly the overall Signal-to-Noise ratio (SNR) and power consumption of the acquisition chain. A common characteristic of the above medical and diagnostic devices is the relatively small bandwidth of the signal to be digitized, within a range of few hundreds of Hz. On the other hand, the required effective resolution of the ADC depends on the specific application, which also sets the number of acquisition channels [8]–[12]. Fig. 1 shows the range of the required resolutions and the typical number of channels for the previous-mentioned applications. Additional healthcare devices, where either a gas or a fluid pressure must be sensed and digitized, have been also included. The graph highlights as ADCs with resolutions in the 14-to-16 bits range are suitable for a large number of healthcare and diagnosis applications.

Among state-of-the-art ADCs, Sigma-Delta ($\Sigma\Delta$) converters [13] exhibit the lowest power consumption for the mentioned resolution range and a signal bandwidth of a few hundred hertz [14]. Focusing the analysis on single-loop implementations, switched capacitor (SC) $\Sigma\Delta$ modulators usually outperform continuous-time implementations. Good performance has been reported for multi-bit SC modulators in the considered application domain [15], but the non-linearity of the Digital-to-Analog Converter (DAC) in the modulator loop requires the implementation of the Dynamic Element Matching (DEM) to transfer the added harmonic distortion into partially shaped noise [16]. However, DEM technique leads to in-band residual tones and to the degradation of the converter SNR [17]. Moreover, the circuit complexity and the area overhead of the DEM control circuits should be taken into account.

An interesting feature of continuous-time (CT) modulators is

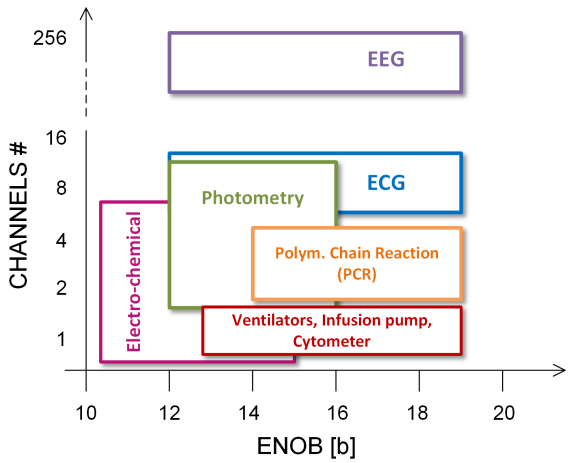

Fig. 1. Applications chart of small-bandwidth A/D converters in healthcare and medical diagnostic devices.

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the built-in low-pass filtering function. This allows the anti-aliasing filter to be removed with some simplification of the interface circuits. However, they usually exhibits a resistive input impedance, forcing the adoption of an instrumentation amplifier. To overcome this issue and achieve high input impedance, the CT-$\Sigma\Delta$ modulator proposed in [18] adopt a non-inverting integrator. However, the effective resolution (ENOB), at the maximum input gain, is lower than 13 bits and 2.5-V thick-oxide transistors are used, thus calling for an additional technology option. In photometry applications, the low input resistance of the CT modulator is exploited for the current signal source. In [19] a DR larger than 100 dB is achieved combining a front-end 1-st order CT modulator with a single-slope ADC, but a voltage supply of 3.3 V is required and the measured ENOB of the biosensing chain is lower than 11 bits. In [19] a capacitve transimpedance amplifier is merged with a 2-nd order CT modulator, achieving 86-dB DR with a 1.8-V supply.

The paper presents a 1.2-V SC-$\Sigma\Delta$ modulator featuring an effective resolution suitable for a large range of health care and medical diagnostic applications. The front-end integrator is based on a low-noise opamp with a novel implementation of the Miller-Ahuja frequency compensation enabling the near-1-V supply, with the concurrent design optimization for power consumption, voltage gain, and noise [20]. Thanks to the proposed compensation circuit, low sensitivity of the main operational amplifier parameters to both process corner and temperature is achieved in spite of the low supply voltage. A specific feature of the proposed modulator is the capability to operate over a large temperature range with a limited performance degradation. It is worth noticing that state-of-the-art $\Sigma\Delta$ ADCs for the considered application domains are seldom characterized over temperature, despite this is mandatory for electronic devices for medical and healthcare markets. Indeed, maintaining the target performance over the temperature range with a low supply voltage, a large signal range, and low power consumption raises significant design issues. Additionally, thanks to low supply sensitivity of the proposed opamp, the modulator achieves the highest power supply rejection (PSR) among the low-voltage ADC in the literature for the considered applications. This performance is of primary importance, taking into account that the converters designed for portable systems are commonly integrated into a mixed-signal chip or a System on a chip (SOC).

The modulator exhibits a conversion energy efficiency that is aligned with state-of-the-art and low-supply ADCs. This was achieved by means of the proposed low-noise opamp and through design optimization, balancing the kT/C and opamp noise to minimize the overall power consumption.

The paper also includes a mathematical model of the opamp for the design optimization based on the target specifications (i.e. gain, bandwidth, slew-rate, phase margin, and noise).

The modulator was implemented in a 90-nm technology to operate over the target temperature range, i.e. from -40°C to 80°C. It exhibits a dynamic range (DR) of 96-dB, 14.8-b ENOB, and more than 70 dB of PSR, with 30 μW of power consumption. The experimental results are aligned with the simulations and in agreement with the mathematical model.

TABLE I
MODULATOR COEFFICIENTS

Stage	Inter-stage coeff.	Feed-forward coeff.	Feed-in coeff.
1^{st} Int.	$c_1 = 0.5$	$d_1 = 0.2$	$e_1 = 0.5$
2^{nd} Int.	$c_2 = 0.0625$	$d_2 = 0.2$	-
3^{rd} Int.	$c_3 = 0.02$	$d_3 = 0.3$	-

TABLE II
MODULATOR SPECIFICATIONS

Parameters	Symbol	Value	Unit
Sampling frequency	f_{CK}	250	kHz
Signal bandwidth	f_b	250	Hz
Oversampling Ratio	OSR	500	-
Common-mode input voltage	V_{cm}	0.5	V
Full-scale (diff.)	V_{FS}	1	V
Power supply	V_{dd}	1.2	V
Reference - HIGH	$Vref_P$	1	V
Reference - LOW	$Vref_N$	0	V
Minimum Dynamic Range	*DR*	95	dB

The paper is organized as follows. The architecture of the $\Sigma\Delta$ modulator and the SC integrator is described in Section II. The low-noise opamp used in the front-end integrator is presented in Section III, whereas the complete modulator schematic and other analog blocks is discussed in Section IV. The measurement results are presented and compared with the state-of-the-art $\Sigma\Delta$ modulators in Section V.

II. MODULATOR SPECIFICATIONS AND ARCHITECTURE

The block diagram of the proposed 3-rd order $\Sigma\Delta$ modulator with a single-bit quantizer is shown in Fig. 2. A cascade of integrators with feed-forward (CIFF) topology, was preferred over the implementation with distributed feedback (CIFB) [13], considering the smaller signal swing at the output of each integrator, which makes CIFF modulators preferable with a low supply voltage. Furthermore, this topology exhibits larger inter-stage and feed-in coefficients of the first integrator, c_1 and e_1, respectively, in Fig. 2, with clear benefits in terms of silicon area and load capacitance. The values of the coefficients obtained with the Delta Sigma Toolbox [21] for the CIFF architecture, and the main specifications of the modulator in Fig. 2 are reported in Table I and in Table II, respectively.

A. SC Integrator

Each integrator in the modulator of Fig. 2 is based on an opamp with an SC feedback circuit [13]. In low-pass modulators, the low-frequency noise of the opamp may severely affect the effective resolution of the ADC. Thus, a noise cancellation technique such as the correlated-double sampling (CDS) or the chopping modulation (CHM) [22] is mandatory for the first integrator. In the proposed design CDS was preferred to CHM, which pushes the low-frequency noise outside the ADC signal bandwidth, but at the cost of added spurious content in the output spectrum. The single-ended equivalent schematic of the differential integrator is shown in Fig. 3 [23], where

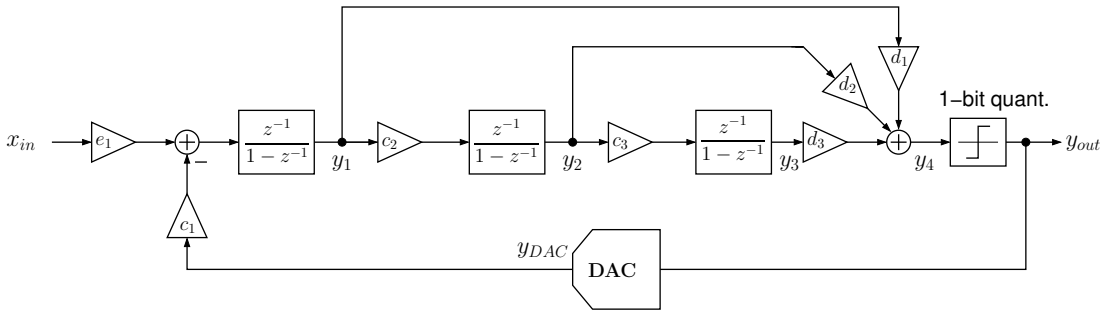

Fig. 2. Block diagram of the third-order ΣΔ modulator based on the CIFF architecture.

$V_{out-DAC}$ corresponds to the feedback signal y_{DAC} in Fig. 2. With $\phi_1 = 1$ and $\phi_2 = 0$ the input voltage V_{in} is sampled on C_{S-1}, while the offset voltage and the low-frequency noise of the opamp are sampled on C_{CDS-1}. During the integration phase, with $\phi_1 = 0$ and $\phi_2 = 1$, only the difference between V_{in} and the output of the DAC $V_{out-DAC}$ is integrated, thus, the offset voltage and the low-frequency noise voltage are removed from the integrator output.

The total harmonic distortion (THD) affecting the output signal of the modulator is caused by two sources of errors: the non-linearity of the input sampling switch, discussed in Section IV, and the settling error at the integrator output, which is mainly ascribed to the opamp limited gain, bandwidth, and slew-rate, together with the stability margin of the integrator in the integration phase [24]. Several behavioural models have been proposed to estimate the Signal-to-Noise-and-Distortion ratio (SNDR) of the modulator from the opamp specifications and the values of the capacitors [24]–[27]. Thus, they provide the design targets for the opamp in the first integrator to achieve the required effective resolution in the mentioned healthcare and diagnostic applications, at the minimum power consumption. The large signal swing at the output of the first integrator, about the 60% of the conversion range of the modulator in Fig. 2, makes challenging the opamp design. Indeed, the estimated lower limits of the voltage gain, bandwidth, and output slew-rate must be fulfilled over the output range of the integrator. For the second and third integrators in Fig. 2, the opamp specifications can be relaxed for power saving, due to the noise suppression factor provided by the modulator loop [13]. For the proposed topology, the noise transfer function (i.e. the inverse of the suppression factor) is -116 dB from the input of the second stage to the modulator input and -162 dB from the input of the third stage

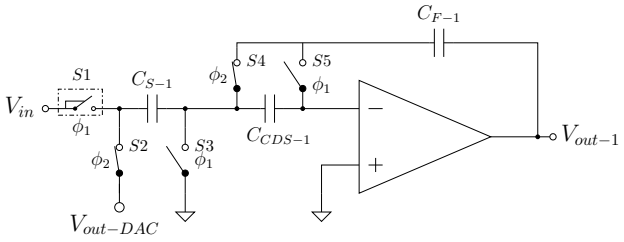

Fig. 3. Single-ended equivalent of the front-end integrator with CDS. With reference to Fig. 2, $V_{out-1} \equiv y_1$ and $V_{out-DAC} \equiv y_{DAC}$.

to the modulator input stage, compared with the -70 dB of the front-end integrator. Therefore, the modulator noise floor in the signal bandwidth is mainly set by the noise of the front-end integrator.

In the integrator circuit with CDS in Fig. 3, the input-referred noise $v_{n,int}$ is due to noise sources in the sampling ($\phi_1 = 1$) and integration ($\phi_2 = 1$) mode:

$$v^2_{n,int} \approx v^2_{n,s,sw} + v^2_{n,i,op} + v^2_{n,i,sw} + v^2_{n,cds,op} \quad (1)$$

where $v^2_{n,s,sw}$ is the contribution of switches S_1 and S_3 in sampling mode, $v^2_{n,i,sw}$ and $v^2_{n,i,op}$ are the contributions of switches S_2 and S_4, and of the opamp, respectively, in integration mode [27], [28]:

$$v^2_{n,s,sw} = d\,\frac{k\,T}{C_{S-1}} \quad (2)$$

$$v^2_{n,i,sw} = d \cdot \alpha_{i,sw}\,\frac{k\,T}{C_{S-1}} \quad (3)$$

$$v^2_{n,i,op} = N_{op}\frac{\omega_t}{4}\,k_{pk} \quad (4)$$

$$v^2_{n,cds,op} = \alpha_{cds,op} \cdot v^2_{n,i,op} \quad (5)$$

where *d* is either 1 or 2 with respectively a single-ended or a differential integrator, *k* is the Boltzmann constant, *T* is the absolute temperature, and $\alpha_{i,sw}$ depends on the on-resistance of switches S_2 and S_4 and on the opamp bandwidth in the closed-loop configuration. The contribution of the opamp noise in the integration mode is $v^2_{n,i,op}$ in (4) where N_{op} is the input-referred noise spectral density of the opamp in the flat region, and ω_t is the unity-gain frequency of the integrator loop-gain in integration mode. The coefficient k_{pk} is added to the basic noise model to take into account the effect of the in-band peaking of the input-referred noise spectrum. The input noise of the integrator in Fig. 3 is affected by CDS since the noise of switches and opamp are sampled by C_{CDS-1} and then transferred to C_{S-1} [29]. If the contribution of the switches is neglected, only the additional contribution due to the opamp noise must be added, i.e. $v^2_{n,cds,op}$ in (5), where $\alpha_{cds,op}$ depends on the C_{CDS-1}/C_{S-1} ratio. The higher this ratio, the lower $\alpha_{cds,op}$. With $C_{CDS-1} = C_{S-1}$, $\alpha_{cds,op}$ is approximated to unity [27].

The modulator design optimization for the minimum power consumption starts from the noise partitioning of the input noise, between the *kT/C* component and the opamp in the first integrator, using the equations of N_{op}, ω_t, and integrator

TABLE III
INTEGRATORS' CAPACITORS

Stage	$C_{S-<i>}$	$C_{F-<i>}$	$C_{CDS-<i>}$
1^{st} Int.	2-pF	4-pF	2-pF
2^{nd} Int.	128-fF	2-pF	-
3^{rd} Int.	128-fF	6.4-pF	-
Adder	250-fF	-	-

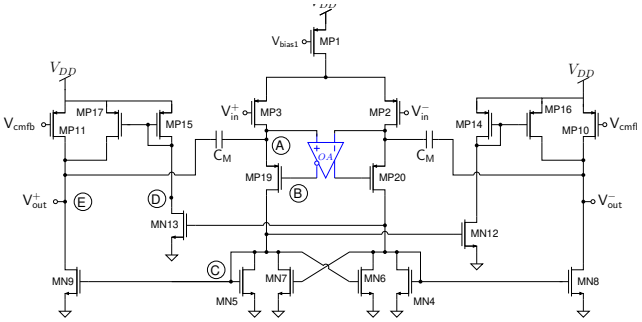

Fig. 4. Schematic of the low-noise opamp in the first integrator (SC-CMFB circuit omitted).

phase margin. It is worth to be noticed that such parameters are usually affected by the opamp non-dominant poles and zeroes if the design is optimized for minimum power. Nevertheless, some modulator models are based on an approximated first-order transfer function [24], [26], [30], even though this assumption is acceptable only for single-stage opamp's.

III. LOW-NOISE OPAMP

With behavioral simulations a minimum DC voltage gain of 50 dB for the opamp was estimated to achieve the target effective resolution. Since the 1.2-V supply makes difficult the exploitation of cascoding techniques in a single gain stage, the two-stage operational amplifier in Fig. 4 was implemented in the integrator. A local positive feedback is introduced in the input stage with *MN6* and *MN7* boosting the load resistance and thus leading to a higher voltage gain with respect to the amplifier with a simple NMOS-diode load [31]. Improved Miller-Ahuja compensation is implemented to enable concurrent optimization of power consumption, voltage gain and input noise [20]. Indeed, introducing a common-gate amplifier, embedded in the first stage (*MP19, MP20*), in the Miller feedback path allows achieving the same phase margin (PM) with a lower value of transconductance of the second stage g_{m9} [32], and without any additional power consumption. However, this enhanced Miller compensation adds a pair of complex conjugate non-dominant poles to the opamp transfer function depending on the transconductance of the common-gate stage, g_{m19} [33]. Since all the transistors are biased in the moderate-to-weak inversion for minimum power consumption, $g_{m19} \approx g_{m3}$ and, consequently, g_{m19} cannot be changed without affecting the unity-gain frequency of the opamp, which is proportional to g_{m3}. If the gate voltage of the common-gate amplifier in the Miller path is controlled through an auxiliary amplifier, OA in Fig. 4, a further degree of freedom is introduced in the design, and the stability margin of the integrator is improved since the value of the complex-conjugate poles frequency and of the dumping ratio is increased [20], [33].

Nevertheless, introducing an auxiliary amplifier with a 1.2-V supply raises relevant design issues due to the cascode configuration of the input stage, considering the process, voltage, and temperature (PVT) variation. Furthermore, the added power consumption should be a small fraction of the opamp consumption, to make the improved Miller-Ahuja compensation suitable for an ultra-low-power design.

By means of the gain-boosting amplifier in the dashed box of Fig. 5 a low sensitivity is achieved for both the opamp voltage gain and the stability margin of the integrator to the PVT variations, in spite of the near 1-V supply. This fully-differential auxiliary amplifier is based on input buffers and a PMOS differential pair, with NMOS diodes *MN23* and *MN24* setting the common-mode output voltage and providing a low output impedance. The DC differential voltage gain (A_{aux-0}) and the angular frequency of the first pole (ω_{aux}) are:

$$A_{aux-0} \approx \frac{g_{m21}}{g_{m23}} \tag{6}$$

$$\omega_{aux} \approx \frac{g_{m23}}{C_{gs23}} \tag{7}$$

where $C_{gs<i>}$ and $g_{m<i>}$ are the gate-source capacitance and the small-signal transconductance of the *i*-th MOS transistor. The proposed implementation allows satisfying the saturation condition for the involved devices despite the low supply voltage. Indeed, *MP19* is always in the saturation region if

$$V_B \geq V_C + V_{Tp} \tag{8}$$

where V_B and V_C are the voltages at nodes *B* and *C* in Fig. 5, and V_{Tp} is the threshold voltage of PMOS devices. Since $V_B \approx V_C \approx V_{Tn}$, V_{Tn} being the threshold voltage of NMOS devices, the condition in (8) is always satisfied over the process and temperature corner space, since $V_{Tp} < 0$. The saturation condition for the opamp input devices is

$$V_{in}^{+}, V_{in}^{-} \geq V_A + V_{Tp} \approx V_{Tn} \tag{9}$$

where $V_{gs23} \approx V_{Tn}$ and $V_{sg19} \approx -V_{Tp}$ have been assumed. Therefore, a suitable range for the common-mode input voltage is obtained over the PVT variations at 1.2-V supply.

Since the implemented compensation allows to scale down the

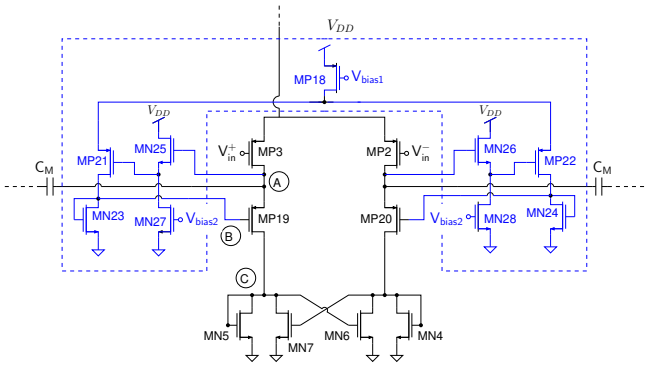

Fig. 5. Schematic of the auxiliary amplifier (blue lines in the dashed box) for the transconductance enhancement of *MP19* and *MP20*.

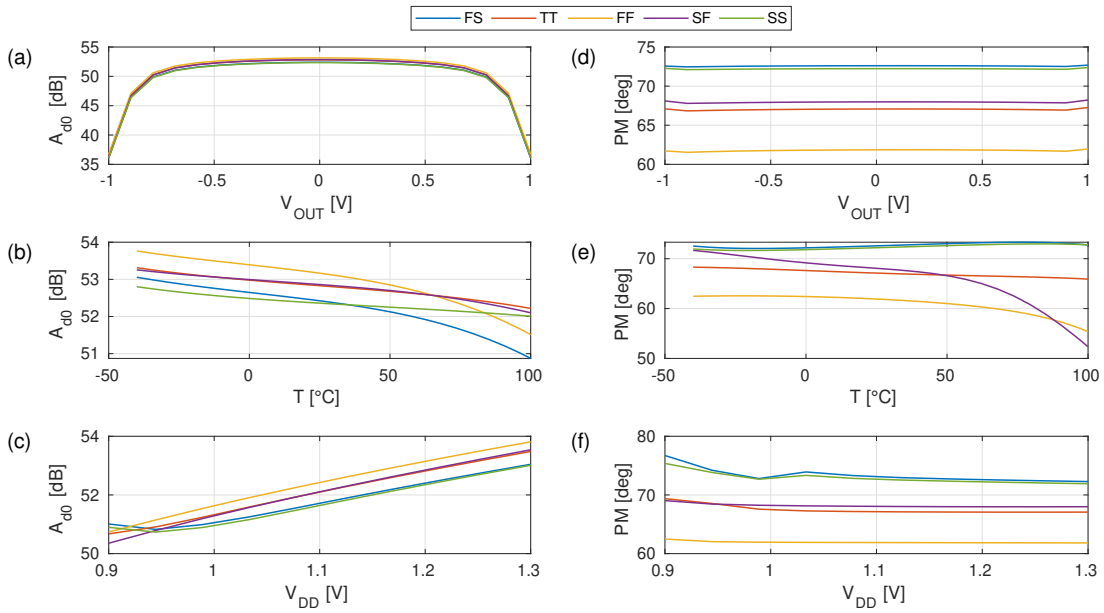

Fig. 6. From (a) to (c) and from (d) to (f): simulated opamp DC gain and phase margin (with unity feedback factor) over corners and vs. the DC output voltage, temperature, and supply voltage.

transconductance of the output devices (g_{m9}), the bias current of the output stage is reduced accordingly for power saving. Therefore, a dynamic bias (class-AB) is introduced to maintain a suitable slew-rate with a low quiescent current and, thus, to limit the settling error of the integrator [26].
The simulated DC-gain and phase margin (with unity feedback factor) over the corner space and vs. the integrator DC output voltage, temperature, and supply are shown in Fig. 6(a)-to-(f). The results confirm the expected low sensitivity of the critical opamp specs, allowing to achieve the target modulator performance over the full PVT space.

A. Small-signal and noise analysis

Assuming the 3-dB bandwidth of the auxiliary amplifier large enough not to affect the transfer function of the opamp, the small-signal equivalent circuit of the left-side of the amplifier in Fig. 4 can be simplified as in Fig. 7. The expression of each equivalent resistance and capacitance are reported in Appendix with a detailed circuit analysis. A fifth-order transfer function is obtained for the voltage gain:

$$A_d(s) \equiv \frac{v_{out}^+}{v_{in}^+} = \frac{A_{d-0} \cdot \left(a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + 1\right)}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} \tag{10}$$

The equation of the DC-gain is:

$$A_{d-0} = R_C \, R_{out} \, g_{m3} \, g_{m9} \cdot \left(1 + \frac{g_{m13} \, g_{m17}}{g_{m9} \, g_{m15}}\right) \tag{11}$$

If C_C and g_{m9} are, respectively, lower and higher than critical values C_{C-crit} and $g_{m9-crit}$, the second pole of $A_d(s)$ is real, while the third and fourth poles are complex conjugates. The case corresponding to $C_C \geq C_{C-crit}$ or $g_{m9} < g_{m9-crit}$ is not relevant because it corresponds to a small phase margin.

Approximated analytic expressions of the first, second, and third pole (p_1, p_2, and p_3) are reported in Appendix. The frequency z_1 of the dominant zero is obtained from a_1:

$$z_1 \approx -\frac{1}{a_1} \approx -\frac{g_{m9} \, g_{m15} + g_{m13} \, g_{m17}}{g_{m9} \, C_D} \tag{12}$$

Thus, considering the analytic expression of the second-pole frequency p_2 in (28), a pole-zero cancellation is obtained, if the following conditions hold:

$$g_{m9} \, R_C \quad >> \quad \frac{C_{out}}{C_M} \tag{13}$$

$$g_{m9} \, R_C \quad >> \quad 1 \tag{14}$$

This is achieved with the local feedback boosting the equivalent load resistance of the first stage (R_C). The pole-zero cancellation is a relevant benefit of this opamp architecture, leading to improved bandwidth and stability margin.
Since the second zero in the transfer function lies in the right-half plane (RHP), it should be taken into account in the stability-margin estimation. Finally, if the contributions of the high-frequency zeroes (z_3, z_4) and of the fourth pole p_4 are neglected, an approximated expression for the phase margin of the integrator in Fig. 3 is obtained:

$$PM = 90° - atan\left(\frac{2\,\delta_3 \cdot (\omega_t/|p_3|)}{1 - (\omega_t/|p_3|)^2}\right) - atan\left(\frac{\omega_t}{z_2}\right) \tag{15}$$

where $|p_3|$ and δ_3 are the complex frequency and the dumping factor of the third-pole, z_2 is the frequency of the RHP zero, and ω_t is the unity gain frequency of the integrator loop gain. Therefore, the DC gain of the auxiliary amplifier is sized from (15) to achieve the target stability margin.
The spectral power density of the input-referred voltage-noise

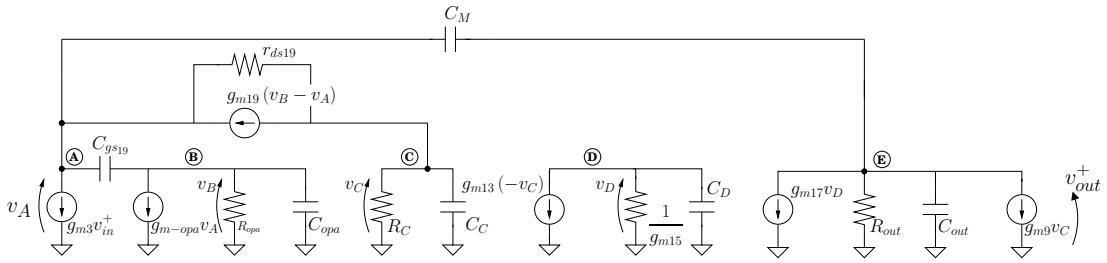

Fig. 7. Small-signal equivalent circuit of left side of the amplifier in Fig. 4.

$(v_{n,in}^2)$ of the opamp in Fig. 4 is obtained from its small-signal equivalent circuit, and depends only on the input stage:

$$v_{n,in}^2 \approx \frac{8\,k\,T\,\gamma_p}{g_{m3}} \cdot \left[1 + \frac{(g_{m_5} + g_{m_7})\,\gamma_n}{g_{m3}\,\gamma_p}\right] \tag{16}$$

where γ_n and γ_p are the gamma factors of the thermal channel noise of NMOS and PMOS devices. The flicker noise sources are not considered since their effect is removed with the CDS at the integrator-level. The contribution of the auxiliary amplifier is negligible in the integrator bandwidth, since the source nodes of *MP19* and *MP20* are connected to ground through a high equivalent impedance. A similar equation can be obtained for a 2-stages Miller-compensated opamp with a high-gain input stage [34]. Therefore, the implemented opamp achieves significant improvements in terms of bandwidth (due to pole-zero cancellation), stability margin, and power saving, without any degradation of the noise performance with respect to the basic Miller opamp.

B. Power-driven opamp design

In this section we provide an accurate model to link the opamp noise and bandwidth to the power consumption. Since the amplifier is optimized for minimum power consumption, all the devices are biased in moderate-to-weak inversion region.

The bias current of the first stage (I_{d1}) is sized on the basis of the value of $Max\left[v_{n,in}^2\right]$. From (16) with $\gamma_p \approx \gamma_n$, the following equation is obtained:

$$I_{d1} \geq \frac{n\,v_{th}}{\alpha_n} \cdot \frac{8\,k\,T\,\gamma_p}{Max\left[v_{n,in}^2\right]} \tag{17}$$

where α_n is the relative contribution of the input devices $M2$ and $M3$ to the power spectral density of the input-referred noise voltage. The Miller capacitance, C_M is sized from (50). If the slew-rate resulting from this sizing is not compatible with the maximum acceptable settling error, the current in first stage must be increased. In order to limit the noise contributions of the load devices well below $(1-\alpha_n) \cdot Max\left[v_{n,in}^2\right]$, they are sized for a higher Inversion Factor (IF) than the input transistors [35]. The following condition must be guaranteed over the PVT space to make the stability margin independent of the auxiliary amplifier:

$$\omega_{aux} \geq 10 \cdot \omega_t \tag{18}$$

From (7) and approximating the gate-source capacitance with the worst-case value corresponding to the gate-to-channel capacitance, a lower bound for the IF of *MN23* and *MN24* is found:

$$\omega_{aux} \geq \frac{IF_{23}}{0.5 + \sqrt{0.25 + IF_{23}}} \cdot \frac{3k_n' v_{th}}{L_{23}^2 C_{ox}} \geq 10\,\omega_t \tag{19}$$

The minimum bias current of *MN25* and *MN26* is obtained by setting the pole introduced by the input buffer stage at least one decade over the unity loop-gain frequency ω_t.

The equivalent capacitance C_D, introduced by *MN13*, *MN15*, and *MN17* used for the dynamic control of the output current, affects the frequency of the second pole and first zero as in (28) and (12). The step response of the amplifier is improved if the pole-zero (p_2-z_1) cancellation occurs at a frequency higher than ω_t. From (34) and (12), and assuming $g_{m9}\,R_C$ much larger than C_{out}/C_M:

$$z_1 \approx p_2 \approx \frac{g_{m17}}{C_{gs17}} \cdot \frac{g_{m9} + g_{m13}}{g_{m9}} \geq \omega_t \tag{20}$$

Therefore

$$\frac{g_{m17}}{C_{gs17}} \geq \omega_t \cdot \frac{g_{m9}}{g_{m9} + k_{AB1}\,g_{m5}} \tag{21}$$

where $k_{AB1} \equiv (W/L)_{13}\,/\,(W/L)_5$ is the current gain of the $MN4$-$MN13$ mirror. A lower bound for g_{m17}/C_{gs17} is obtained from (21), leading to a lower limit for IF_{17} (and IF_{15}). Furthermore, the lower k_{AB1}, the lower the power consumption of the control circuit at the cost of a higher g_{m17}/C_{gs17}. The condition in (21) can be fulfilled by reducing

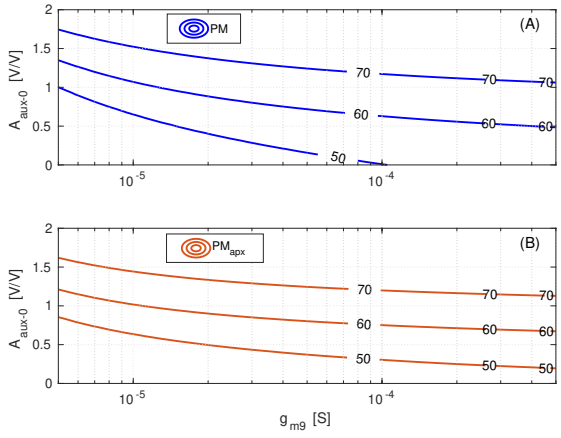

Fig. 8. Contour plot of $PM\,(A_{aux-0}, g_{m9})$ at 50°, 60°, and 70° levels. A: exact PM value from $A_d(j\omega)$; B approximated PM with equation in (15).

TABLE IV
SPECIFICATIONS OF THE LOW-NOISE OPAMP

Metric	Value	Unit
A_{d-0}	53	dB
ω_t @ H_r=1	14.1	Mrad/s
SR	1.4	V/μs
Noise	38	nV/$\sqrt{Hz}$
Load Capacitance (C'_L)	2.33	pF
Power consumption	15	μW

the length L_{17} of $MP17$ (and $MP15$), leading to a lower DC voltage gain, or by increasing the *IF* of $M17$, with a detrimental effect on the output voltage swing. The current gain of the mirror $MP17$-$MP15$ k_{AB1} must be sized to achieve a maximum drain current of $M17$ compatible with the target slew-rate (SR) limit:

$$\frac{I_{d1}\, k_{AB1}\, k_{AB2}}{C'_L} \geq SR \tag{22}$$

The DC voltage gain of the auxiliary amplifier A_{aux-0}, and the transconductance of the output stage g_{m9} are sized on the target phase margin (PM). To this aim the value of PM at different values of A_{aux-0} and g_{m9} was calculated from the transfer function $A_d(j\omega)$ in (10) and resorting to the approximation in (15). The contour plots of PM are shown in Fig. 8, where the other small-signal parameters of the circuit have been sized for the target resolution, at the minimum power consumption. The results show that a value of A_{aux-0} in the range of 1-to-2 is enough for a large stability margin and power saving in the output stage. It should be noticed that the approximation in (15) is in a good agreement with the exact value of PM (from the full transfer function) for values higher or equal to 60°. Therefore, with our circuit model, it is possible to easily size A_{aux-0} and g_{m9} for the minimum power consumption at the target PM. From (6) and the gm-over-Id dependence on IF [35], A_{aux-0} is written as:

$$A_{aux-0} = -\frac{n_p}{n_n} \cdot \frac{0.5 + \sqrt{0.25 + IF_{23}}}{0.5 + \sqrt{0.25 + IF_{21}}} \tag{23}$$

The bias current of *MN9* is sized from the target value of g_{m9}:

$$I_{d9} \geq n\, v_{th}\, g_{m9} \cdot \left(0.5 + \sqrt{0.25 + IF_9}\right) \tag{24}$$

where $IF_9 = IF_5$. The value of I_{d9} must be compatible with the minimum slew-rate limit of the opamp. Since the drain current of *MN9* is set by the *MN5*-*MN9* mirror, the transient peak value corresponds to twice the DC value:

$$I_{d9} \geq 0.5\, C'_L\, SR \tag{25}$$

The simulated specifications (typical corner) of the low-noise opamp are reported in Table IV. The size and bias (i.e. g_m/I_d) of main devices are listed in Table V.

TABLE V
DEVICE SIZE AND BIAS

device	W/L	g_m/I_d
*M*P3	9/0.9	20.9
*M*P19	9/0.45	23.0
*M*N5	2.4/3	14.4
*M*N7	1.2/3	13.3
*M*N9	4.8/3	14.3

IV. MODULATOR: CIRCUIT AND BUILDING BLOCKS

The complete modulator circuit is shown in Fig. 9, where C_A=4.1 pF, C_B=2 pF, and C_C=6.1 pF. In the second and third integrator the specifications for the amplifier can be relaxed. Therefore, the common-gate stage in the Miller feedback path is moved outside from the input stage, and no auxiliary amplifier is used. The schematic is shown in Fig. 10. This amplifier exhibits lower power consumption compared to the opamp in the front-end integrator in Fig. 4, at the cost of higher noise and worst dynamic performance. However, the noise suppression factor of the 2-nd and 3-rd integrator makes this opamp fully compatible with the target resolution of the modulator.

The signal-sampling switch in the first integrator may have a relevant impact on the overall harmonic distortion of the modulator. Considering that the swing of the input signal is about 80% of the supply voltage, a CMOS transmission gate cannot be used in the front-end. Hence, bootstrapped switches with thin-oxide transistors are included in this design [36]. The switch exhibits a simulated THD lower than -100-dB over the PVT variations, with back-annotated layout parasitics, up to the maximum signal amplitude.

The single-bit quantizer is implemented with a dynamic latch comparator, shown in Fig. 11. With *RST* at low level, the latch is in reset mode with the outputs, $Vout_P$ and $Vout_N$, at the supply voltage (V_{DD}). When *RST* goes high, the latch is in regeneration/hold mode.

V. MEASUREMENT RESULTS

The proposed third-order modulator was implemented in STM 90-nm digital CMOS technology, with the Metal-Insulator-Metal (MIM) capacitor as the only technology option. The chip photograph is shown in Fig. 12, where the bootstrapped switch (B_{SW}), the integrators, and the quantizer are highlighted. The silicon area is 0.39-mm^2, including the clock tree. The silicon samples are packaged in a Quad Flat Package (QFP) with an exposed back pad, internally connected to the chip ground by multiple down-bonds. Fig. 13 shows the FFT spectrum of the output bitstream with an input sine-wave of 35-Hz frequency and amplitude of -0.91 dBFs, i.e. normalized to the modulator full-scale. The second harmonic at -105 dBFs is due to a layout imperfection, causing a mismatch between the positive and the negative signal path. After a layout fix, this harmonic is pushed below -120 dBFs as shown by post-layout simulations with back annotated parasitics. In the same output spectrum starting from 30 mHz, the 1/f noise contribution is negligible, as a result of the low-frequency noise cancellation in the first integrator. The plot in Fig. 14 shows the modulator SNR and SNDR versus the

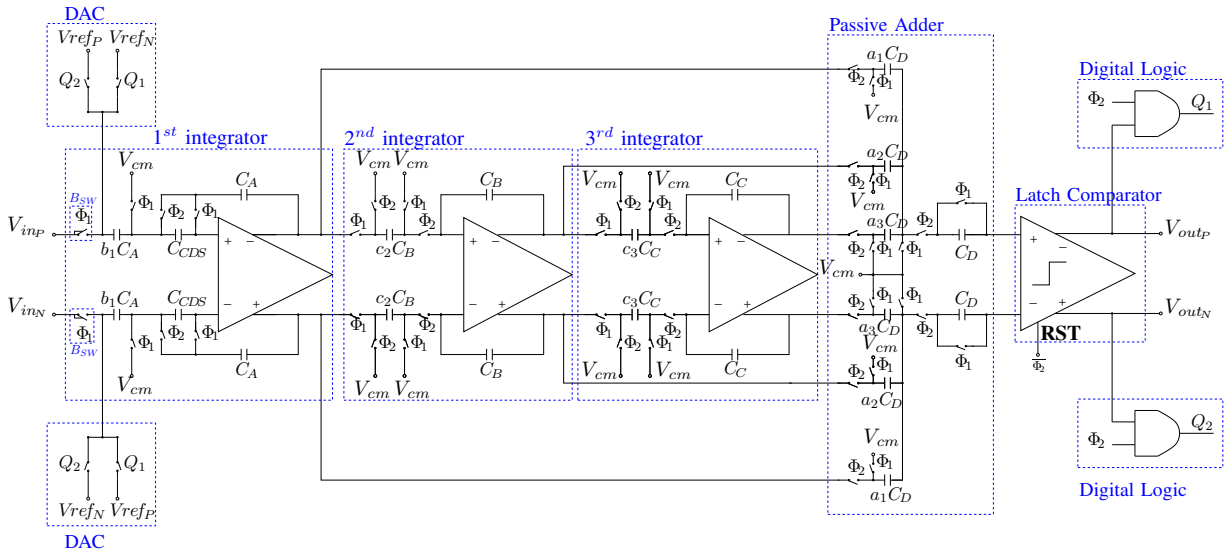

Fig. 9. Full schematic of the ΣΔ modulator.

normalized input signal amplitude, with a peak-SNR of 93 dB. The proposed converter was measured over the target temperature range with an ACS climatic chamber, featuring a temperature stability within ±0.5°C. From the measured dynamic range (DR) vs. the temperature in the plot of Fig 15, a sensitivity of -8.4 mdB/°C is estimated over the -40°C to +80°C range. This performance slightly degrades for temperatures above the considered range. In Fig. 16 the modulator SNR at the extreme temperatures is plotted vs. the input signal amplitude. The performance achieved at 90°C confirms the smooth degradation of the noise performance beyond the maximum specified temperature. The supply rejection of the modulator was measured with a 35-Hz, 100-mV sine-wave signal superimposed to the 1.2-V supply. As shown in the output spectrum in Fig. 17(a), a 76-dB PSR was achieved. The output spectrum in Fig. 17(b) was obtained with a common-mode input signal of 100-mV amplitude and with the modulator inputs shorted. The fundamental tone at -77 dBFs corresponds to a common-mode rejection (CMR) of 57 dB. A summary of the measured performance is reported in Table VI. The proposed design was compared to the state-of-the-art SC and CT modulators suitable for the healthcare and medical diagnostic applications in the chart of Fig. 1. To this aim, low-pass modulators with input bandwidth within 1 kHz and effective resolution higher than 10 bits was considered [52]. The Schreier Figure of Merit (FOM) was used for this

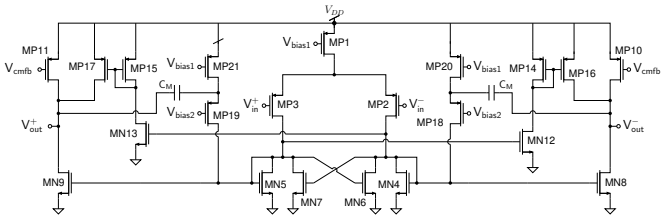

Fig. 10. Schematic of the class AB opamp for the 2nd and 3rd integrator.

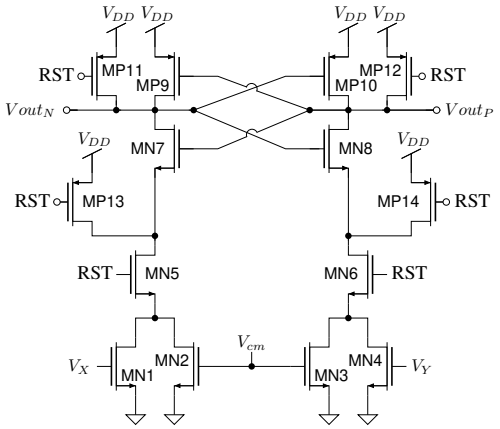

Fig. 11. Schematic of the latch comparator.

comparison [13]:

$$FOM \equiv DR + 10 \cdot log_{10}\left(\frac{BW}{Pw}\right)\ [dB] \qquad (26)$$

where *BW* and *Pw* are the input bandwidth (in Hz) and the power consumption (in W) of the modulator. The result of the comparison is shown in Fig. 18, where **SC_SB** and

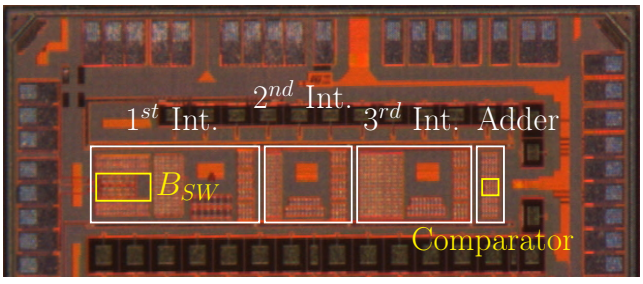

Fig. 12. Chip photograph, with main modulator blocks in white boxes. Bootstrapped switches of the first integrator, and comparator in yellow boxes.

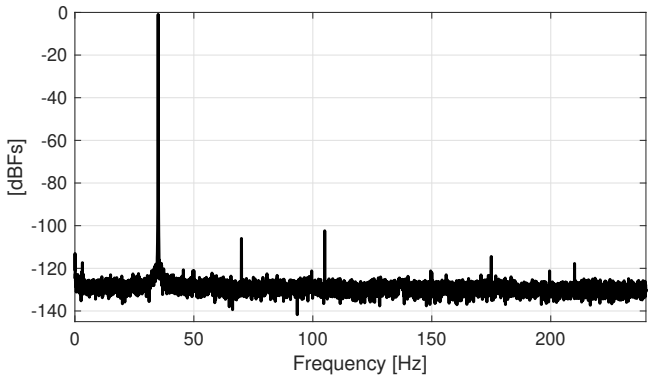

Fig. 13. Measured output spectrum with a 35-Hz sinusoidal input. The measured frequency is limited to the input bandwidth.

TABLE VI
MEASURED PERFORMANCE SUMMARY

Input bandwidth (BW)	250-Hz
Supply voltage	1.2-V
Power consumption	30-μW
Peak SNR	93-dB
Peak SNDR	91-dB
Peak SFDR	100.5-dB
DR	95.6-dB
DR sensitivity	-8.4 mdB/°C
THD	-101-dB
PSR	76-dB
TEMP	[-40°,+80°]

SC_MB correspond to switched-capacitor modulator with single-bit and multi-bit quantizer, respectively, **CT_SB** and **CT_MB** to continuous-time single-bit and multi-bit modulators, and **CT_SB_ZADC** to CT modulators with zoom-adc [42]. Among the modulators with a resolution higher than 12.5 b and a supply voltage lower than 1.8 V, the proposed modulator exhibits one of the highest FOM and it is overcome only by the multi-bit SC design in [15], which, however, requires a pair of supply voltages (i.e. 1 and 1.2 V), with increased complexity and area for the power management circuits. Compared with our previous 3-rd order CIFF architecture in [27], where the opamp in the first integrator is compensated with the basic Miller configuration, the proposed implementation, integrating a low-voltage Miller-Ahuja

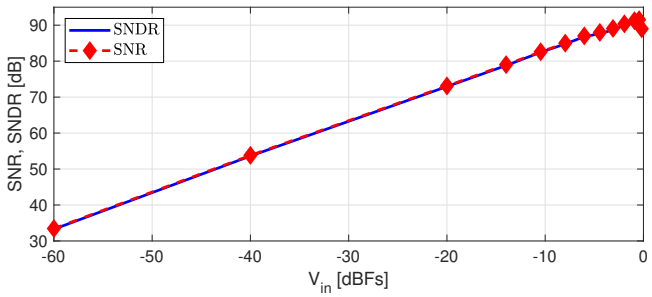

Fig. 14. Measured SNR and SNDR vs. input amplitude.

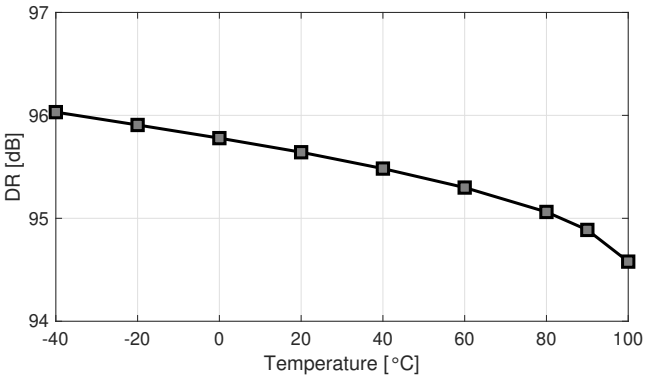

Fig. 15. Measured DR over the -40°C-to-100°C temperature range.

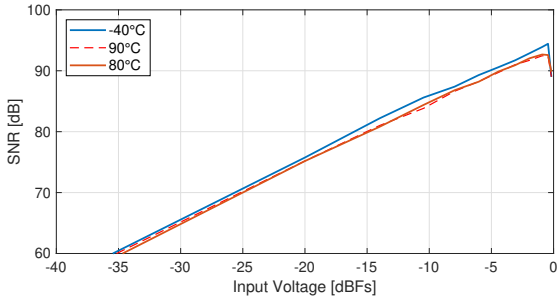

Fig. 16. Measured SNR vs. input amplitude at -40°C, 80°C, and 90°C.

compensation, achieves lower power consumption and hence higher FOM. The significant FOM result was achieved thanks to the low-noise opamp in the first integrator and the global design optimization for the minimum power consumption. The details of some silicon-proven modulators considered for the comparison are reported in Table VII. It should be noticed that the proposed design exhibits the highest PSR among the modulators with a sub-1.8-V supply. Restricting the survey to the low-voltage modulators with more than 12-b resolution, only the design reported in [15] outperforms our implementation in terms of current consumption, but with a larger silicon area and at the cost of two distinct supply voltages. It is worth noticing that the proposed modulator was

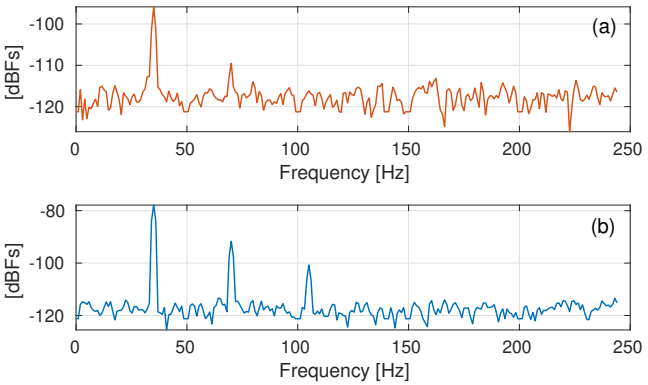

Fig. 17. Measured output spectrum with: (a) a 35-Hz, -20-dBFs signal superimposed to the supply, (b) a 35-Hz, -20-dBFs common mode input signal. Modulator inputs are shorted in both cases.

TABLE VII
COMPARISON TO STATE OF THE ART

Ref.	BW [Hz]	ENOB [b]	Cons. [μA]	Supply [V]	Techn. [nm]	DR [dB]	S. FOM [dB]	Arch.	Area [mm^2]	PSR [dB]
[18]	150	12.2[a]	20.8	1	65[b]	99.3	167.8	CT_SB	0.225	N.D.
[15]	256	16.2	8.6	1.2/1	180	99.9	174.6	DT-MB	0.59	N.D.
This work	250	14.8	25	1.2	90	95.6	164.8	DT-SB	0.39	76
[39]	256	11.7	9.5	1.4	180	83	155.8	CT-SB	0.51	N.D.
[41]	120	10.5	0.5	1.5	350	75.0	160.0	DT-SB	0.35	32
[46]	150	15	800[c]	1.8	130	112.0	162.2	DT-SB	0.4[d]	N.D.
[43]	250	12.7	12.8	1.8	180	90	153.1	CT-SB	0.088	92
[44]	45	14.7	23	2.6	350	98	156.8	DT-MB	0.7	N.D.
[19]	11	10.2	28	3.3	180	104	154.7	CT_MB	0.475[e]	N.D
[50]	400	19.6	280	5	600	122	166	DT-SB	2	N.D
[47]	400	19	540[f]	5	2000	116.1	168.7	DT-MB	4	N.D.
[48]	10	16.7	240	5	700	121	160.2	CT-MB	N.D.	N.D.
[45]	100	16.4	101	5	180	110.1	163.1	DT-SB	0.8	80
[40]	100	12.8	400	5	700	82	129	CT-SB	3.3	120

[a] At the conditions for maximum DR (i.e. maximum input gain).
[b] With 2.5-V thick-oxide transistors option.
[c] Including decimation filter.
[d] Including anti-aliasing and decimation filter.
[e] Including optical sensor.

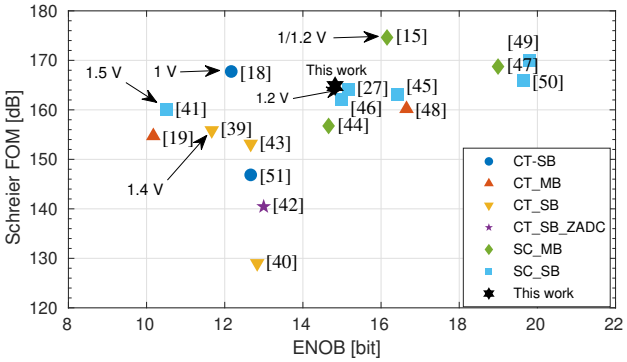

Fig. 18. Comparison of single-loop and low-pass $\Sigma\Delta$ modulators with input bandwidth lower than 1-kHz and resolution higher than 10-b. The modulator supply voltage is reported if lower than 1.6 V.

characterized over a large temperature range, with limited DR degradation at the highest temperature. The graph of Fig. 19 reports the silicon area vs peak-SNDR performance of the low-pass $\Sigma\Delta$ modulators presented at the IEEE ISSCC and VLSI conferences in the 2000-2020 period. The proposed modulator is close to the state-of-the-art frontier thanks to the area minimization guaranteed by the low-noise opamp, which allows to reduce the value of the sampling capacitor. Moreover, the single-bit architecture does not require the additional circuit for DEM, which is mandatory with a multi-bit quantizer.

VI. CONCLUSION

A third-order $\Sigma\Delta$ modulator in 90-nm CMOS for the digitization of low-frequency signals was presented. A dedicated opamp was designed with local positive feedback and enhanced Miller compensation, through a common-gate stage, with fully-differential gain boosting. A mathematical model of the opamp was presented, enabling a power-driven optimization of the amplifier and of the full modulator. Despite the low supply voltage, combined with a large input signal range, and the Miller compensation through a gain stage, the opamp exhibits low sensitivity to temperature and process variations. The modulator achieves the highest Figure of Merit among the state of the art $\Sigma\Delta$ ADCs featuring more than 12.5-b effective resolution and a single sub-1.8-V supply. The silicon area is aligned with the state-of-the-art frontier. Furthermore, thanks to the proposed opamp architecture, the modulator exhibits the highest supply rejection compared to the low-voltage and small-bandwidth implementations in literature. The achieved performance makes the proposed modulator suitable for portable medical healthcare and diagnostic devices with multiple acquisition channels.

APPENDIX A
DETAILED CIRCUIT ANALYSIS OF THE LOW-NOISE OPAMP

The small-signal equivalent circuit of the left-side of the low-noise amplifier with improved Miller-Ahuja compensation

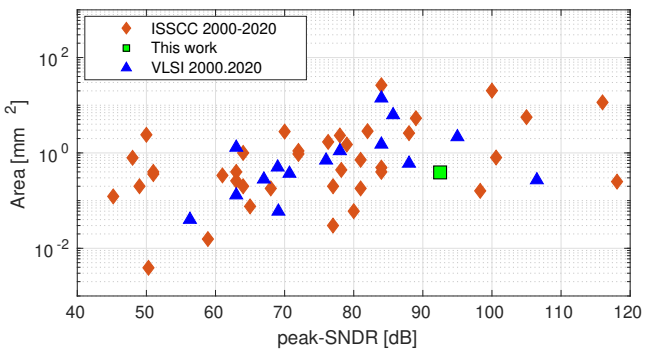

Fig. 19. Silicon area vs. peak-SNDR of SC-$\Sigma\Delta$ modulators published in the 2000-2020 period, from [53].

$$p_1 \approx -\frac{1}{R_{out}\,C_M \cdot \left[1 + g_{m9}\,R_C \cdot \left(1 + \frac{g_{m13}\,g_{m17}}{g_{m9}\,g_{m15}}\right) + \frac{C_{out}}{C_M \cdot (1 + A_{aux-0})}\right]} \tag{27}$$

$$p_2 \approx \frac{g_{m15} \cdot \left[(1 + A_{aux-0}) \cdot \left(1 + g_{m9}\,R_C + R_C \frac{g_{m13}\,g_{m17}}{g_{m15}}\right) + \frac{C_{out}}{C_M}\right]}{C_D \cdot \left[(1 + A_{aux-0}) \cdot (1 + g_{m9}\,R_C) + \frac{C_{out}}{C_M}\right]} \tag{28}$$

$$|p_3| \approx \sqrt{\frac{g_{m9}\,g_{m19} \cdot (1 + A_{aux-0})}{C_C\,C_{out}}} \tag{29}$$

$$\delta_3 \approx |p_3| \cdot \frac{\omega_{aux} \cdot \left[R_C\,C_C \cdot (1 + A_{aux-0}) \cdot \left(1 + \frac{C_{out}}{C_M}\right) + \frac{C_{out}}{g_{m19}} \cdot \left(1 + g_{m15}\,R_C\,\frac{C_C}{C_D}\right)\right] + g_{m9} R_C}{2 \cdot \omega_{aux} \cdot (1 + A_{aux-0}) \cdot (1 + g_{m9}\,R_C)} \tag{30}$$

$$z_2 \approx \frac{g_{m19} r_{ds19} \cdot \left[R_C C_D g_{m9} \cdot (1 + A_{aux-0}) - C_M \frac{g_{m15}}{g_{m19}}\right]}{C_M \cdot [C_D \cdot (R_C + r_{ds19}) + C_C R_C g_{m15} r_{ds19}] - \frac{C_D R_C g_{m9} g_{m19} r_{ds19}}{\omega_{aux}}} \tag{31}$$

is shown in Fig. 4. Only the equivalent capacitance to ground has been considered for nodes *C*, *D*, *E*, whereas the effect of the drain-source resistance of *MP3* has been neglected. The approximated equations of each equivalent capacitance and resistance in the circuit are:

$$R_C \approx \frac{1}{g_{m5} - g_{m7}} \tag{32}$$

$$C_C \approx C_{gs5} + C_{gs6} + C_{gs9} + C_{gs12} \tag{33}$$

$$C_D \approx C_{gs15} + C_{gs17} = C_{gs15} \cdot (1 + k_{AB2}) \tag{34}$$

$$R_{out} \approx r_{ds9} \parallel r_{ds11} \parallel r_{ds17} \tag{35}$$

$$C_{out} \approx C'_L \tag{36}$$

where $r_{ds<i>}$ is the drain-source resistance of the *i*-th device, k_{AB2} is the current gain of *MP15-MP17* mirror, i.e. $k_{AB2} \equiv (W/L)_{MP17} / (W/L)_{MP15}$, and C'_L is the effective load capacitance of the opamp in the integrator of Fig. 3, corresponding to the series of the feedback and sampling capacitor (i.e. C_{F-1} and C_{S-1}) combined with the input capacitance of the adder and the SC-CMFB circuit.

Under the assumption of well-separated poles, the angular frequency of each pole is approximated with the coefficients of the denominator of the fifth-order transfer function in (10).

$$p_1 = -1/b_1 \tag{37}$$

$$p_2 \approx -b_1/b_2 \tag{38}$$

$$|p_3| \approx \sqrt{b_2/b_4} \tag{39}$$

$$\delta_3 \equiv \frac{-\Re\,(p_3)}{|p_3|} \approx \frac{p_1 p_2 |p_3| b_3}{2} \tag{40}$$

From these equations, approximate expressions are obtained for p_1, p_2, $|p_3|$, and δ_3, as reported in (27), (28), (29), and (30), under the following assumptions:

$$g_{m19}\,r_{ds19} >> 1 \tag{41}$$

$$g_{m9}\,R_{out} >> 1 \tag{42}$$

$$g_{m19}\,r_{ds19} > g_{m9}\,R_{out} \tag{43}$$

$$g_{m13} \approx g_{m15} << g_{m9} \tag{44}$$

$$g_{m13} \approx g_{m15} << g_{m19} \tag{45}$$

$$C_{out} > C_M \tag{46}$$

$$C_M >> C_C, C_D \tag{47}$$

$$\omega_{aux} >> \frac{g_{m3}}{C_M} \tag{48}$$

The value of C_{C-crit} is estimated by solving the following equation:

$$\delta_3(C_C = C_{C-crit}) = 1 \tag{49}$$

Under the assumption of $z_1 << z_2 << |z_3|$, a similar approximation as in (38) can be used for z_2, i.e. $z_2 \approx -a_1/a_2$, leading to (31).

The analytic expression of the unity-gain angular frequency of the integrator is obtained from (27) and considering that $g_{m9}\,R_C >> 1$, due to the local feedback in the first amplifier stage:

$$\omega_t = \beta\,A_{d-0}\,|p_1| \approx \beta \cdot \frac{g_{m3}}{C_M} \tag{50}$$

where $\beta \equiv C_{F-1} / (C_{S-1} + C_{F-1})$ is the feedback factor in the integration phase.

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