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# A low-power native NMOS-based bandgap reference operating from -55°C to 125°C with Li-Ion battery compatibility

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**Abstract**

The paper describes the implementation of a bandgap reference based on native-MOSFET transistors for low-power sensor node applications. The circuit can operate from -55°C to 125°C and with a supply voltage ranging from 1.5 V to 4.2 V. Therefore, it is compatible with the temperature range of automotive and military-aerospace applications, and for direct Li-Ion battery attach. Moreover, the circuit can operate without any dedicated start-up circuit, thanks to its inherent single operating point. A mathematical model of the reference circuit is presented, allowing simple portability across technology nodes, with current consumption and silicon area as design parameters.

Implemented in a 55-nm CMOS technology, the voltage reference achieves a measured average (maximum) temperature coefficient of 28 ppm/°C (43 ppm/°C) and a measured sample-to-sample variation within 57 mV, with a current consumption of 420 nA at 27°C.

**KEYWORDS:**
Bandgap Circuit, CMOS, Low-Power, Native Transistors, Wireless Sensor Node, Large Temperature Range.

## 1 | INTRODUCTION

Voltage reference circuits featuring small sensitivities to temperature, supply voltage, and process corner are fundamental blocks in several analog and mixed-signal integrated systems. Indeed, an accurate voltage reference is required to generate a regulated power supply with a linear or a switched voltage regulator or to set the full-scale reference of Analog-to-Digital and Digital-to-Analog converters [1,2]. In ultra-low-power systems, such as wireless sensor nodes (WSNs), autonomous circuits with energy harvesting capability [3,4], and battery-powered devices, a relevant fraction of the current consumption in stand-by mode is ascribed to the voltage reference circuit. In the last decade, there has been a major research effort to expand the application field of WSNs in harsh environments like the automotive, the industrial and the military-aerospace ones. A well known automotive wireless sensor is the tire pressure monitoring system (TPMS) [5,6], which is powered by a mechanical energy harvester. Other automotive sensors, powered by different energy harvesting (EH) techniques, have been proposed in literature [7]. Furthermore, WSNs have been introduced for leakage detection in oil or gas pipelines [8], and for monitoring the temperature and the humidity of the storage sites of missile equipment [9]. It is worth to notice that in all these WSN implementations the system is required to operate over a large temperature range (TR) extended between -55°C and 125°C.

Wireless sensors must be designed for minimum power consumption, since both tiny batteries and energy harvesters can deliver

a very limited amount of energy, and to limit the cost of the periodical battery replacement. Therefore, bandgap circuits featuring a large TR, a low power consumption, and an adequate temperature coefficient (TC) are required to expand the applicability of the WSNs in the mentioned fields.

A reference voltage circuit achieves a low TC by combining two voltages being, respectively, proportional (PTAT) and complementary (CTAT) to the absolute temperature (T). In bipolar junction transistor (BJT) bandgap references, both the PTAT and CTAT voltages are generated by means of p-n junctions [10,11], whereas in hybrid bandgaps the PTAT voltage is generated by MOS devices, possibly combined with resistors [12,13,14]. Instead, in a MOS reference, both CTAT and PTAT voltages are generated by MOS transistors [15,16].

In the last decades, several design techniques have been investigated to reduce the minimum supply voltage of the bandgap circuit. Moreover, in Internet-of-things (IoT) applications the use of advanced process nodes is getting common to achieve both power saving and a smaller area of the digital core. However, the breakdown voltage of the thick-oxide devices in the sub-100-nm nodes is usually between 3.3 V and 1.8 V, with relevant design issues to extend the voltage supply up to 4.2 V. Indeed, this voltage would allow the bandgap reference to be directly attached to a Li-Ion battery, as often required in the power management units (PMU).

Remarkable research activity has been also carried out to push the power consumption of voltage references in the hundreds of pW range [15,12,17], by exploiting the leakage current of a MOS device to bias the circuit [15,16,18,14,19]. However, these architectures exhibit small operative TRs due to the high variability of the bias current, which becomes too small to mantain target performance at low temperatures.

In a bandgap reference, the presence of an additional operating point, usually corresponding to the zero-bias condition, requires a dedicated start-up circuit (SUPC), which, at the power-on, pushes the circuit bias far from the undesired operating condition [20,21]. The most common SUPC implementations belong to three main categories. In the first category (type-1 SUPC) a start-up device, either an NMOS [22] or a PMOS transistor [23], injects current in specific nodes of the bandgap core at the power-on. This device is driven by an inverter gate having its input controlled either by the output reference voltage or by the CTAT voltage. This inverter stops the current injection when the circuit is far from the wrong bias point, and it is usually implemented either with a PMOS load with the gate shorted to ground [22] or as a CMOS gate [24,23,25,26]. In type-2 SUPCs, a start-up current is derived from the supply voltage and injected in the bandgap core. A feedback loop is introduced to switch-off the current injection [27]. In type-3 SUPCs, the inverter is replaced by a POR generator, based on a current generator mirroring the bias current of the bandgap core [28]. It is worth noticing that SUPCs of the first type exhibit a significant dependence of the inverter threshold with the supply voltage, whereas in type-2 SUPCs the start-up current increases with the supply voltage.

Therefore, in the majority of the SUPCs, two main issues stand: proper start-up operations at low voltage supplies and proper deactivation of the SUPCs at high voltage supplies. Achieving both features can be very challenging if the application requires a wide supply range.

Moreover, if the supply voltage exceeds the gate-source voltage limit of the MOS devices a major issue occurs at the power-on when some transistors in the bandgap core may undergo significant over-voltage stress, leading to drift of the reference voltage. This situation is common to many SUPCs with some internal nodes forced, at the power-on, to a voltage close either to the supply or to ground. Summarizing, start-up free bandgap circuits, featuring a single operating point, are preferred when the target application requires a wide temperature range, a large supply voltage range, and a sub-microampere current consumption.

This paper presents a hybrid voltage reference, based on native NMOS (N-NMOS) transistors in 55-nm CMOS. N-NMOS devices exhibit a negative threshold voltage and are generally available in modern silicon technologies [16,29,30]. The proposed voltage reference operates on a TR of 180°C, a supply range from 1.5 V to 4.2 V, with a current consumption in the hundreds-nanoamperes range. A typical TC of 28 ppm/°C was measured. To the best of authors' knowledge, this is the first bandgap reference that is fully compliant with the military-aerospace temperature range, with a current consumption lower than 500 nA. The circuit is biased with a PTAT current, which is strongly desensitized to the MOS process tolerance. In addition, the proposed reference circuit exhibits a single bias point, thus eliminating the need for a SUPC and enabling wide operating ranges for both supply voltage (up to 4.2 V) and temperature. Finally, this paper proposes a simple mathematical model that allows the design optimization for power consumption, noise, and silicon area. The lack of simple design equations enabling easy portability across technology nodes is a further limitation of some leakage-based reference generators [18,31].

The paper is organized as follows. In Section 2.1 the fundamental equations of the proposed bandgap are discussed, whereas the absence of additional bias points is demonstrated in Section 2.2 and the curvature affecting the output voltage is analyzed in Section 2.3. In Section 2.4 the complete circuit diagram of the proposed bandgap is presented, and in Section 2.5 the noise

model of the circuit is discussed. The measurement results on the silicon samples in 55-nm technology and a comparison with the state-of-the-art bandgap circuits are reported in Section 3.

## 2 | NATIVE NMOS-BASED BANDGAP ARCHITECTURE

The circuit diagram of the basic Native-NMOS based bandgap (NBB) is shown in Figure 1. Here, two matched N-NMOS devices with the same aspect ratio W/L, i.e. $M_1$ and $M_2$, have their gates shorted to ground. The drain currents $I_{N1}$ and $I_{N2}$ depend on the aspect ratio of $M_1$ and on the value of resistors $R_A$ and $R_B$. By means of the current mirror made by enhanced-type PMOS $M_3$ and $M_4$, the difference between $I_{N1}$, multiplied by the mirror gain, and $I_{N2}$ is routed to the branch with a polysilicon resistor, $R_G$, and a substrate pnp BJT, $Q_1$, connected in series. If $M_1$ and $M_2$ are biased in the weak-inversion (W.I.) region, $I_{BG}$ exhibits an approximate PTAT behavior. Therefore, the sensitivity of $V_{BG}$ to $T$ is canceled at a reference temperature, $T_0$, by proper sizing of $R_G$.

### 2.1 | Circuit Analysis

An analytic expression of $I_{BG}$ is obtained starting from the voltage balance equation of the loop involving the gate-source terminals of $M_1$ and $M_2$, together with resistors $R_A$ and $R_B$:

$$\Delta V_{GS} \equiv V_{GS2} - V_{GS1} = I_{N1} R_A - I_{N2} R_B \tag{1}$$

where $V_{GS<i>}$ is the gate-source voltage of $M_{<i>}$. If $M_1$ and $M_2$ are biased in W.I., the approximate expression of the drain current is[32]:

$$I_{N<i>} = I_{SS} \cdot \left(\frac{W}{L}\right)_{<i>} \cdot e^{\frac{V_{GS<i>} - V_{TN}}{n_n \cdot v_{th}}} \cdot \left(1 - e^{-\frac{V_{DS<i>}}{v_{th}}}\right) \tag{2}$$

where $V_{DS<i>}$ and $(W/L)_{<i>}$ are the drain-source voltage and the aspect ratio of $M_{<i>}$, respectively, $v_{th}$ is the thermal voltage, i.e. $v_{th} = kT/q$, with $q$ and $k$ corresponding to the electron charge and the Boltzmann constant respectively, $V_{TN}$ and $n_n$ are the threshold voltage and the slope factor, and $I_{SS}$ is the saturation current with $W/L$=1. Limiting the analysis to the case with $V_{DS1} \gg v_{th}$, $\Delta V_{GS}$ exhibits the following dependence on the temperature:

$$\Delta V_{GS} \equiv V_{GS2} - V_{GS1} = n_n \, v_{th} \, \ln\left(\frac{I_{N2}}{I_{N1}}\right) \tag{3}$$

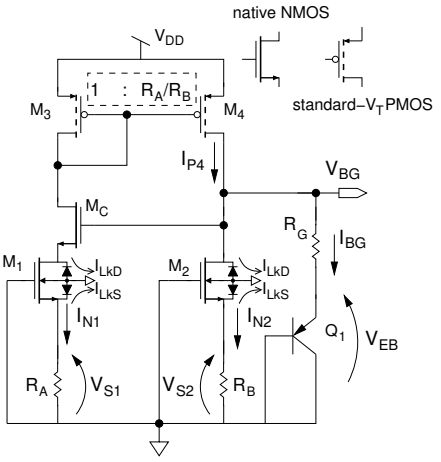


**FIGURE 1** Schematic of the NBB voltage reference.

whereas, from (1), a relationship between the drain currents and the values of $R_A$ and $R_B$ is obtained:

$$\frac{I_{N2}}{I_{N1}} = N \cdot \left(1 - \delta_V\right) \tag{4}$$

where

$$N \equiv \frac{R_A}{R_B} \quad \text{and} \quad \delta_V \equiv \frac{\Delta V_{GS}}{V_{S1}} \tag{5}$$

Therefore, (3), is rewritten as:

$$\begin{aligned} \Delta V_{GS} &= n_n \, v_{th} \, ln \left[N \cdot \left(1 - \delta_V\right)\right] \\ &\approx n_n \cdot v_{th} \, \left[\ln\left(N\right) - \delta_V\right] \end{aligned} \tag{6}$$

where $\delta_V$ is temperature-dependent, as will be discussed in Section 2.3. From (3) and (4) the following equations are written to obtain an analytic expression for $I_{BG}$:

$$I_{N1} = \frac{I_{N2} R_B + \Delta V_{GS}}{R_A} \tag{7}$$

$$I_{P4} = N \, I_{N1} \tag{8}$$

$$I_{BG} = I_{P4} - I_{N2} \tag{9}$$

Thus, replacing $\Delta V_{GS}$ in (7) with (6), the following expression is obtained from (9):

$$I_{BG} \approx \frac{N \, n_n \, v_{th}}{R_A} \cdot \left[\ln\left(N\right) - \delta_V\right] \tag{10}$$

Therefore, $I_{BG}$ is PTAT, if the circuit is sized for $\delta_V \ll \ln(N)$. From (3), (4), and (5) this condition is rewritten as:

$$V_{S1} >> n_n \, v_{th} \tag{11}$$

Hence, the PTAT dependence of $I_{BG}$ requires a negative $V_{GS}$ for $M_1$ (and $M_2$). Therefore, MOS devices with a negative threshold voltage are mandatory to avoid the deep sub-threshold bias, where the simulation models are inaccurate, the current is extremely low, and, consequently, the channel noise is very high. The output voltage $V_{BG}$ is the superposition of the PTAT voltage across $R_G$ and the base-to-emitter voltage of $Q_1$, $V_{EB}$, which is CTAT.

$$V_{BG} = V_{EB} + \frac{N \, n_n \, v_{th} \, R_G}{R_A} \cdot \left[\ln\left(N\right) - \delta_V\right] \tag{12}$$

The value of $R_G$ leading to a zero-TC of $V_{BG}$ at $T_0$ is obtained by derivation vs. temperature of (12):

$$R_G \approx - \left(\frac{\partial V_{EB}}{\partial T}\right)_{T_0} \cdot \frac{q \, R_A}{N \, n_n \, k \, \ln\left(N\right)} \tag{13}$$

where $\delta_V$ has been neglected.

The N-NMOS $M_C$ is added to keep the drain voltages of $M_1$ and $M_2$ almost equal and to desensitize their difference from the supply voltage. The supply sensitivity of $V_{BG}$ is due to the variation of $I_{BG}$ with $V_{DD}$:

$$\frac{d \, V_{BG}}{d \, V_{DD}} \approx R_G \, \frac{d \, I_{BG}}{d \, V_{DD}} \tag{14}$$

where the sensitivity of $V_{EB}$ has been neglected due to its log-dependence on $I_{BG}$. Since the drain voltage of $M_2$ is equal to $V_{BG}$, the sensitivity of $I_{N2}$ is negligible with respect to $I_{N1}$, therefore $d \, I_{BG} / d \, V_{DD} \approx d \, I_{P4} / d \, V_{DD}$.

The dependence of $I_{P4}$ on $V_{DD}$ is due to the finite output resistance of the $M_3$-$M_4$ mirror and to the dependence of $I_{N1}$ on $V_{DS1}$ from (2). Neglecting the supply-dependence of the gate voltage of $M_C$, the sensitivity of $I_{P4}$ to $V_{DD}$ with $M_C$ becomes:

$$\frac{d \, I_{P4}}{d \, V_{DD}} \approx N \cdot \left(\frac{n_n \, v_{th}}{V_{AN}}\right)^2 \cdot \frac{1}{L_1 \, L_C} \cdot \frac{1}{R_A} + \frac{N \, I_{N1}}{V_{AP} \, L_4} \tag{15}$$

where $V_{AN}$ and $V_{AP}$ are the normalized Early voltages[33]. If the calculation is repeated without $M_C$, it is found that $M_C$ reduces the line sensitivity of $I_{P4}$ and $V_{BG}$ by a factor $\left(V_{AN} \, L_C\right) / \left(n_n \, v_{th}\right)$.

A mandatory feature of any analog cell to be used in a low power system is the ability to be driven in power-down condition. In the circuit of Figure 1, the presence of N-NMOS devices, which requires a negative gate-to-source voltage to limit their drain current at the level of the leakage current, raises some design issue. The power-down condition can be achieved by introducing a PMOS switch that shorts the gate of $M_3$ and $M_4$ to the supply. Thus, switching off the PMOS current mirror at the top of the

circuit in Figure 1 guarantees that the current through the right branch, i.e. $M_4$, $M_2$, and $R_B$, and through $Q_1$ is reduced to the leakage current. The left branch requires an additional NMOS switch placed in series to $R_A$ to inhibit the current flow through N-NMOS $M_C$. The value of $R_A$ in the megaohm range makes negligible the effect of the series resistance of the additional NMOS switch on the bandgap behavior.

## 2.2 | Self Start-up analysis

Several bandgap architectures[34,13,35,36,20] are based on a feedback loop where an amplifier sets the bias current injected in a couple of nodes to null their voltage difference. This circuit technique usually leads to an additional bias point with almost zero current, thus forcing the adoption of a dedicated SUPC[21]. The proposed bandgap reference is, by design, free from the undesired bias point, since the current is set by a pair of N-NMOS devices with the gate tied at the ground potential. Indeed, an N-NMOS device, with a negative threshold voltage and with $V_{GS} = 0$, is biased in the moderate (M.I.) or even in the strong inversion (S.I.), depending on the value of $V_{TN}$. In the circuit of Figure 1, at the start-up, $I_{N1}$=$I_{N2}$=0 and, consequently, $V_{S1}$=$V_{S2}$=$V_{BG}$=0. As soon as the voltage at the drain of $M_C$ reaches a few thermal voltages, $M_C$ is biased in the M.I. or S.I. and saturation due to its negative $V_{TN}$. Since $I_{P4}$ is linked to the drain current of $M_C$, the output voltage $V_{BG}$ rises, while the drain voltage of $M_1$ follows the $V_{BG}$ voltage, due to the unity voltage gain from the gate to the source of $M_C$. Therefore both $M_1$ and $M_2$ leave the linear region and are biased in M.I. or even S.I.. Afterward, the negative feedback introduced by $R_A$ (and $R_B$) progressively reduces the drain current of $M_1$ (and $M_2$) until a stable bias point is reached.
It is worth noticing that in the circuit of Figure 1 a positive feedback loop involving $M_C$, $M_3$, and $M_4$ is present. To exclude any stability issue, the low-frequency loop gain $T_C$ must be evaluated:

$$T_C \approx \frac{g_{mC}}{1 + g_{mC} \cdot \left(r_{ds1} + R_A\right)} \cdot \frac{R_G\, g_{m4}}{g_{m3}} \tag{16}$$

where $g_{m<i>}$ and $r_{ds<i>}$ are respectively the small-signal transconductance and drain-source resistance of $M_{<i>}$. Cosidering that in W.I. $g_{mC} \approx g_{m1}$ and the intrisic voltage gain of $M_1$, i.e. $g_{m1} r_{ds1}$, is expected to be much higher than unity, (16) is simplified as follows:

$$T_C \approx \frac{N\, R_G}{r_{ds1} + R_A} \tag{17}$$

Sizing $M_1$ with $r_{ds1} >> R_G$, will keep the value of $T_C$ below unity over process corner and temperature range, thus leading to an inherently stable loop, with no issues at the start-up.

## 2.3 | Bandgap Curvature and Tolerance

A non-linear equation is obtained from (2) with $M_1$ in the saturation region and $V_{GS1}$ replaced by its current-dependent expression, i.e. $V_{GS1} = -I_{N1} \cdot R_A$:

$$I_{N1} - I_{SS} \cdot \left(\frac{W}{L}\right)_1 \cdot e^{\frac{-I_{N1} R_A - V_{TN}}{n_n \cdot v_{th}}} = 0 \tag{18}$$

The analytic expressions of $I_{N1}$ is obtained by solving (18):

$$I_{N1} = \frac{n_n v_{th}}{R_A} \cdot \mathrm{W}\left(\alpha_L\right) \tag{19}$$

$$\alpha_L = \frac{I^0_{N1}\, R_A}{n_n\, v_{th}} \tag{20}$$

where W($z$) is the Lambert's W function solving the equation $x \cdot exp(x) = z$[37] and $I^0_{N1}$ is the equivalent[1] W.I. drain current of $M_1$ at $V_{GS1} = 0$, i.e. calculated with (2). Following a similar procedure with $V_{GS2} = -I_{N2} \cdot R_A / N$ the expression of $I_{N2}$ is obtained:

$$I_{N2} = N \cdot \frac{n_n v_{th}}{R_A} \cdot \mathrm{W}\left(\frac{\alpha_L}{N}\right) \tag{21}$$

Furthermore, a design equation for $(W/L)_1$ is obtained from (2), with $I_{N1}$ as independent variable and $V_{S1}$ as a parameter:

$$\left(\frac{W}{L}\right)_1 = \frac{I_{N1}}{I_{SS}} \cdot e^{\frac{V_{S1} + V_{TN}}{n_n v_{th}}} \tag{22}$$

[1] With $V_{TN} < -4 \cdot v_{th}$ the N-NMOS device is in S.I. at $V_{GS} = 0$ and, hence, the effective drain current will differ from $I^0_{N1}$.

From (11), $V_{S1}/\left(n_n v_{th}\right)$ is expected to be large. Thus if a bias current in the tens-to-hundreds nA range is required, a large aspect ratio for $M_1$ is called for, in the case of slightly negative $V_{TN}$ and a typical value for $I_{SS}$.
The tolerance affecting $I_{N1}$ and $I_{N2}$ at some T is mainly ascribed to $R_A$ and $n_n$, since the W($x$) function exhibits a small derivative at high values of $x$. Hence, the sensitivity of $I_{N1}$ to $I_{N1}^0$, i.e. to the MOS process corner, is strongly attenuated. Therefore, with respect to leakage-based references [15,13,14,18,38,16], the proposed circuit exhibits a much smaller variation of the bias current over the MOS corner space. Furthermore, the mismatch and process tolerance affecting $R_A$ and $R_B$ cause a negligible deviation from the PTAT behavior, as proved by simulations and experimental results. Table 1 reports the values of the normalized sensitivities of $I_{N1}$ and $I_{BG}$ to $k_n \equiv \mu_n C_{OX}$, $V_{TN}$, and $n_n$, for the NBB reference:

$$S_{kn} \equiv \frac{\partial I_{N1}}{\partial k_n} \cdot \frac{k_n}{I_{N1}} \quad , \quad S_{nn} \equiv \frac{\partial I_{N1}}{\partial n_n} \cdot \frac{n_n}{I_{N1}} \quad , \quad S_{VTN} \equiv \frac{\partial I_{N1}}{\partial V_{TN}} \cdot \frac{V_{TN}}{I_{N1}} \tag{23}$$

$$S_{kn}^{BG} \equiv \frac{\partial I_{BG}}{\partial k_n} \cdot \frac{k_n}{I_{BG}} \quad , \quad S_{nn}^{BG} \equiv \frac{\partial I_{BG}}{\partial n_n} \cdot \frac{n_n}{I_{BG}} \quad , \quad S_{VTN}^{BG} \equiv \frac{\partial I_{BG}}{\partial V_{TN}} \cdot \frac{V_{TN}}{I_{BG}} \tag{24}$$

$$\tag{25}$$

Two technology cases were considered (55 nm and 65 nm) in the sensitivity analysis in Table 1. The former exhibits a threshold voltage close to zero, i.e. $V_{TN} \approx$-55 mV, and the latter a large (negative) threshold, i.e. $V_{TN} \approx$-250 mV. Both designs were sized for $I_{N1}$=20 nA, $V_{S1} \approx$ 330 mV, and with N=12. From the simulations, it results clearly that the lower $V_{TN}$, the higher the corresponding sensitivity for both currents. A relevant parameter of a bandgap circuit is the TC, which, in hybrid references, is due to the non-linearity, with respect to $T$, of the PTAT current, i.e. $I_{BG}(T)$, and of the CTAT voltage, i.e. $V_{EB}$. If the analysis is limited to the former contribution, the equation of $I_{BG}$ is written from (19), (21), and (9):

$$I_{BG}(T) = \frac{N\, n_n\, v_{th}}{R_A} \cdot \left\{ \mathrm{W}\left[\alpha_L(T)\right] - \mathrm{W}\left[\frac{\alpha_L(T)}{N}\right] \right\} + (N-1) \cdot I_{Lk}(T) \tag{26}$$

where the substrate currents of $M_1$ and $M_2$ has been taken into account. In a MOS transistor, the drain/source-to-substrate current is ascribed to the p-n junction leakage and to the gate-induced drain leakage (GIDL) currents, i.e. $I_{Lk} = I_{LkD} + I_{LkS}$ in Figure 1, [39]. The impact ionization effect adds a further contribution [40,41,42]. Both the junction leakage and the GIDL currents exhibit an approximate exponential dependence on the temperature [40,43]. The effect is enhanced in the NBB circuit if $M_1$ and $M_2$ are sized with a large width, as from (22), since it affects the slope of $I_{BG}(T)$ at high temperature due to the higher value of $I_{LK}(T)$. Furthermore, N-NMOS devices exhibit a larger depletion width than standard-$V_T$ devices at the same bias, due to the lower channel doping, thus leading to a higher substrate current [39]. Concerning the gate leakage, it is negligible if thick-oxide devices are used.
The increase of the first-order derivative of $I_{BG}(T)$, due to $I_{Lk}$, over-compensates the CTAT behavior of $V_{EB}(T)$, leading to a local minimum in the $V_{BG}(T)$ function. The effect is clearly visible in the simulation results of Figure 2, which are obtained from the design of the NBB reference in the previously considered technologies with $I_{N1}$=20 nA and N=12. The device models include the GIDL effect and the drain/source-to-substrate diodes. The circuits were sized with different values of $R_A$ to operate with the same $V_{S1}$ value (traces A and B) or with almost the same overdrive voltage for $M_1$ and $M_2$ (traces A and C). From simulation results the worst average TC is obtained with the highest $V_{S1}$, at the same $V_{GS1} - V_{TN}$, or with the highest $V_{TN}$, at the same $V_{S1}$. This is due to the larger width of $M_1$-$M_2$, as from (22), and, hence, to the higher leakage current.

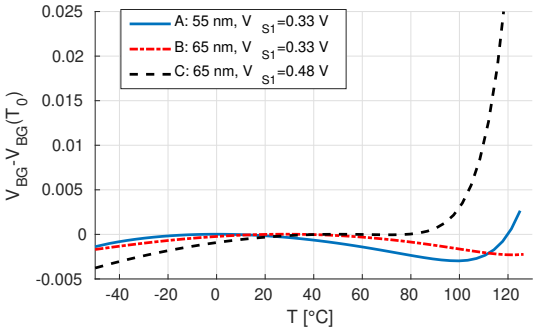


**FIGURE 2** Simulated $V_{BG}$-$V_{BG}(T_0)$ of the NBB designed in 55 nm ($V_{TH}$=-55 mV) and 65 nm ($V_{TH}$=-250 mV) technologies.

At low-temperatures, the effect of $I_{Lk}$ on the curvature is negligible. As shown in Appendix, Section .1, if $I_{Lk}$ is not considered, (10) can be derived from (26) by resorting to the log-series expansion of W($x$)[44].
Summarizing, the design equations (19), (20), and (21), shown in this section, allow a preliminary estimation of the variation of the bias current due to the process tolerance. Eq. (26) and the results shown in Figure 2 demonstrate that the minimization of the curvature of $V_{BG}$, in a current-constrained design, requires the optimization of the width of $M_1$ and $M_2$.

## 2.4 | Area and curvature optimization

In the previous section, the substrate currents of $M_1$ and $M_2$ have been identified as the cause of the local minimum of $V_{BG}$ occurring at high temperatures. Such currents are reduced if the width of N-NMOS devices $M_1$ and $M_2$ can be reduced. This is made possible in the Threshold-Compensated NBB (THC-NBB) reference in Figure 3, where the gate voltage of $M_1$ and $M_2$, i.e. $V_G$, is generated by a diode-connected N-NMOS device $M_5$. This transistor is biased with a scaled replica of $I_{N1}$ and is sized to operate with $V_{GS5} > 0$ V. Still in Figure 3, an option for reducing the silicon area is alos introduced. Indeed, with the current mirror $M_3$-$M_6$ the current through resistor $R_A$ is increased, with respect to $I_{N1}$, by a factor equal to $\left(1 + K_1\right)$, hence reducing the value of $R_A$ accordingly, assuming $I_{N1}$ and $V_{S1}$ unchanged. It is worth noticing that the area reduction is paid for by an increase in current consumption. Therefore this option should be activated if an optimum trade-off between area and current consumption is required. The current gain $K_2$ of the $M_3$-$M_4$ mirror must be set to:

$$K_2 = N \cdot \left(1 + K_1\right) \tag{27}$$

where $N \equiv R_A/R_B$, as for the basic NBB circuit, and $K_1$ is set to 0 if the low-area option ($M_6$ in Figure 3) is not implemented. The almost-PTAT current $I_{BG}$ is modeled with (26), but with $\alpha_L$ and $R_A$ being replaced by $\alpha_{L-C}$ and $R_{A-C}$ respectively:

$$\alpha_{L-C} \equiv \frac{I^0_{N1-C}\, R_{A-C}}{n_n\, v_{th}} \tag{28}$$

$$R_{A-C} = \left(K_1 + 1\right) R_A \tag{29}$$

where $I^0_{N1-C}$ is now defined as

$$I^0_{N1-C} = I_{SS1} \left(\frac{W}{L}\right)_1 \cdot e^{\frac{V_{OV5}}{n_n \cdot v_{th}}} \tag{30}$$

The parameter $V_{OV5}$ corresponds to the overdrive voltage of $M_5$, i.e. $V_{OV5} \equiv V_{GS5} - V_{TN}$. Equation (30) holds for $M_5$ in S.I. down to the W.I.. Using the log-series expansion of the W($x$) function[44], as done for (26), the approximate equation for $I_{BG}$ is obtained:

$$I_{BG} \approx \frac{N\, n_n\, v_{th}}{R_A} \ln\left[(K_1 + 1) \cdot N\right] \tag{31}$$

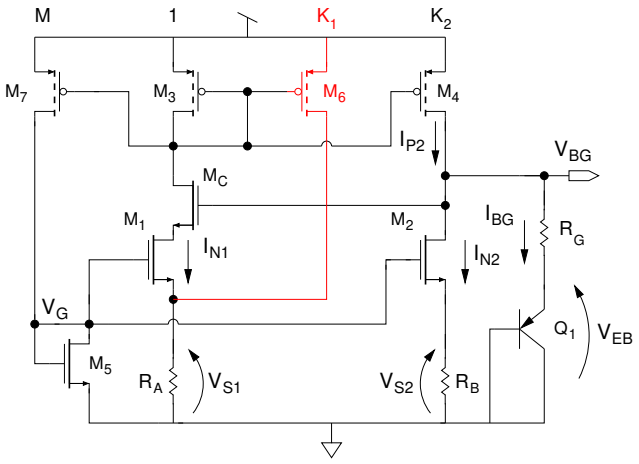


**FIGURE 3** Schematic of the THC-NBB reference. In red the optional part for area saving.

With the same procedure used for the NBB reference, a design equation for the aspect ratio of $M_1$ is obtained:

$$\left(\frac{W}{L}\right)_1 = \frac{I_{N1}}{I_{SS}} \cdot e^{\frac{V_{S1}-V_{OV5}}{n_n v_{th}}} \tag{32}$$

Hence, if $V_G > 0$ V, the same value of $I_{N1}$ is obtained with a smaller width of $M_1$ than in the circuit in Figure 1. Since the smaller width leads to a lower substrate current, a lower average TC is expected in the THC-NBB reference in Figure 3. The local minimum, occurring for $V_{BG}(T)$ at high temperatures can be optimized by tuning the value of $V_{OV5}$.

Moreover, the different temperature dependence of $\alpha_{L-C}$ with respect to $\alpha_L$ must be taken into account. Indeed, the temperature behavior of $I_{N1}$ (PTAT) and $\mu_n$, i.e. $\mu_n(T) \propto T^{-3/2}$ [40], results in an almost PTAT behavior of $V_{OV5}$ if $M_5$ is biased in S.I. and saturation:

$$V_{OV5} = \sqrt{\frac{2\,M\,I_{N1}(T)}{\mu_0\,T^{-3/2}\,C_{OX}\cdot(W/L)_5}} \propto T^{5/4} \tag{33}$$

Therefore, since $v_{th} = k\,T/q$, the exponent in (30) becomes almost independent of the temperature, leading to a lower variation over the temperature range of $\alpha_{L-C}$ compared to $\alpha_L$ in the NBB (i.e. without threshold compensation). It is worth noticing that in the circuit of Figure 3, a feedback loop involving $M_5$ has been introduced, with the potential risk of an additional bias point. Nevertheless, the drain current of $M_5$ is zero at the power-on and, consequently, $V_G$=0, leading to the proper start-up, as discussed in Section 2.2.

## 2.5 | Output Noise

The Power Spectral Density (PSD) of the output voltage noise $v^2_{nBG}$ is calculated from the superposition of three noise sources: the BJT collector shot noise $i^2_{nQ1}$ [45], the thermal noise voltage of $R_G\,v^2_{nRG}$, and the current noise from the MOS core generating the PTAT current $i^2_{nBG}$. Usually the last term is largely dominant compared with the other sources, leading to the following approximate expression:

$$v^2_{nBG} \approx R^2_G\,i^2_{nBG} \tag{34}$$

Referring to the circuit in Figure 3, the following noise sources are identified as the contributors of $i_{nBG}$: the channel noise of $M_1$-to-$M_4$ and $M_6$, the resistor noise of $R_A$ and $R_B$, i.e. $v^2_{nRA}$ and $v^2_{nRB}$ [45], and the noise of the voltage $V_G$, $v^2_{nG}$.
The noise affecting the drain current of $M_1$ and $M_2$, i.e. $i^2_{n1}$ and $i^2_{n2}$ respectively, is obtained by circuit analysis:

$$i^2_{n1} = \frac{i^2_{nd1} + g^2_{m1}\cdot\left(v^2_{nG} + v^2_{nRA}\right)}{\left[g_{m1}\,R_A\cdot\left(K_1+1\right)+1\right]^2} \tag{35}$$

$$i^2_{n2} = \frac{i^2_{nd2} + g^2_{m2}\cdot\left(v^2_{nG} + v^2_{nRB}\right)}{\left(g_{m2}\,R_B+1\right)^2} \tag{36}$$

where $i^2_{nd<i>}$ is the channel noise current (PSD) of $M_{<i>}$. The output noise current (PSD) due to N-MOS devices and resistors is calculated by current balance at the drain of $M_2$:

$$i^2_{nBG-NR} \approx \frac{K_2^2\cdot\left[i^2_{nd1} + g^2_{m1}\cdot\left(v^2_{nRA} + v^2_{nRB}\right)\right] + i^2_{nd2}}{\left[g_{m1}\,R_A\cdot\left(K_1+1\right)+1\right]^2} \tag{37}$$

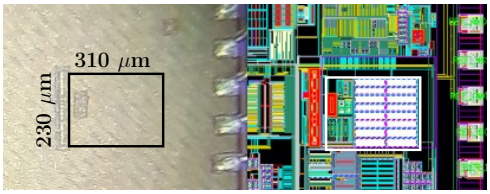


**FIGURE 4** Die micro-photograph (left) and layout (right) of a part of the test-chip. The THC-NBB cell is in the black (photo) and the white (layout) rectangles.

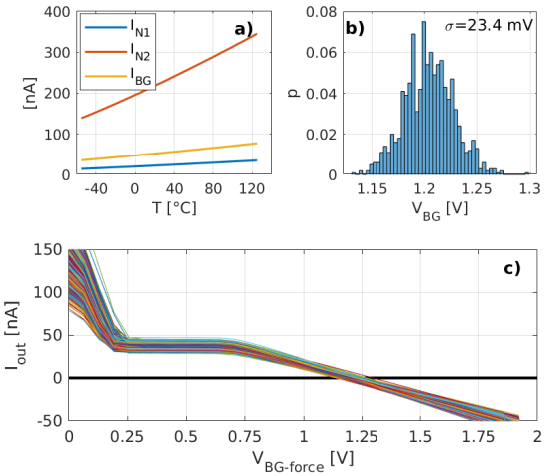


**FIGURE 5** a: simulated $I_{N1}$, $I_{N2}$, and $I_{BG}$ of the THC-NBB. b: Monte-Carlo simulation of $V_{BG}$ at RT (y-axis is the probability of occurrency). c: Monte-Carlo search for bias points.

where the relationship between $R_A$ and $R_B$, i.e. $R_B = R_A/N$, and (27) have been taken into account and assuming $\delta_V \ll 1$, thus leading to $g_{m2} \approx N\, g_{m1} \cdot (K_1 + 1)$.
The contribution of the threshold compensation circuit, i.e. $v_{nG}^2$, is canceled since it generates two correlated noise currents in $i_{n1}^2$ and $i_{n2}^2$. The contribution of the PMOS current mirror is:

$$i_{nBG-P}^2 \approx i_{nd4}^2 + \left(\frac{K_2}{1+K_1}\right)^2 \cdot \left(i_{nd3}^2 + i_{nd6}^2\right) \tag{38}$$

where the approximation holds assuming $g_{m1}\, R_A >> 1$.
Thus, the overall output noise current (PSD) is the superposition of the two contributions:

$$i_{nBG}^2 = i_{nBG-NR}^2 + i_{nBG-P}^2 \tag{39}$$

Therefore, if $g_{m1}\, R_A >> 1$ the PMOS devices are expected to be the most relevant noise contributors if biased in the W.I. region. The equations for the noise-driven design are reported in Appendix, Section .3.

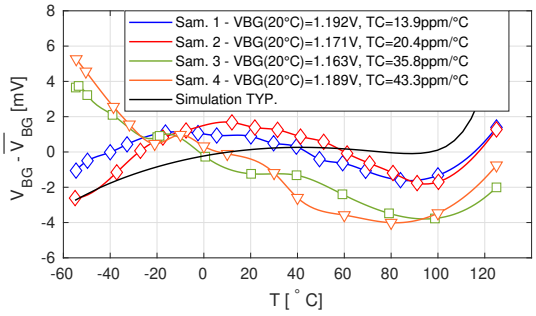


**FIGURE 6** Measured $V_{BG}$ referred to the average value of four samples. Black solid line: simulation (typical corner). The values at 20°C are reported in the legend.

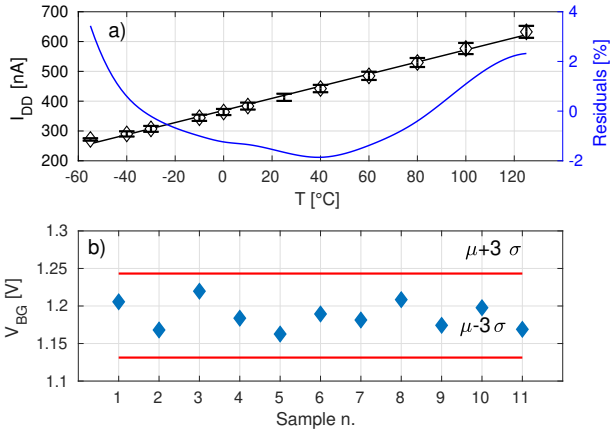


**FIGURE 7** a: measured supply current and residual of the linear fitting, left and right Y-axis, respectively. Error bars show the variation over the available samples. b: output voltage of 11 samples at 30°C.

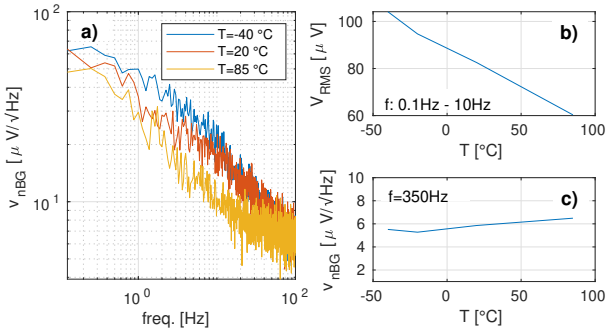


**FIGURE 8** Measured noise performance. a: voltage noise spectra. b and c: low-frequency noise (rms) and PSD value in the flat region vs. temperature.

## 3 | EXPERIMENTAL RESULTS

### 3.1 | Circuit Implementation

The THC-NBB reference in Figure 3 was implemented in a 55-nm CMOS technology, Figure 4. The circuit, with a silicon area of 0.073 $mm^2$, was designed for the extended automotive and aerospace-military temperature range, i.e. -55°C to 125°C, with a supply voltage ranging from 1.5 V up to 4.2 V, for compatibility with Li-Ion batteries. Thick-oxide 2.5-V N-NMOS (with $V_{TN}$=-55 mV) and standard-$V_T$ PMOS devices were used. The former can be over-driven up to 3.3 V of $V_{GS}$ and $V_{DS}$, whereas the latter are LDMOS withstanding 3.6 V and 5.5 V of maximum $V_{GS}$ and $V_{DS}$, respectively. At the maximum supply, the critical device is $M_C$ with $V_{DSC} \approx V_{DD} - V_{SG3} - V_{BG}$. P-poly unsilicide resistors were used for $R_A$, $R_B$, and $R_G$ with -700 ppm/°C of TC. From (12) it is clear that the resistor tolerance and temperature sensitivity affects only the $V_{EB}$ term, which exhibits a log-dependence on $I_{BG}$.

Figure 5-a shows the simulated $I_{N1}$, $I_{N2}$, and $I_{BG}$ vs. temperature for the typical process corner. The results of the Monte-Carlo simulation (process and mismatch) at RT return a standard deviation of 23.4 mV for $V_{BG}$, Figure 5-b. The size of the main devices of the circuit is reported in Table 2.

The presence of multiple bias points is excluded by the Monte-Carlo simulation in Figure 5-c, which shows a monotone behavior of the output current vs. the forced output voltage. This simulation was performed at the lowest temperature, corresponding to the highest threshold voltage condition.

## 3.2 | Measurements

Experimental measurements were performed on a set of untrimmed silicon samples, packaged in a 48-pin dual-in-line ceramic package. For the DUT characterization over temperature, we used an in-house ACS climatic chamber, featuring a maximum fluctuation of 0.3°C over the -40°C to +125°C range. For the measurement down to -55°C a Flower-ACS chamber with similar temperature stability was used. The DUT temperature was measured with a Platinum PTAT resistor (PT-100) attached to the package.

Figure 6 shows the measured voltage reference at 3.2-V supply, from -55°C to +125°C, of four samples. The average value, calculated over temperature for each sample, is subtracted from the measured $V_{BG}$ values, to highlight the curvature. A maximum TC of 43.3 ppm/°C was measured. All the measured reference voltages show a local minimum in the range of 80°C to 100°C, in good agreement with the simulation result at a typical corner (black line). The measured reference voltages exhibit a local maximum at a lower temperature than expected from the simulation.

The measured current consumption $I_{DD}$ vs. temperature is shown in the plot of Figure 7-a, left y-axis. An average value of 420 nA at T=27$^o$C and $V_{DD}$=3.2 V is measured. The linear fitting of the measured supply current values exhibits a maximum error of about 4%. Since the supply current is equal to $I_{N1} \cdot \left(1 + K_1 + K_2 + M\right)$, the small deviation from the PTAT behavior is due to the temperature dependence of the W $\left(\alpha_L\right)$ term in (19). The measured tolerance of $I_{DD}$ over the available sample population is shown by the error bar at each temperature point. Peak-to-peak variations of 3.1% and 3.0% are measured at 125°C and -40°C, respectively. Figure 7-b shows the $V_{BG}$ value of 11 samples at 30°C. The measured mean value of $V_{BG}$ is 1.181 V, with 1.57% of relative standard deviation, and a spread of 57 mV.

The measured power spectral density (PSD) in the low-frequency region at the low, typical, and high temperature are shown in Figure 8-a. In Figure 8-b and Figure 8-c the plots of the root-mean square (rms) value of the noise voltage in the 0.1-10 Hz range and of the power density in the white region vs. T are shown. Therefore, a positive coefficient is measured for the spectral density in the flat region, in agreement with the noise model discussed in Appendix, Section .2. The negative derivative of the low-frequency noise is ascribed to the temperature dependence of the MOS 1/f noise[53].

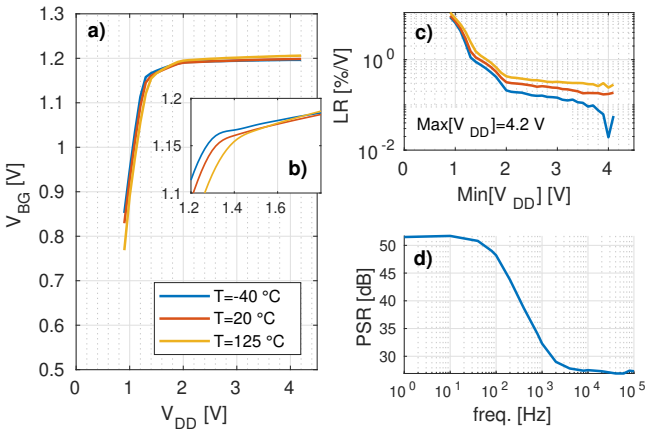


**FIGURE 9** a and b: measured $V_{BG}$ vs. $V_{DD}$. c: line regulation vs. minimum supply. d: PSR at 3.2-V supply.

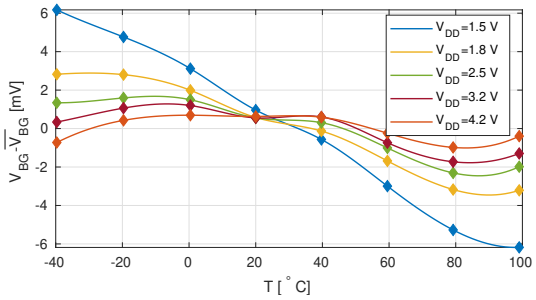


**FIGURE 10** Measured $V_{BG} - \overline{V_{BG}}$ vs. temperature over the supply range.

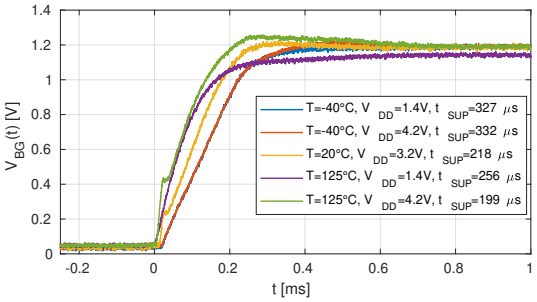


**FIGURE 11** Measured $V_{BG}$ waveforms at the power-on at different temperatures.

The variation of the voltage reference with the supply voltage, at three temperatures, is shown in Figure 9-a, with a zoomed view of the reference voltage, over a reduced supply range, in Figure 9-b. The measured line regulation for the three temperatures, is within 1%/V for a voltage supply range from 1.5 to 4.2 V, whereas it is lower than 0.6%/V and 0.3%/V with 1.8 V and 2.4 V as minimum voltage supplies, respectively.

Moreover, the measured (small-signal) power supply rejection, PSR, shown in Figure 9-d, is 52 dB at low-frequency and about 32 dB at 1 kHz, with a 3.2-V supply. The DC PSR is aligned with or better than other reported circuit implementations with a current consumption lower than 1 $\mu$A. The supply-rejection could be significantly improved with a cascode PMOS current mirror, at the cost of a smaller supply voltage range.

The measured $V_{BG}$ of a sample vs. temperature and supply voltage is shown in Figure 10, highlighting an almost constant average TC from 3.2 V up to 4.2 V. In the lower end of the supply range the reference voltage exhibits a progressively increasing CTAT behavior. This effect is due to the supply sensitivity of $I_{P4}$, according to (15).

The measured start-up time, at 1% settling error, is between 200 $\mu$s and 330 $\mu$s over the supply voltage range. An on-chip shunt capacitance of 5 pF was introduced at the output. The oscilloscope waveforms are shown in Figure 11, where the supply voltage transition from 0 V to $V_{DD}$ occurs at 0 s.

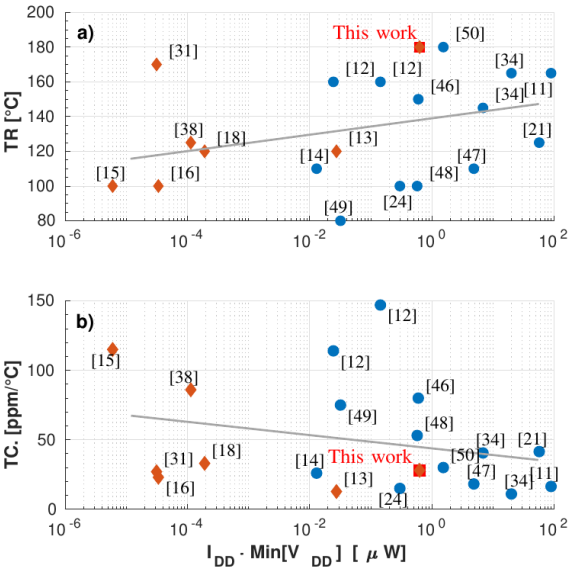


**FIGURE 12** State of the art survey: blue circles: bandgaps with SUPC, orange diamonds: without SUPC, square: proposed design.

### 3.3 | Discussion and comments

The measured performance metrics of the proposed reference are summarized in Table 3 and compared with state-of-the-art low-power bandgap circuits, featuring a minimum supply voltage lower than 2 V [12,13,14,15,16,18,24,34,31,38,46,47,48,49,50,51,52]. Differently from the leakage-based approach [13,14], this circuit reaches a minimum operating temperature of -55°C with a 180 °C of TR, which is the largest reported in the literature at the same power consumption level. Furthermore, to the authors' knowledge, the proposed reference is the first featuring a supply voltage range from 1.5 V and up to 4.2 V, with a sub-microampere current consumption, among the silicon-proven designs reported in literature, implemented in a technology node equal or lower than 55 nm. Indeed, in [54] a bandgap reference in 28-nm technology with 5-V maximum supply is reported, but it exhibits a current consumption of 2.5 $\mu$A and a TR of only 150°C. The 28-nm PMU in [55] operates at 5 V, with a 1-$\mu$A bandgap reference, but the TR and the TC are not provided. The 5-V sub-microampere bandgap reported in [56], designed in a 180-nm technology node exhibits a temperature range of 170°C, but it is not compatible with a voltage supply lower than 2 V. The 350-nm voltage reference proposed in [57] is compatible with Li-Ion battery voltage range, but it exhibits a minimum supply voltage of 2.8 V and a temperature range of 80°C. Other N-NMOS-based bandgap circuits were reported, but none is capable to achieve our large temperature range. In [16], an N-NMOS is used for generating the bias current flowing in a stack of diode-connected PMOS devices. A power consumption of 35 pW has been achieved, but the bias current varies exponentially with the temperature, with a TR of only 100°C. In [18] and [31] N-NMOS devices are used only for cascoding purposes. The circuit in [31] achieves a TR of 170°C, but with a minimum temperature of 0°C. This severe limitation is probably a consequence of the four orders magnitude variation of the bias current over the operating TR.

The low-frequency PSR value reported in Table 3 is aligned with those of the other state-of-the-art bandgap circuits. The THC-NBB reference exhibits a comparable silicon area with the most of the other circuits in the table. The silicon occupied areas of [15,16,18,31,38,50] are approximately one order of magnitude smaller, due to the absence of high value resistors. Our bandgap circuit achieves slightly worse noise performance at room temperature than other leakage-based implementations [26,16], despite the higher current consumption. This is ascribed to the higher number of devices. Nevertheless, the white noise exhibits a relatively small dependence on the temperature, as shown in Figure 8-c. This specific feature is particularly relevant if the circuit provides the full-scale reference to an A/D or a D/A converter. Indeed, the noise affecting the reference sets an upper bound for the peak Signal-to-Noise ratio (SNR) of the converter, irrespective of its architecture. With a maximum rms noise of about 100 $\mu$V, as shown in Figure 8-c, the peak-SNR of the A/D converter is limited to approximately 78 dB. Therefore, the proposed voltage reference generator is compatible with a maximum effective resolution of 12.7 bits over the temperature range.

The scatter plots of Figure 12-a and of Figure 12-b show the TR and the TC vs. the power consumption at the minimum supply voltage [36,46,12,11,47,21,48,24,13,18,14,16,38,15,34,49,50,31]. None of the reference circuits on the left side of the graphs, hence with the lower power consumption, incorporates any SUPC, thus confirming the trend to avoid it in ultra-low power designs. It is worth to notice that our bandgap is the only one operating on a temperature range of 180°C, with power consumption lower than 1 $\mu$W. Moreover, except for [31], which exhibits a minimum temperature of 0°C, the measured mean TC is the lowest reported among the references featuring a TR larger than 120°C, and maximum power within 1 $\mu$W.

## 4 | CONCLUSION

A bandgap reference based on N-NMOS devices has been presented. Thanks to the novel topology, the proposed circuit operates from -55°C to 125°C, exhibits a minimum voltage supply of 1.5 V, a current consumption of 420 nA, and can be directly attached to a Li-Ion battery. The start-up circuit is not required since the proposed bandgap exhibits a single operating point. The measured TC and the limited power consumption make this circuit suitable for WSNs operating over the automotive and military-aerospace temperature range.

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# APPENDIX

## .1 Approximation with the log-series expansion.

At high values of the independent variable $x$, the W($x$) function can be approximated by the log-series expansion[44]. The expansion, limited to the second term, gives the following equation:

$$\mathrm{W}(x) \approx \ln(x) - \ln[\ln(x)] \tag{1}$$

Therefore, from (26) $I_{BG}$ is approximated as:

$$I_{BG} \approx \frac{N\, n_n\, v_{th}}{R_A} \cdot \left\{ \ln(N) - \ln\left[ \frac{\ln(\alpha_L)}{\ln(\alpha_L/N)} \right] \right\} \tag{2}$$

which corresponds to (10) with $\delta_V \approx \ln\left[\frac{\ln(\alpha_L)}{\ln(\alpha_L/N)}\right]$.

## .2 Output noise voltage

The equation of the power spectral density of the output voltage noise is reported in (34), where the contribution of $Q_1$ has been neglected. The dependence of the output voltage noise on the temperature is obtained starting from the equations of $i^2_{nd<i>}$, $v^2_{nRA}$, and $g_{m<i>}$, assuming all MOS transistors in W.I.:

$$i^2_{nd<i>} = 2\, q\, I_{D<i>} \tag{3}$$

$$v^2_{nRA} = 4\, k\, T\, R_A \tag{4}$$

where $I_{D<i>}$ is the drain bias current of $M_{<i>}$. The following equation is obtained for the power spectral density of the noise voltage from (19) and (34):

$$\begin{aligned} v^2_{nBG} \approx\; & 2\, k\, T\, \frac{R_G^2}{R_A}\, N\, \mathrm{W}(\alpha_\mathrm{L}) \cdot \\ & \left\{ \frac{2 \cdot (N+1)\, \mathrm{W}(\alpha_\mathrm{L}) + n_n \cdot \left[ N \cdot \left( K_1 + 1 \right) + 1 \right]}{\left[ \mathrm{W}(\alpha_\mathrm{L}) + 1 \right]^2} + \right. \\ & \left. n_n \cdot (N+1) \right\} \end{aligned} \tag{5}$$

Since the dependence of the $W(\alpha_L)$ on the temperature can be neglected, (5) proves an approximate linear dependence of the power spectral density (in the white region) on the absolute temperature. The theoretical result is confirmed by the measurements in Figure 8-c, where the ratio of the values of $v_{nBG}$ at 85°C and at -20°C is very close to the square-root of the ratio of the absolute temperatures.

## .3 Design Optimization

In this section a set equations is presented for the automatic sizing of the main devices and currents in the THC-NBB in Figure 3. For the noise spectral density in the flat region, a useful equation is obtained from (34) with (3) and (4) in this appendix, if $I_{N1}$ and $V_{S1}$ are taken as independent variables. To this aim, $R_A$ and $R_G$ are written as:

$$R_A = V_{S1} / \left[ I_{N1} \cdot \left( K_1 + 1 \right) \right] \tag{6}$$

$$R_G = V_{PTAT} / I_{BG} \tag{7}$$

where $V_{PTAT}$ is the difference between $V_{BG}$ and $V_{EB}$. Then, if $I_{BG}$ is replaced by (31) the following equation of $v^2_{nBG}$ at RT is obtained:

$$\begin{aligned} v^2_{nBG} \approx\; & \frac{2\, {V_{\mathrm{PTAT}}}^2\, {v_{\mathrm{S1}}}^2\, q}{I_{\mathrm{N1}} \cdot \left( K_1 + 1 \right) \cdot \ln^2 \left[ N \cdot \left( K_1 + 1 \right] \right)} \cdot \\ & \left[ \frac{2\, v_{\mathrm{S1}} + n_n \cdot \left( K_1 + 1 \right)}{n_n \cdot \left( v_{\mathrm{S1}} + 1 \right)^2} + \frac{N+1}{N} \right] \end{aligned} \tag{8}$$

where

$$v_{S1} \equiv \frac{V_{S1}}{n_n v_{th}} \tag{9}$$

The first term within square brackets in (8) refers to the noise originated from the N-NMOS devices and resistors, whereas the second term is the contribution of the PMOS mirror. Therefore, (8) reveals that $v_{nBG}^2$ is inversely proportional to $I_{N1}$ with $v_{S1}$ constant, whereas the contribution of the N-NMOS and resistors is reduced by increasing $V_{S1}$.

The silicon area is approximately proportional to the sum of the values of $R_A$, $R_B$, and $R_G$, since it is largely dominated by the high-value resistors. Hence, the following equation for area-driven design optimization is obtained:

$$\begin{aligned} Area \approx & \frac{W_R^2}{R_\square} \cdot \frac{V_{S1}}{I_{N1} \cdot (K_1 + 1)} \\ & \cdot \left[ \left(1 + \frac{1}{N}\right) + \frac{V_{PTAT}}{n_n v_{th} \ln\left[N \cdot (K_1 + 1)\right]} \right] \end{aligned} \tag{10}$$

where $W_R$ is the resistor width, assumed equal for all resistors in the design, and $R_\square$ is the square resistance. Referring to the schematic of Figure 3 and from (27), the current consumption of the THC-NBB circuit is:

$$I_{DD} = I_{N1} \cdot \left[(K_1 + 1) \cdot (N + 1) + M\right] \tag{11}$$

Therefore, (2), (11), (8), and (10) allow the global design optimization for current consumption, area, noise voltage, and PTAT error.

As design example of the THC-NBB in Figure 3, the following design targets are given: $I_{DD}$=420 nA, $v_{nBG}$ ≈7 $\mu V/\sqrt{Hz}$, and Area≈0.075 mm$^2$. The technology parameters are $R_\square$=2 kΩ and $W_R$=2 $\mu$m with $I_{SS}$=1.85 $\mu$A and $n_n$=1.1 both extrapolated at $V_{GS} - V_{TN}$ ≈-200 mV.

A first circuit sizing is obtained by solving (8), (10), and (11), with $I_{N1}$, $V_{S1}$, and $K_1$ as unknown variables. Since the problem is under determined, the values of $N$ and $V_{GS5}$ must be preliminary chosen. For this example, with $N$=3 and $V_{GS5}$=50 mV, the set of equations returns $I_{N1}$=23 nA, $V_{S1}$=330 mV, and $K_1$=3. The aspect ratio of $M_1$ and $M_2$ is therefore obtained from (32), i.e. 41 $\mu$m/$\mu$m. It is worth noticing that these results are in very good agreement with the final values, obtained by simulation tuning, shown in Table 2. The procedure can be repeated by changing the value of $V_{GS5}$ to verify the effect on the curvature and the position of the local minimum of $V_{BG}(T)$ as discussed in Section 2.4.

*The data that support the findings of this study are available from the corresponding author upon reasonable request.*

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**TABLE 1** Sensitivity of $I_{N1}$ to N-NMOS model parameters

| | $S_{kn}$ | $S_{VTN}$ | $S_{nn}$ | $S_{kn}^{BG}$ | $S_{VTN}^{BG}$ | $S_{nn}^{BG}$ |
|---|---|---|---|---|---|---|
| $V_{TN}$=-55 mV | 0.12 | 0.16 | 1 | 18m | 24m | 1 |
| $V_{TN}$=-250 mV | 0.11 | 0.66 | 0.5 | 17m | 0.1 | 0.92 |

**TABLE 2** Component Values of the THC-NBB prototype

| Device | W/L | Res | [Ω] | Param. | Value |
|---|---|---|---|---|---|
| $M_1$ | 80/2 | $R_A$ | 3.6 M | $K_1$ | 3 |
| $M_2$ | 80/2 | $R_B$ | 1.2 M | $K_2$ | 12 |
| $M_5$ | 1.4/50 | $R_G$ | 12 M | $M$ | 2 |

**TABLE 3** Performance comparison with state-of-the-art low-power untrimmed reference circuits

| | **TR** [C°] | **Min T**[C°] | **TC** [ppm/°C] | $I_{DD}$[b] [nA] | $V_{DD}$ [V] | **Area** [mm$^2$] | **PSR@DC** [dB] | LR [%/V] | **Acc** 3$\sigma$ [%] | **SUPC** | **Techn. [nm]** | **Arch.**[c] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **This work** | **180** | **-55** | **28** | **420** | **1.5-4.2** | **0.073** | **52** | **1** | **4.7** | **NO** | **55** | **Hyb.** |
| [46] | 150 | -50 | 80 | 600 | 1-3 | N.A. | N.A. | N.A. | 1.70 | YES | N.A. | MOS |
| [12] | 160 | -40 | 147 | 120 | 1.2-1.8 | 0.029 | 62 | N.A. | 2.20 | YES | 180 | Hyb. noRes |
| [12] | 160 | -40 | 114 | 35 | 0.7-1.8 | 0.024 | 56 | N.A. | 3.15 | YES | 180 | Hyb. noRes |
| [47] | 110 | -20 | 14.78 | $2.7{\cdot}10^3$ | 0.85-1.8 | 0.063 | N.A. | N.A. | 0.9 | YES | 350 | MOS |
| [48] | 100 | 0 | 53.1 | 500 | 1.15-1.3 | 0.028 | 50 | 0.3 | 3.90 | YES | 90 | Bip. |
| [24] | 100 | -20 | 15 | 214 | 1.4-3 | 0.05 | 45 | 0.002 | 2.8 | YES | 350 | MOS noRes |
| [13] | 120 | -10 | 12.75 | 25 | 1.1-3 | 0.48 | 54 | 0.198 | 0.60 | NO | 350 | Hyb. lb |
| [18] | 120 | -20 | 33 | 0.192 | 1-1.8 | 0.0045 | 55 | 0.02 | 1.56[a] | NO | 180 | Hyb. noRes lb |
| [14] | 110 | 0 | 26 | 9.3 | 1.4-1.8 | 0.055 | 46 | 0.08 | 1.29 | YES | 180 | Hyb. lb |
| [16] | 100 | 0 | 23 | 0.024 | 1.4-3.6 | 0.0025 | 41 | 0.31 | 2.40 | NO | 180 | MOS lb noRes |
| [38] | 125 | -40 | 86 | 0.095 | 1.2-2.1 | 0.0049 | 42 | 0.38 | 5.7[a] | NO | 180 | MOS lb noRes |
| [15] | 100 | -20 | 115 | 0.012 | 0.5-3.3 | 0.0014 | 49 | 0.033 | 2.40 | NO | 180 | MOS lb noRes |
| [34] | 145 | -20 | 40.51 | 9800 | 0.7-0.88 | 0.065 | N.A. | N.A. | 2.35 | YES | 12 | Bip. |
| [49] | 80 | 0 | 125 | 64 | 0.5-1.5 | 0.03 | 40 | 1.6 | 2.00 | YES | 130 | Bip. SC |
| [50] | 180 | -45 | 30 | $1.4{\cdot}10^3$ | 1-1.7 | 0.0025 | N.A. | N.A. | 2.40 | YES | 160 | Hyb. |
| [31] | 170 | 0 | 27 | 0.034 | 0.9-3.3 | 0.0076 | N.A. | 0.27 | 1.8 | NO | 180 | Hyb. noRes lb |
| [51] | 180 | -60 | 32 | $3.8{\cdot}10^3$ | 0.7-1.8 | 0.023 | 27 | N.A. | 2.3[d] | YES | 180 | MOS |
| [52] | 105 | -25 | 97 | 68 | 0.8-1.4 | 0.28 | 68 | 0.1 | 1.05 | NO | 180 | Bip. |

[a] wafer
[b] Measured at the typical supply voltage
[c] **Bip**: BJT for PTAT and CTAT, **Hyb**: MOS (PTAT)+BJT (CTAT), **MOS**: MOS for PTAT and CTAT, **noRes**: resistorless, **lb**: leakage-based, **chop.**: chopping, **SC**: switched capacitors
[d] Half max-to-min range.