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Smart Converters for Industrial Applications: Active Gate Drivers, Rectifiers and Protections

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Introduction

The efforts toward building a more sustainable world demand radical changes in human activities and processes. To meet the ambitious global climate targets, nations must phase in new technologies that drive energy efficiency and lower emissions [1, 2]. In this context, electronic power conversion plays a crucial role, as electrification significantly enhances the efficiency and performance of various energy systems [3, 4]; all this against a setting in which the demand for electricity is growing year by year [5].

This is especially evident in industrial motive power applications, where electric motors consume nearly half of the world's electrical energy [6, 7].

While the absolute energy savings are more pronounced for large megawatt-scale machines, even smaller motors can collectively make a substantial impact [8]. This explains why many home appliances have adopted inverters to drive their motors, achieving energy savings between 25 - 90%, compared to traditional line-connected induction motors [9, 10]. For years the AC Induction motor (IM) has been the world-wide workhorse in civil and industrial applications. Its low cost, robustness, and line supply without electronic converter needs, have made this machine almost ubiquitous in various application fields. However, IM efficiency is low (70 - 92% [11]) if compared to other machines, and it drops drastically if operated at low speed. When the application requires speed regulation different types of motor can be profitably adopted, the most common are permanent magnet motors (PMSM). These machines are very efficient (90 - 95% [12]) over a wide operating range of torque and speed. However, magnets are expensive and the rare-earths mining necessary for their creation is highly polluting [13, 14], often occurring in politically unstable areas [15],

thus contributing to the increasing tensions between states [16]. The Synchronous Reluctance Motor (SyR) and the Switched Reluctance Motor (SRM) represent high-efficiency solutions that does not involve the use of rare-earths. They combine the advantages of simple, cheap and robust motor construction with performances almost comparable to PMSM [17]. This technology dates back to the end of the nineteenth century [18], however, the necessity to use a converter and the high computational power required for the correct operation of the drive have made the use of different solutions preferable. Some tech companies have implemented reluctance motors with great performances (e.g., Tesla Model 3, Dyson vacuum); despite a global electric motor market expansion in new tech areas [19], an industry transition has not happened yet. It is quite easy to realize the importance of this issue, since a 1% increase in average efficiency in the induction motor market, would result in an annual savings of 100 TW h, three times greater to the yearly production of the biggest coal-fired power station in the world [20], equal to an annual emission's saving of 41 Mt of particulate matter [21]. As stated in [22], a potential improvement in the induction motor ecosystem could be retrofitting; Optimize the rotor winding designs, improving the insulations, and the use of low-friction bearings could benefit the potential savings in energy and maintenance costs, and by replacing the original rotor while keeping the stator, would allow the integration of reluctance motors at a low cost [23]. In this perspective, adding a variable-speed drive (VSD) is mandatory and would bring additional benefits in terms of efficiency.

The main objective of this thesis is to provide a starting point for the analysis of a grid-connected VSD system, comprising front-end rectifier, protection circuit and inverter, that can be compatible with induction motors directly connected to the grid, maintaining comparable size and lifespan, to enable a retrofit approach. This thesis does not claim to be exhaustive in its contents and due to the wide variety of subjects within, it will not result in a finished integrated system, however, by adding elements of innovation in the various aspects of the system involved, it aims to be a starting point for future developments.

In order to simplify the view to the macro-system, a divide-et-impera approach has been implemented treating each block separately; different aspects of each block have been evaluated searching to optimize the key points in terms of efficiency, reli-

ability, area and number of components.

Chapter 1

State of the Art

Small industrial and household appliances are typically connected to single-phase AC mains, often resulting in an AC-DC-AC system, where a rectifier is paired with a motor drive [24, 25]. Modern electronic converters are driven by a need for high power density, with advancements in switching frequencies, miniaturized components, and reduced losses. Despite these developments, reliability remains a major concern, particularly in high-reliability markets, where lifetime issues inhibit the widespread adoption of electrical solutions. Research in high-density and high-reliability power conversion focuses on improving control algorithms, architectures, and semiconductor technologies. Optimized control schemes reduce device stress, while improved architectures enable the use of smaller passive components. Additionally, significant advancements in device design and manufacturing processes have led to better performance. This chapter, taking as a benchmark the common AC-DC-AC system, discusses the key technological improvement drivers in power conversion: higher density, greater reliability, and cost efficiency.

A generalized structure for line-connected motor drive [26] can be seen in Fig. 1.1, this has been taken as an example for the structure of this thesis, which is organized as follows:

- in Chapter 1.1 the front-end Rectifier structure is discussed. In chapter 2 a novel control method for power factor correction in AC/DC rectifiers is dis-

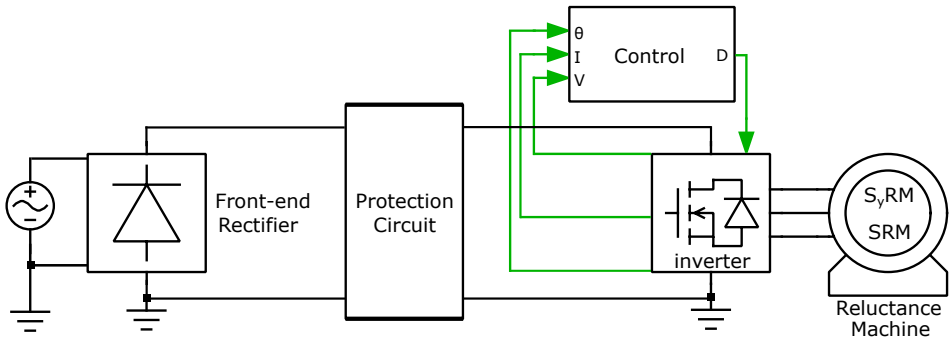


Figure 1.1: Schematic of the proposed single-phase line connected inverter for motor control, the main system blocks are visible: the AC/DC rectifier converter, the line protection system, the inverter with its control block and the motor.

cussed evaluating possible improvements in terms of efficiency and reliability.

- In Chapter 1.2 different types of protection circuits are evaluated. In chapter 3 a new protection circuit is discussed, highlighting its design in terms of efficiency and performance.

- in Chapter 1.3 the relevance of Thermal Sensitive Electric Parameters is discussed. This topic is not directly related to the topology magnified in this study; however, it is of cross-cutting importance for all converters regarding reliability and power density, the three-phase inverter, in particular, appears to benefit from this methodology given the high number of components required to implement it. In chapter 4 a novel calibration procedure for the on-state resistance Thermal Sensitive Electric Parameter is discussed evaluating different improvements of this method.

1.1 Front-end Rectifier

AC/DC rectifiers are electrical topologies used to convert Alternating Current (AC), which periodically reverses direction, into Direct Current (DC), which flows in only

one direction. This conversion is essential for powering most electronic devices, as they typically require a steady DC voltage, making rectifiers key components in various electrical appliances. A common type of AC/DC rectifier is the uncontrolled full bridge rectifier that uses four diodes arranged in a bridge configuration, allowing a full-wave rectification. The term "uncontrolled" indicates that the rectifier does not use controllable elements (like transistors) to manage the current flow. Instead, the diodes passively direct the current, ensuring that it always flows in the correct direction through the load. Full bridge rectifiers are widely used in low-cost power supplies and applications where simplicity and resiliency are important. However, using a simple uncontrolled diode bridge rectifier is not always feasible due to its low power factor and the high total harmonic distortion (THD) it introduces in the current [27].

To address this, Power Factor Correction (PFC) circuits are commonly integrated within the rectifier. Different topologies can be found in literature depending on the needs in terms of output voltage [28, 29] and the number of phases involved [30, 31]. In this study, the single-phase Boost-type PFC topology will be discussed. Boost-type PFC circuits are commonly used in PFC applications [32–35], while this topology can reach almost near-unity power factor. However, this approach necessitates the use of bulky energy storage components, typically electrolytic capacitors (E-Caps), to stabilize the DC link [36, 37]. Unfortunately, these capacitors are costly, and due to their limited ripple current capability [38–40], have reliability issues. Reliability is a critical feature for Power Electronic Converters (PECs) [41], particularly in applications transitioning from converter-less systems to motor drives. A feasible alternative is to use film capacitors (F-Caps), which offer better temperature stability, longer life, and improved resilience to voltage spikes. However, F-Caps have a lower capacitance per unit volume, which typically makes them unsuitable for high-power applications [42]. To enable the use of F-Caps, we propose modifying the boost PFC control strategy to balance energy storage between the inductor and the capacitor, thus reducing the capacitance requirement to a level where F-Caps can be used without a significant increase in volume [43]. While this approach involves a trade-off in terms of power factor and output voltage ripple, achieving unity PF is not always necessary, as regulatory requirements often mandate a PF above 0.9 [44].

Additionally, some output voltage ripple can be tolerated by the load, especially if it includes DC-link voltage monitoring. However, voltage ripple remains a critical factor affecting the lifecycle of F-Caps [42]. In chapter 2 the PFC boost front-end solution with reduced capacity is discussed as proposed in [43]. Then the validation of this approach has been consolidated evaluating the reliability improvement of this solution as proposed in [45].

1.2 Active Overcurrent Protection

The DC circuit breaker is a critical component in modern DC power systems, playing essential roles in both controlling and protecting the power grid. Over time, system protection has evolved significantly, transitioning from simple, rudimentary devices with limited capabilities to sophisticated systems equipped with advanced hardware [46]. These modern protective systems are designed to be more precise and selective in their fault detection and operational response, enabling them to handle a wider range of contingencies with greater accuracy [47]. However, this increased complexity also demands more advanced analytical efforts and refined control algorithms to ensure optimal performance in identifying faults, minimizing disruptions, and safeguarding the grid from damage. The continuous development of DC circuit breakers reflects the growing need for speed, and flexibility in an era where power systems are becoming increasingly decentralized and integrated with renewable energy sources [48].

While conventional electromechanical circuit breakers have a proven track record of being effective and reliable for circuit protection, emerging power distribution technologies and architectures, such as DC microgrids, demand enhanced interruption performance and faster speeds. The need for quicker operation, coupled with advancements in power semiconductor technologies, has driven significant research and development in newer circuit breakers. In High voltage and medium voltage applications, Hybrid DC Breakers (HDCBs) take a key role in grid protection [49]. In a conventional HDCB [50], the semiconductors in the commutating branch carry the fault current until the electromechanical switch of the primary branch quenches the arc and restores sufficient voltage. Solid-state circuit breakers (SSCBs) use power

semiconductors enabling faster switching, making possible smoother turn-off controls. While ideal for fast, precise applications, SSCBs are less suited for high-current environments [51].

Another key element for the load and grid protection is the in-rush current limiting; during the startup phase of many loads, such as lights, induction motors, and power supplies, can draw large inrush currents that may exceed ten times the steady-state peak level [52]. NTC resistors are commonly used in this kind of application; they are economically appealing and simple in implementation, however, those are not usable in certain ambient temperature ranges, and severe cooling systems must be introduced to maintain a low resistive path during normal behavior diminishing the advantages of this approach [53].

Among the different circuit topologies, a possible solution can come from satellite power systems, those must endure long-term operation in space without any possibility of maintenance. To prevent failure propagation caused by short circuits, overcurrent-protected power distribution lines are implemented, isolating faults within any subsystem.

A commonly used protection device is the latching current limiter (LCL) [54], traditionally linear regulators used with a PMOS transistor as shown in Fig. 1.2 [55]. However, the PMOS design has high dissipation and requires large size to handle maximum current. Silicon Carbide (SiC) N-type transistors have been proposed as a better alternative to reduce losses and increase voltage rating [55].

Another alternative is the switching LCL (SwLCL) [56, 57], which uses a buck topology that switches during fault occurrence, limiting the output current as shown in Fig. 1.3, showing a topology proposed in [58]. This design includes an LC filter to reduce harmonics and benefits from wide-bandgap materials like Gallium Nitride (GaN) and SiC to minimize switching losses and allow higher frequencies, reducing size [59].

The SwLCL has lower dissipation compared to the linear one and can operate continuously under overload conditions with proper design. During normal operation, the SwLCL has the pull-up transistor fully on and the filter inductor is involved in the current path; this is not an optimal solution, since the transistor needs derating. Additionally, if the current request on the load changes, more power dissipation

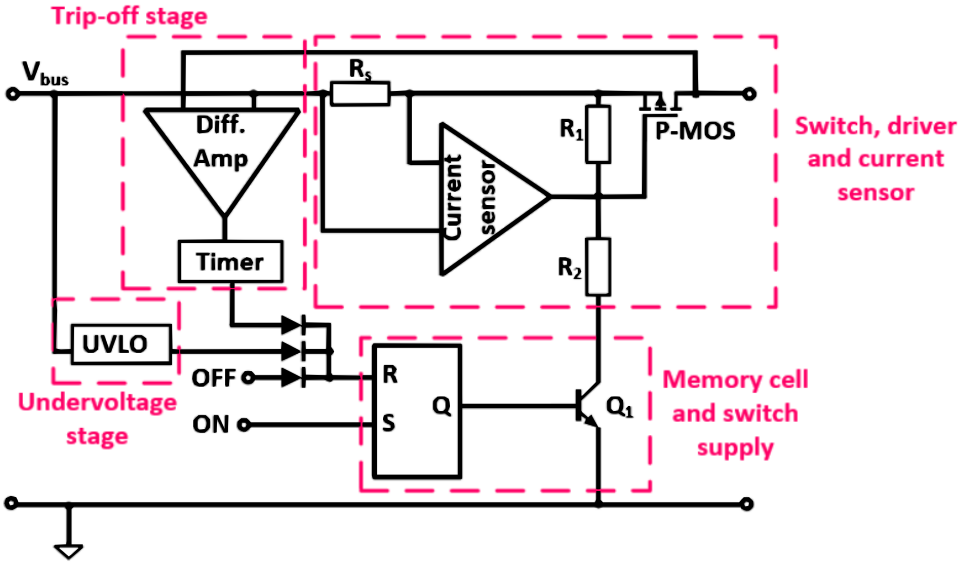


Figure 1.2: Traditional LCL architecture based on a P-MOSFET adopting an analog hysteresis control typically used in space applications.

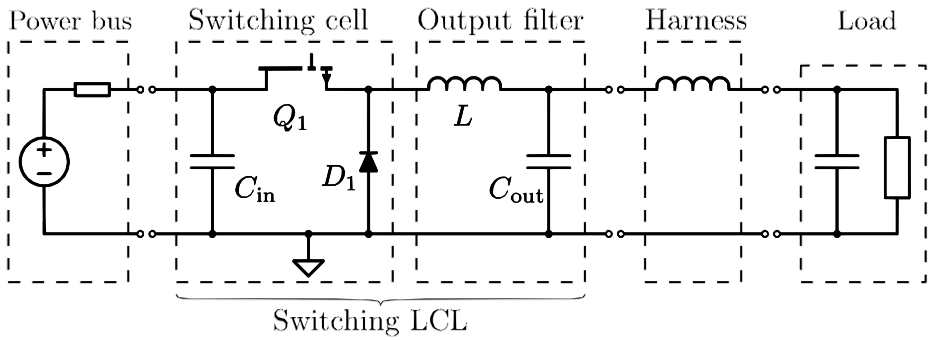


Figure 1.3: Switching LCL topology. The circuit is composed of a buck converter with an output *LC* filter.

on the inductor could arise. To fight these issues, considering the more permissive design standards in the industrial environment than in aerospace, in this work, an additional transistor is added to the circuit to bypass the switching path and the inductor during the normal behavior of the system. In chapter 3 this new topology, called Industrial LCL (ILCL), is discussed. This circuit actively handles faults by maintaining a controlled current regime but also acts as an inrush current limiter during system startup. The use of this technology in the industrial environment makes possible the implementation of digital controls, which are little used in the space field given the high cost of RADHARD-qualified microcontrollers.

1.3 Thermal Sensitive Electric Parameters

In modern power electronics, the junction temperature of power semiconductor devices is very useful information, which can be exploited to improve many performance metrics of power converters [60, 61]. Even in the age of wide band-gap transistors, conscious thermal management can maximize the converter's power density while ensuring reliable operation over time. Generally, commercial converters implement some sort of derating algorithm, aimed at reducing its power output when a certain temperature reaches critical levels [62]. Usually, one or more temperature sensors are placed strategically inside the converter, monitoring different parts and components. The granularity of the temperature measurement is influenced by several converter design choices such as cost, circuit topology, package of the transistors, cooling system type, and application needs. Typically, increasing the number of sensors enables a more refined derating algorithm, but this is not always feasible and the junction temperature of SiC MOSFETs can hardly be measured directly. Instead, it is possible to perform an indirect measurement using temperature-sensitive electric parameters (TSEPs) [63, 64]. Between these parameters, the most mature and well-known is the on-state drain-source resistance, which is commonly adopted for temperature estimation or device characterization, under controlled laboratory environment [65]. Conversely, the use of this technique in real operating conditions, by commercially available converters, is still quite problematic. One of the most critical aspects regards the initial calibration phase, which requires heating the device under

test (DUT) and collecting samples of its drain current (i_d), on-state voltage (v_{ds}) and junction temperature (T_j). This procedure aims to characterize the TSEP across the selected temperature and current range, providing a model that is then used for online temperature estimation.

While the acquisition of current, voltage and temperature can be performed with the converter's own hardware (using dedicated additional circuitry [66,67]), the DUT heating can be achieved with external equipment or exploiting the converter power losses. Concerning the first option, the most popular solutions are:

- thermal chambers [68, 69];
- hot/cold plates in thermal contact with the converter's heatsink [65, 70–72];
- direct heatsink heating using dissipating resistors [73].

These heating techniques are simple and offer good temperature control, enabling the calibration on a wide temperature range. However, they usually require significant power dissipation and long heating times. The aforementioned drawbacks limit the applicability of these procedures on commercial converters produced in high volumes, where the TSEP calibration should be performed at the end of the production line, with minimal modifications to the device.

To simplify the calibration process, if an appropriate electrical load is available, the heatsink heating can be achieved simply by running the converter. In [74, 75] a self-heating procedure is presented for a fully-assembled three-phase inverter, which is using SiC power modules and it is loaded with an induction motor or a synchronous reluctance machine. The authors disabled the inverter's cooling system and synthesized a special mode of operation exploiting the transistor's power dissipation while minimizing the motor's mechanical movement. The aforementioned technique is certainly more suitable for real production environment but imposes a reduced maximum calibration temperature, limited to 80 °C. Additionally, in [76] a thermal chamber is coupled with an inductive load to calibrate the on-state voltage (v_{ce}) in an IGBT-based half bridge converter. The authors propose a simplified procedure requiring only two temperature points, exploiting the theoretical linearity of the relationship between v_{ce} and temperature. While the reduced complexity is advantageous, the thermal chamber requirement is still prohibitive. Furthermore, Wei et

al. [77] described a novel calibration procedure designed for IGBT-based three-phase inverters in EV traction applications, where the $v_{ce} - T_j$ relationship is obtained using only three test points, taking advantage of the natural temperature rise caused by the inverter's DC-link capacitor discharge. When fully developed, this technique should not require any external heater and work with the fully assembled device directly on the vehicle. Nevertheless, this approach is very application specific, requires the vehicle to be driven and parked multiple times to obtain the reference temperatures needed, and since the calibration itself is not complete, the junction temperature monitoring is reduced or even absent.

In chapter 4 a novel calibration procedure for the on-state resistance TSEP in discrete SiC-based power converters is presented. The goal is to present and discuss some of the more relevant issues with the widespread adoption of this TSEP, providing possible solutions, and taking steps towards an accurate, non-invasive, in-circuit calibration technique. In particular, this work focuses on three major areas: simplifying and speeding up the heating process, increasing the junction temperature measurement accuracy during calibration, and identifying the best models for online T_j estimation. The proposed methodology exploits the controlled shoot-through (CST) technique [78]. Although uncontrolled shoot-through phenomena are typically unwanted in push-pull topologies, when controlled and supervised, they can enable a whole unexplored range of features for the power converter. This technique allows a transistor to turn on, during its normally off phase, utilizing a reduced gate voltage. The shoot-through current (which is load independent) can be controlled by varying the gate voltage. To successfully implement this technique, an active gate driver has been specifically designed by the authors.

The CST technique is used to enable the self-heating of the DUT, requiring little power dissipation, providing fast heating times and working even with no electrical load attached. This approach allows the calibration without a thermal chamber or temperature-controlled curve tracer, directly at the end of production, and requires only minimal modifications to the power converter. In addition, the TSEP characterization accuracy is improved by modifying the converter's cooling system to reduce unwanted heat transfer and provide a more accurate reading of its junction temperature.

Chapter 2

AC/DC Front-end

2.1 PFC Converter for DC Link Capacitance Reduction

Adjustable-speed drives usually implement a PFC front-end to reduce the input current distortion; this PFC is often implemented using a boost converter. This topology demands bulky electrolytic capacitors to reduce the output voltage ripple, thus resulting in system size increment and limited lifetime. In this chapter, a dual nested feedback loop control strategy is introduced to minimize output ripple while maintaining low input current distortion. This approach reduces the required capacitance, enabling the use of long-life, low equivalent series resistance (ESR) film capacitors instead of electrolytic capacitors. Additionally, it achieves a high power factor (greater than 0.90) and low output voltage ripple. The proposed control system comprises an inner current loop that utilizes feedback linearization and an outer proportional-integral (PI) controller to regulate system dynamics. The performance of this closed-loop system is assessed through simulations in Chapter 2.1.3 and experimental testing under a constant load in Chapter 2.2, demonstrating the effectiveness of the proposed control algorithm. Furthermore, a workflow for estimating capacitor lifetime in power converters is discussed in Chapter 2.3. This analysis aims to evaluate the reliability improvement gained by using a film capacitor instead of an electrolytic

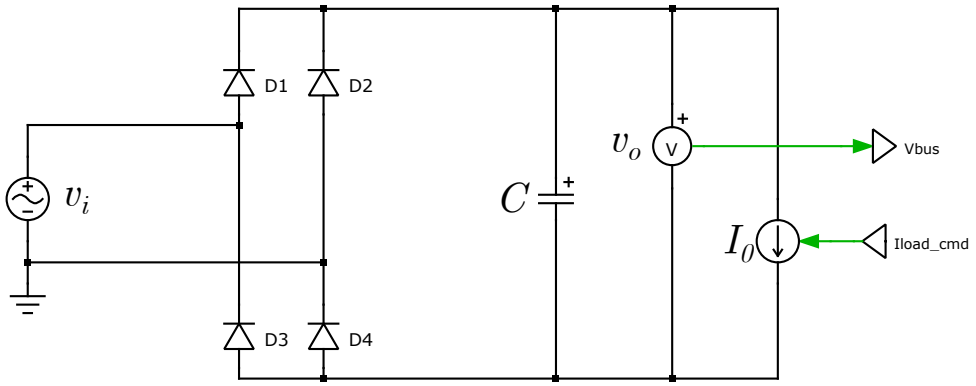


Figure 2.1: Schematic of the uncontrolled rectifier without inductor, used for the simplified computation of the capacitance requirements.

capacitor as a DC-link capacitor for PFC.

2.1.1 Uncontrolled Rectifier and its Limitations

In this first part of the study, the simple uncontrolled rectifier of Fig. 2.1 is studied to find the relationship between the load and the required capacitance. We study this system because the resulting relationship is the same for the sizing of the boost PFC converter, that will in turn share the same issues. PF computation is outside the scope of the present discussion, and it will be covered thoroughly in Chapter 2.1.3.

For this study, the rectified waveform is analyzed in Fig. 2.2. Here a sinusoid $v_i(t) = V_i \cos(\omega t)$ with amplitude V_i and angular frequency ω is assumed as the input to the rectifier, and v_o is the output of the circuit. In Fig. 2.1, C is the capacitance to be designed and the load is assumed to be a constant current load I_0: this is not exactly correct for current-controlled drives, which behave more as a constant power load; a more accurate model is given in the numerical simulations of Chapter 2.1.3.

The normalized variables of Fig. 2.2 are $y = v_o/V_i$ and $x = \omega t/\pi$. The load current is supplied by the capacitor when all the diodes are off. This happens for

$$C\frac{\mathrm{d}v_o}{\mathrm{d}t} = -I_0 \tag{2.1}$$

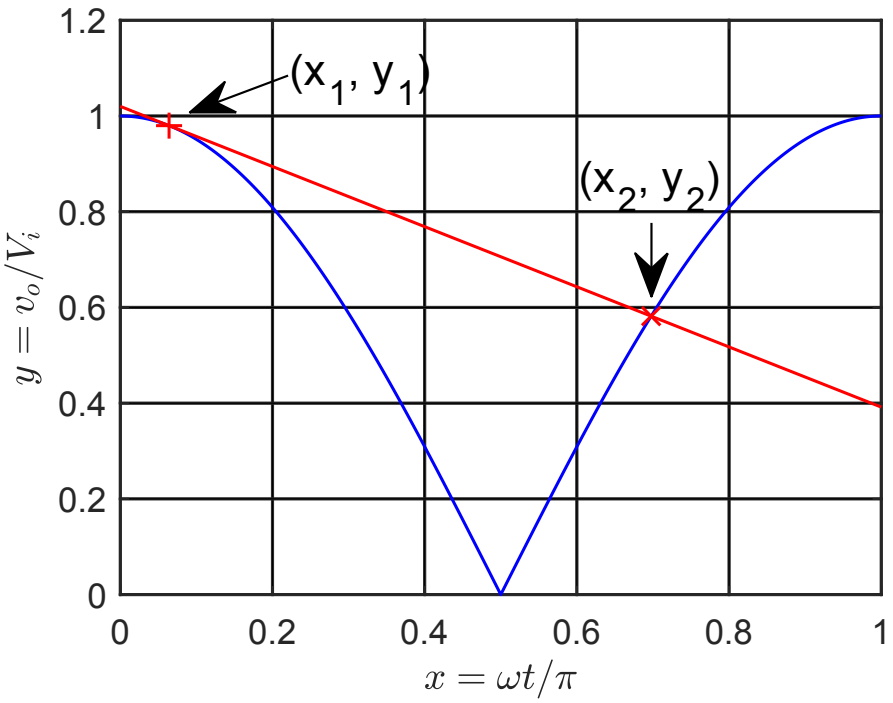


Figure 2.2: Normalized waveforms of the uncontrolled rectifier, used for the analysis of the capacitance requirements.

Because of the shape of v_o, there is a lower bound on the capacitance value which guarantees that (2.1) is satisfied for a normalized time $x < 1/2$:

$$C > C_{\min} = \frac{I_0}{\omega V_i} \tag{2.2}$$

we subsequently use this normalization constant in the following: $c = C/C_{\min}$. If (2.2) holds, then it is possible to determine x_1, the point where the diodes stop conducting, as

$$x_1 = \frac{1}{\pi} \arcsin\left(\frac{1}{c}\right) \approx \frac{1}{\pi c} \tag{2.3}$$

We can then compute the value at which the capacitor starts discharging:

$$y_1 = \cos(\pi x_1) = \sqrt{1 - \frac{1}{c^2}} \approx 1 - \frac{1}{c^2} \tag{2.4}$$

In both the formulas above, the approximations hold for $c \gg 1$, which is usually a practical design condition. By considering the capacitor discharge, we find the moment x_2 at which the diodes turn on again by solving:

$$\frac{\pi}{c}(x_2 - x_1) - y_1 = \cos(\pi x_2) \tag{2.5}$$

which is a transcendental equation and requires numerical solving. We can still give a quite accurate estimation by using the first-order Taylor expression for the cosine around $x = 3/4$, which is halfway in the range where the solution x_2 is expected to fall:

$$x_2 \approx \frac{\sqrt{2}/c + \sqrt{2}\sqrt{c^2 - 1} + c(3\pi/4 - 1)}{\pi(c + \sqrt{2})} \approx \frac{\mathrm{e}c}{\pi(c + \sqrt{2})} \tag{2.6}$$

where e is the Nepero constant, that appears as an unexpected approximation of the numerator coefficient in (2.6). We can then find the value y_2 and subsequently the voltage peak-to-peak ripple $\tilde{y}$ and the average voltage $\bar{y}$ at the output of the rectifier:

$$y_2 = y_1 - \frac{\pi}{c}(x_2 - x_1) \approx 1 - \frac{\mathrm{e}}{c + \sqrt{2}} \tag{2.7}$$

$$\tilde{y} = 1 - y_2 \approx \frac{\mathrm{e}}{c + \sqrt{2}} \tag{2.8}$$

$$\bar{y} = \frac{1 + y_2}{2} \approx \frac{c}{c + \sqrt{2}} \tag{2.9}$$

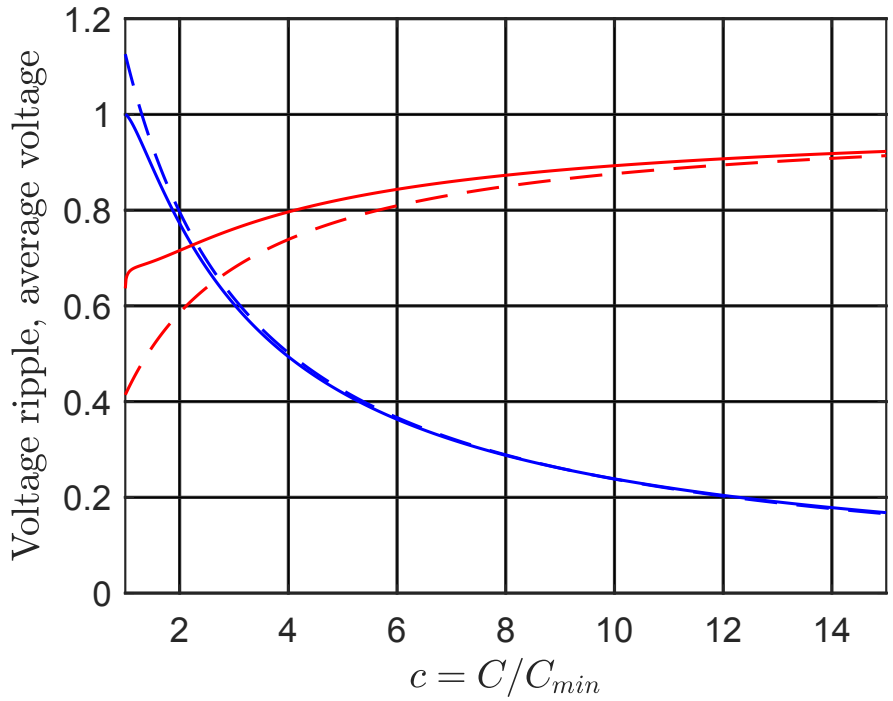


Figure 2.3: Normalized design quantities for the capacitor-only rectifier. The capacitor's average voltage is in red, while the voltage ripple is in blue. Exact results based on numerical solution are solid, while dashed lines pertain to the approximations used for the design and described above.

In (2.8) and (2.9) clearly show that the higher c is the best, yet there is an asymptotic behavior which discourages the use of very high values of C. Nonetheless, the application will pose constraints on $\tilde{y}$ and $\bar{y}$, so these will be used for sizing C. Fig. 2.3 reports all the aforementioned quantities in normalized units, with both the numerical results and the given approximations. It can be seen that the average output voltage in case of $C < C_{\text{min}}$ is $2/\pi$, as it results from straightforward averaging of the rectified cosine.

2.1.2 Proposed Control for DC Link Capacitance Reduction

PFC is a primary practice for AC-DC converters in order to fulfill the requirements of grid codes. PFC will reduce THD in the supply current and boost the efficiency of the system. Even though numerous methods have been suggested to improve power factor, the proposed method is based on a boost PFC Circuit as presented in [34] and with a novel control algorithm, described in this chapter. This control method has two fundamental aims, decrease the front end capacitor to achieve an electrolytic capacitor-less circuit keeping at the same time high PF. To do so, a new control method has been built based on the summation of two distinct duty cycle components:

1. Feed-forward control: Boost converter can work in two distinct modes, Continuous Conduction mode (CCM) and Discontinuous Conduction mode (DCM) depending if the inductor current reaches zero during the switching period. The duty cycle definition is different in the two modes, once input and output voltage are chosen:

$$D_{CCM} = 1 - \frac{V_{in}}{V_{out}} \tag{2.10}$$

$$D_{DCM} = \sqrt{\frac{L}{2R_{out}T_{sw}}\left(\frac{V_{out}I_{out}}{V_{in}} - 1\right)^2 - 1} \tag{2.11}$$

   CCM control methods are more commonly used given their simplicity, however in variable load applications, DCM may occur changing the duty cycle relationship.

2. Feed-back control: a dual nested loop linear feedback control is implemented for parameter adaption and to improve load and line regulation. The inner current loop generates the duty cycle to control (and limit) the inductor current; the outer voltage loop generates a current setpoint to regulate the voltage of the DC link to the desired value, while minimizing the ripple.

The most noteworthy design choice in this control architecture is based on the trade-off between ripple output voltage and peak inductor current. To achieve the

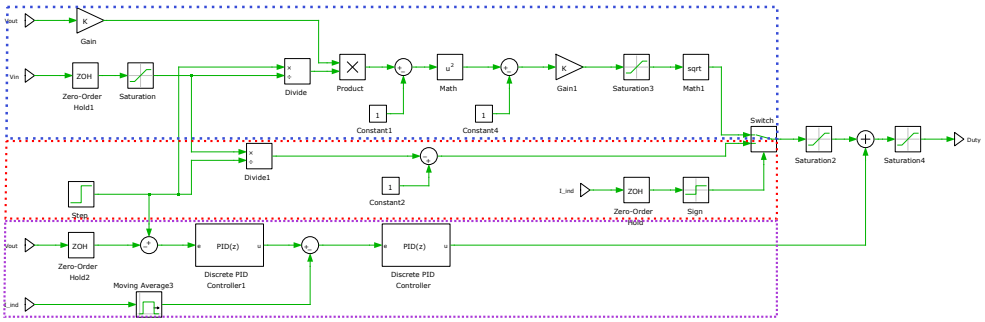


Figure 2.4: Schematic of the control algorithm for the boost front-end with capacitor-reduction action. Three control branches can be recognized: feed-forward for CCM highlighted in red, feed-forward for DCM, highlighted in blue and linear feedback control with inner inductor current loop and outer voltage loop, highlighted in purple. V_{in} is the input voltage after the rectifier, V_{out} is the DC output voltage,I_{ind} is the inductor current.

proper boost gain in the full rectified line period, high duty cycle values must be used, which correspond to high inductor current values. Limiting the inductor current, particularly in an electrolytic-capacitor-less design, will negatively impact the output voltage ripple, since the control will not operate in closed loop conditions on the whole period.

2.1.3 Comparison of Different Rectifier Topologies

To maximize the benefits of the control described in Chapter 2.1 and to properly choose the most appropriate rectifier front-end depending on the specific application, five different rectifier topologies are compared by simulation in this section:

1. Regular capacitor
2. Regular capacitor and inductor on DC side
3. Regular capacitor and inductor on AC side
4. Regular capacitor and boost PFC

5. Reduced capacitor and boost converter for PF limit

They are compared according to several metrics. From the functional point of view, DC voltage average value and peak-to-peak ripple are evaluated, as well as the power factor. Particularly, the latter is split in three components: one which is phase-shift related, and other two which are related to the distortion of both current and voltage. When an AC voltage $v(t)$ is applied to a non-linear load (such as the rectifier bridge), the current $i(t)$ may contain relevant harmonic components. We can express both quantities in terms of Fourier series:

$$v(t) = V_0 + \sum_{n=1}^{\infty} V_n \cos(n\omega t + \varphi_{vn}) \tag{2.12}$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega t + \varphi_{in}) \tag{2.13}$$

hwere V_n and I_n are the peak values. The active power P can thus be computed by its definition, as the average of the instantaneous power $p(t)$:

$$\begin{aligned} P &= \frac{1}{T}\int_T p(t)\,\mathrm{d}t = \frac{1}{T}\int_T v(t)i(t)\,\mathrm{d}t = \\ &= V_0 I_0 + \frac{V_1 I_1}{2}\cos(\varphi_{v1} - \varphi_{i1}) + \sum_{n=2}^{\infty}\frac{V_n I_n}{2}\cos(\varphi_{vn} - \varphi_{in}) \end{aligned} \tag{2.14}$$

Where the first term is the DC power, which is supposed to be zero, the second term is the fundamental frequency power (the desired one) and the last term is the higher-harmonics related power (which is undesirable and cannot be exploited practically in most applications). Considering that for any signal $x(t)$ we can express its RMS and THD values respectively as

$$X_{rms}^2 = \frac{1}{T}\int_T x^2(t)\,\mathrm{d}t = X_0^2 + \sum_{n=1}^{\infty}\frac{X_n^2}{2} = X_0^2 + X_{1,rms}^2 + \sum_{n=2}^{\infty} X_{n,rms}^2 \tag{2.15}$$

$$\mathrm{THD}_x = \frac{1}{X_1}\sqrt{\sum_{n=2}^{\infty} X_n^2} = \frac{1}{X_{1,rms}}\sqrt{\sum_{n=2}^{\infty} X_{n,rms}^2} = \sqrt{\frac{X_{rms}^2}{X_{1,rms}^2} - 1} \tag{2.16}$$

where $X_{n,rms} = X_n/\sqrt{2}$ are the RMS values of the harmonics. We can now express the active power as a function of RMS values, phase-related power factor $\mathrm{PF}_\varphi =$

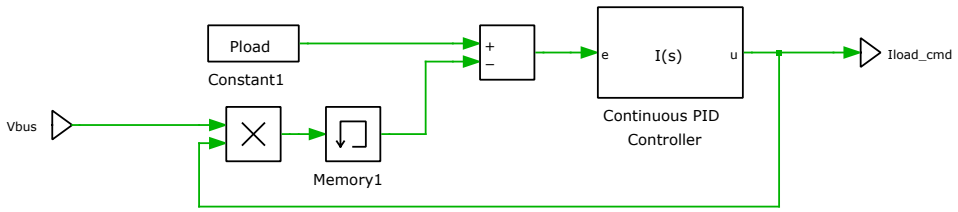


Figure 2.5: The simple control used to compare all the simulations with constant power output, regardless of the effective DC link voltage achieved by each uncontrolled topology.

$\cos(\varphi_{v1} - \varphi_{i1})$ and the two distortion-related power factors PF_{Dv} and PF_{Di}

$$P = V_{rms} I_{rms} \mathrm{PF}_{\varphi} \sqrt{\frac{1}{1+\mathrm{THD}_v^2}} \sqrt{\frac{1}{1+\mathrm{THD}_i^2}} = \\ = V_{rms} I_{rms} \mathrm{PF}_{\varphi} \mathrm{PF}_{Dv} \mathrm{PF}_{Di} = V_{rms} I_{rms} \mathrm{PF} \tag{2.17}$$

In the simulations used here, we assume $\mathrm{THD}_v = 1$, i.e. $\mathrm{PF}_{Dv} = 1$, assuming that the AC source has a very low impedance and is insensitive to current distortion: this is somehow a best case, but it still gives a fair comparison of the various topologies.

To ensure fairness with respect to the drive application the grid front-end is supposed to work with, all the circuits are evaluated at the same output power. This is slightly different from the usual constant current model of the load (see an example in Chapter 2.1.1), but it best describes the load presented by the torque- and speed-controlled drive, which will require more current in case of lower DC voltage, provided that there is still some voltage margin. This descends from the fact that a torque set-point at any given speed gives an output mechanical power, hence a similar power (increased by the motor inverter loss) will be requested to the upfront converter. To model this type of load, a linear, integrator-based control is introduced: Fig. 2.5 shows the control, where V_{bus} is the DC link voltage and $I_{\mathrm{load,cmd}}$ is the command of the dependent current generator acting as load at each rectifier output.

Besides these functional parameters, the circuits are evaluated also with respect to some relevant implementation parameters: size of inductor, capacitor and inductor RMS current, total power factor (combining phase displacement and distortion

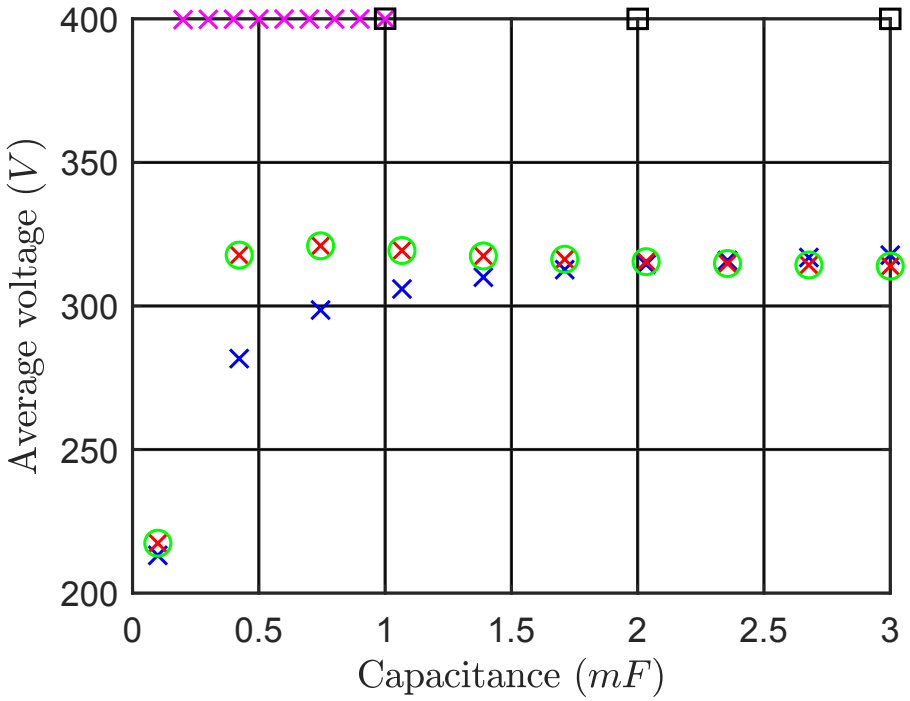


Figure 2.6: Average output voltage comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

on the current). The size of the inductor is obtained by computing the maximum stored energy and normalizing it with respect to the (constant) power load (as done in [79]), thus giving an effective "time of load supply". This enables understanding how the energy is stored into the various components and justifies that this quantity is expressed in time units (milliseconds), as resulting by dividing energy by power.

The aforementioned indexes are given from Fig. 2.6 to Fig. 2.11. The magenta points, representing the reduced capacitor rectifier, are computed on a narrower capacitance range, since this rectifier is supposed to be used with small capacitance

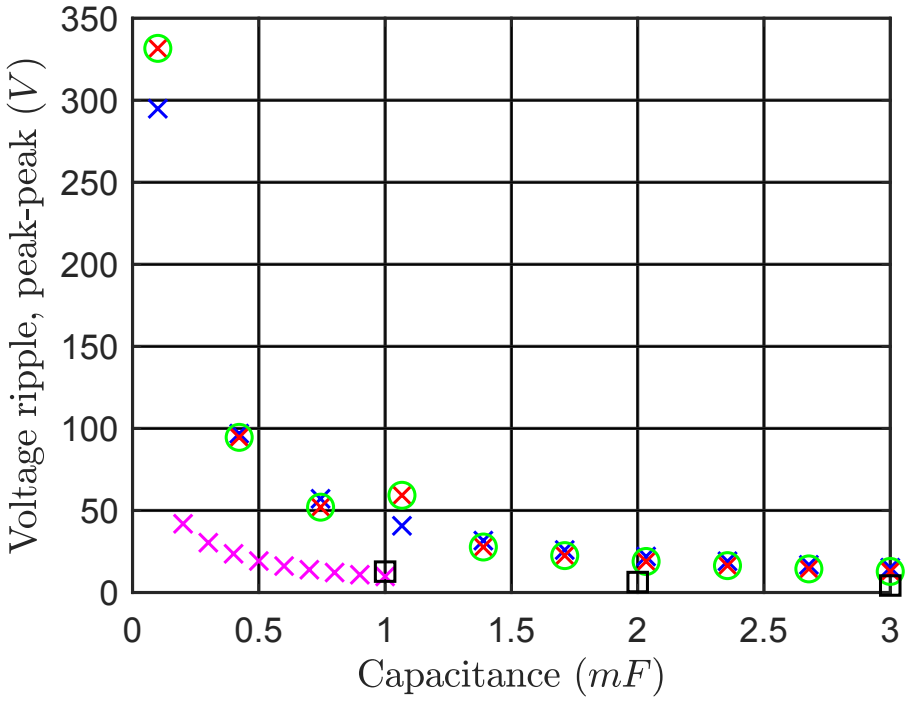


Figure 2.7: Output voltage ripple comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

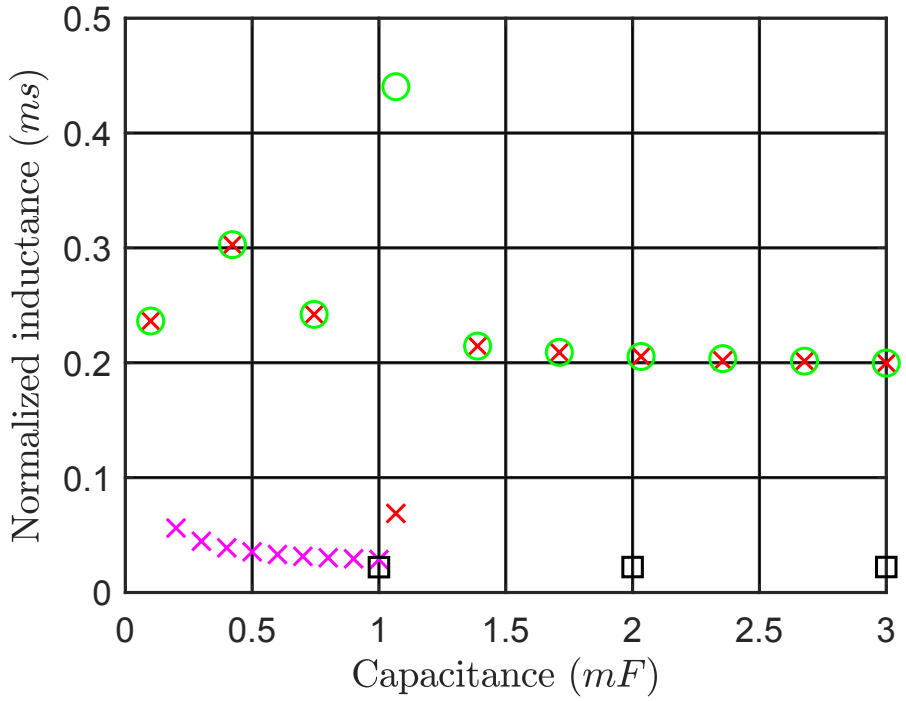


Figure 2.8: Normalized inductance value comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

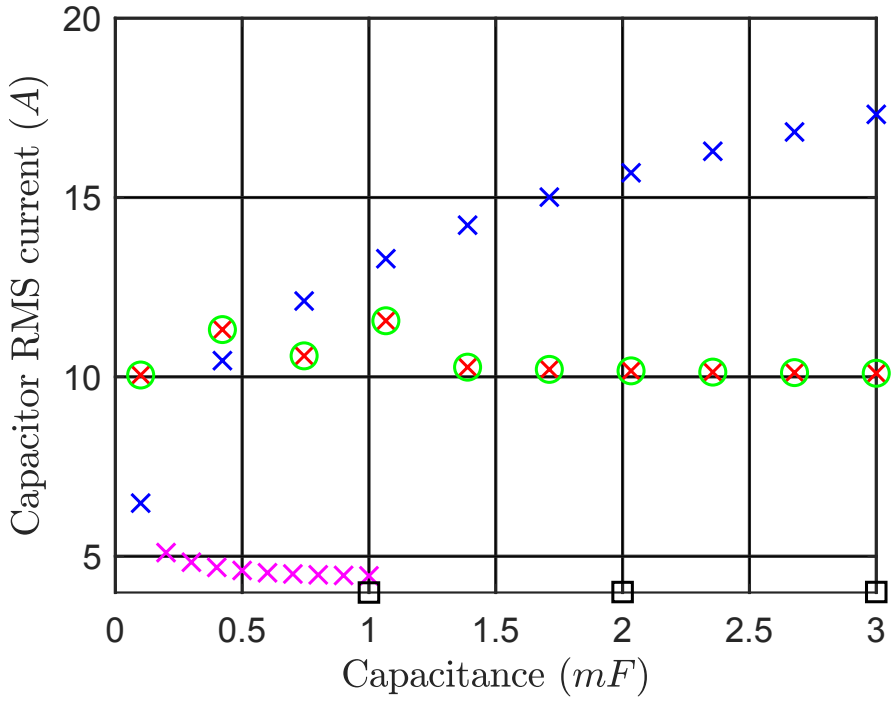


Figure 2.9: Capacitor RMS current comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

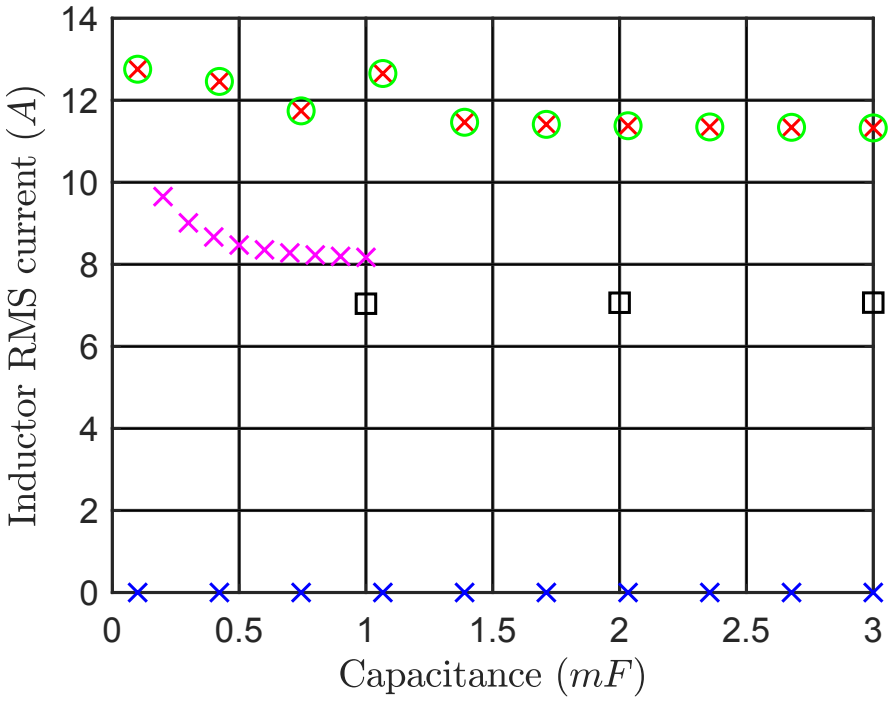


Figure 2.10: Inductor RMS current comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

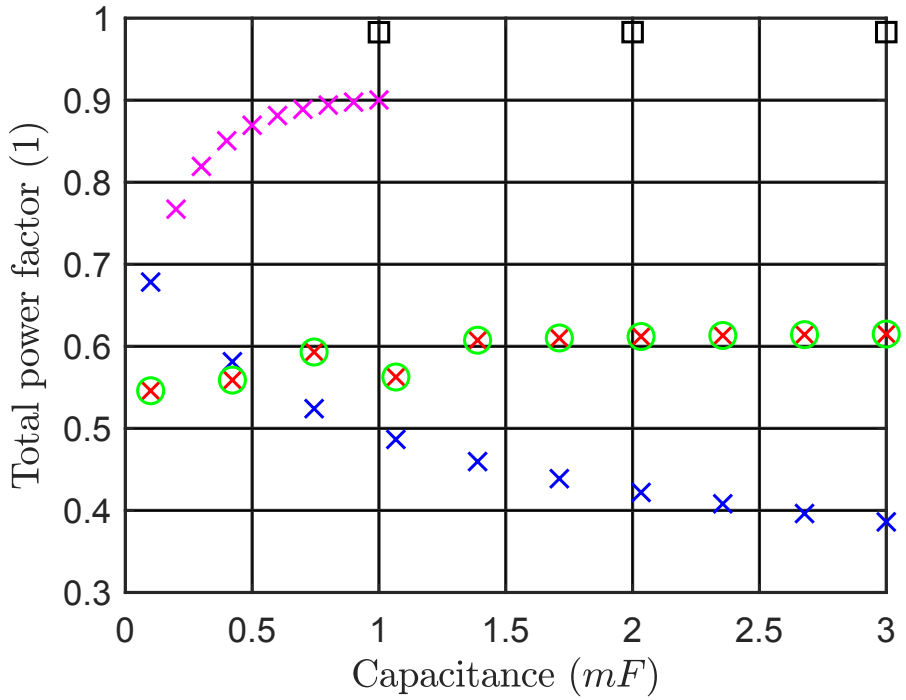


Figure 2.11: Overall power factor (phase and harmonics) comparison of the five different models. Results are presented for the uncontrolled rectifier with capacitor only (blue), rectifier with AC-side inductor (red), rectifier with DC-side inductor (green), boost front-end with reduced-capacitor control (magenta), boost PFC (black squares).

values. According to the boost nature of the front-end, the output voltage is controlled (in this case) at 400 V, with a very small ripple ($< 10\%$) also for capacitor values of 200 µF, for a 1.6 kW load power and an inductance value of 600 µH. It is interesting to see (Fig. 2.8) that, even if the inductance has the same value as in uncontrolled designs, the normalized size of this component is smaller, due to the lower RMS current.

Fig. 2.11 shows an interesting feature of the presented control: even if the overall PF is not addressed directly by the control, the performance of the converter under this aspect is absolutely remarkable. However, unity power factor cannot be reached, as the curve appears to reach an asymptote around 0.9.

The "traditional" boost PFC has similar performance to the proposed circuit, when properly sized, it achieves almost unity power factor; however it cannot operate in the full capacitance range, since its control is based on the hypothesis of a virtual resistive output load, which fails with low capacitance [34]. The small discrepancy in PF in this case is related to the residual THD of the current (connected to the inductor current ripple): the phase related component is, however, exactly unity.

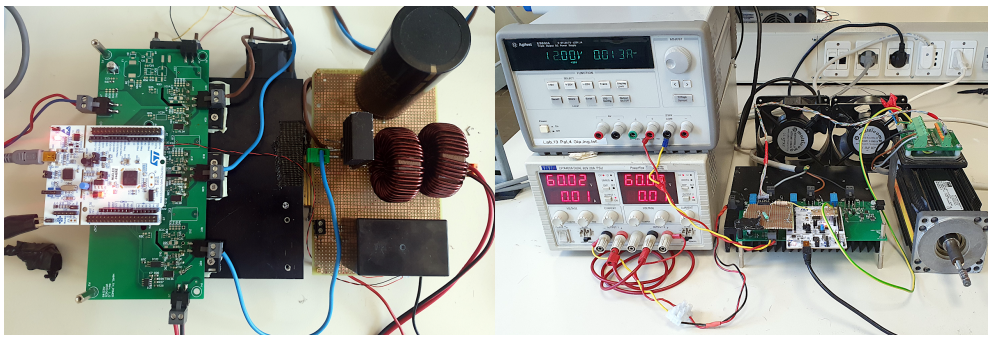
Lastly, it can be noted that when using a passive topology with inductor, putting it on the AC or DC side does not affect the performance, as it may be arguable by the behavior of an ideal rectifier.

2.2 Experimental Results

2.2.1 Boost Front-end with Film Capacitor

The boost converter with reduced DC link capacitance is firstly tested in a standalone fashion, with a purely resistive load. Fig. 2.12a represents the test bench used to gather the results. The boost front-end parameters are summarized by Table 2.1.

As shown in Fig. 2.13, the boost PFC converter with reduced DC link capacitance works as expected, achieving an high PF (> 0.75, depending on control parameters), comparable to the simulations shown in Fig. 2.11 with low capacitance. The output voltage ripple is high (≈ 45 V) but still compatible to the simulations results in Fig. 2.7 with low capacitance. An important aspect to highlight is the trade off



(a) (b)

Figure 2.12: The two test benches used to test the electrolytic capacitor-less drive: (a) the rectifier stage, (b) the three-phase motor drive stage.

Table 2.1: The boost converter parameters.

Parameter	Symbol	Value
Input voltage (Peak)	v_i	125 V
Input frequency	f_0	50 Hz
Output voltage	v_o	150 V
Inductance	L	610 µH
Capacitance	C	110 µF
Resistive load	R_o	100 Ω

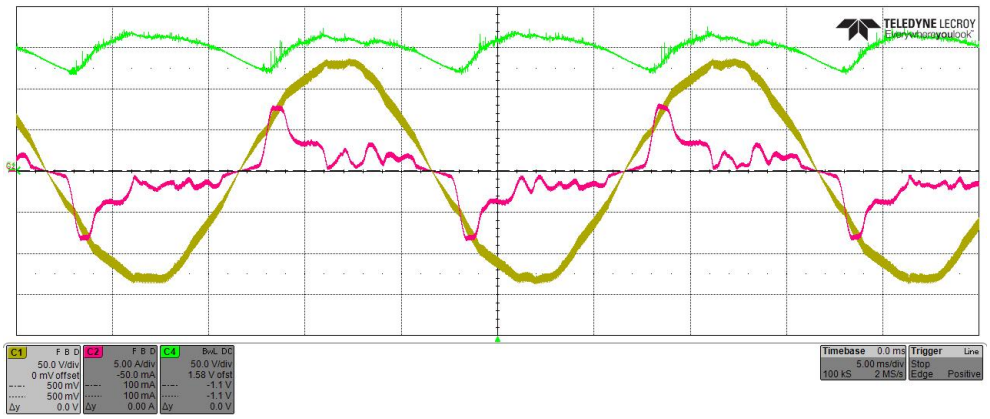


Figure 2.13: Capacitor-less PFC test conducted using the parameters summarized in Table 2.1: Input voltage (Yellow), Input current (Magenta), Output voltage (Green).

between PF, inductor peak current and output voltage ripple depending on the PID tuning. Different results can be achieved with the possibility of optimizing one parameter to the detriment of the others, resulting in a critical challenge in PFC design.

Once the proposed DC link voltage control is validated on its own, it is coupled with a conventional, resolver-based three-phase drive for PMSM; the drive test bench is represented in Fig. 2.12b. The drive parameters are given in Table 2.2.

2.2.2 System Performance in Regenerative Conditions

To analyze the regenerative braking process, the proposed PFC boost converter front-end is coupled with a full bridge inverter PMSM controller. According to Fig. 2.14, motor is spinning at $100\,\mathrm{rad\,s^{-1}}$ and the voltage of the DC link is set to 150 V. At a certain time, a braking signal has been applied to the rotor to reach zero speed and stop. During deceleration in regenerative braking period, negative q-axis current is being generated flowing into DC link capacitor and charging it up to 90 V. After almost 500 ms, reference speed has been changed into $100\,\mathrm{rad\,s^{-1}}$ again, so the motor begin accelerating to reach steady state in almost 250 ms. Based on practical results shown in Fig. 2.14, during the charge and discharge time, DC link voltage ripple has been controlled with appropriate performance.

Table 2.2: The drive parameters.

Parameter	Symbol	Value
Motor rated torque	T_n	2.2 N m
Motor rated speed	ω_n	1000 rpm
Motor rated power	P_n	230 W
Motor rated current (phase, RMS)	I_n	2.42 A
Motor rated voltage (LL, RMS)	V_n	380 V

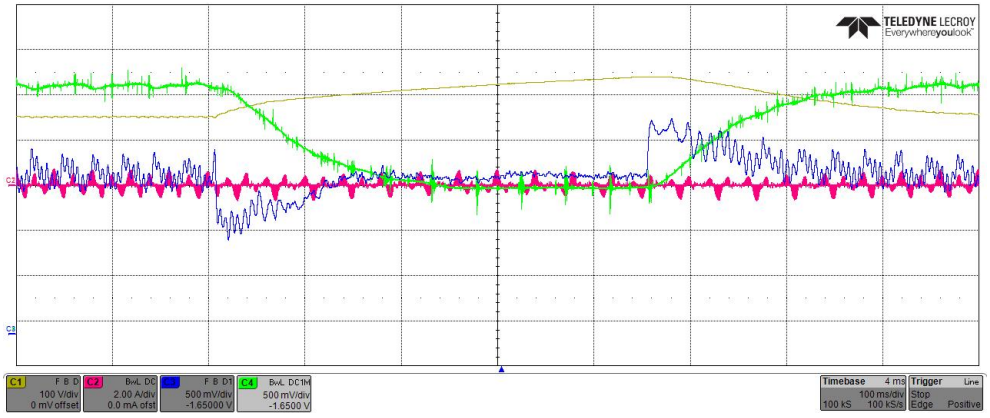


Figure 2.14: Regenerative Braking Test: Input DC voltage of inverter (yellow), Input current of the boost PFC (magenta), Q-axis current of the motor from DAC scaled to 0.15 A per division on the oscilloscope with 1.65 V offset to show negative and positive current(blue), Motor speed scaled to 55 rad s^{-1} per division on the oscilloscope with 1.65 V offset to show negative and positive speed(green).

2.3 General Model

The results that emerged in Chapter 2.2 are certainly promising, however, the performance deterioration of the new control, could detract from the benefits of using a film capacitor in terms of reliability. For this reason, it was necessary to develop a model capable of estimating the life time of a film capacitor and an electrolytic one subjected for long times to different stresses caused by the different controls. In order to determine capacitor lifetime, several steps are required; As shown in Fig. 2.15, the power loss on the capacitor (P_{loss}) is derived from the electric model and consequently it is possible to achieve the hotspot temperature (T_{HS}) from the thermal model. Knowing all the T_{HS} during the full working period, the capacitor's lifespan (L_x) can be estimated from lifetime model and Montecarlo analysis.

2.3.1 Electric Model

First of all, the capacitors have been evaluated for the two methodologies from commercial products. The sizing has been done to obtain an average voltage $v_o = 400\,\mathrm{V}$ from a peak input voltage $v_{i_{pk}} = 325\,\mathrm{V}$.

Table 2.3 summarizes the main characteristics taken from the data-sheet for E-Cap (B43514C5108M000) [80] and F-Cap (C4AQGEW6210P3BK) [81], where v_n is defined as the capacitor DC nominal voltage. Depending on manufacturer definition, v_n may be assumed as absolute maximum rating which is supposed not to be overtaken or the nominal voltage at which the capacitor should operate with a certain ripple. In this last case, v_n corresponds to the maximum voltage that can be reached by the ripple, i.e., the peak voltage, and v_r is the nominal average voltage. C is the

Table 2.3: Capacitors parameters from data-sheet

	C (µF)	v_n (V)	v_r (V)	R_{ESR} (mΩ)	R_θ (°C/W)
E-Cap	1000	450	405	100	7.2
F-Cap	210	450	405	5	7

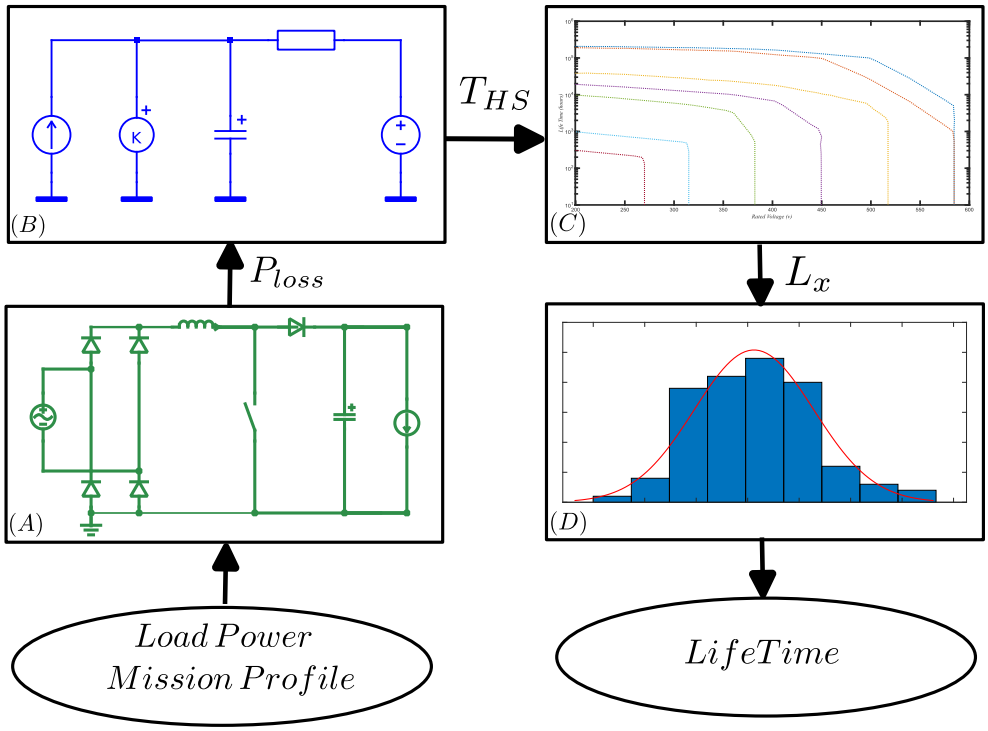


Figure 2.15: Diagram representing the workflow for lifetime estimation: (A) Electric Model; (B) Thermal Model; (C) Lifetime Estimation; (D) Montecarlo Analysis.

capacitance value chosen to obtain a comparable volume with the smallest capacitance decrement of F-Cap at the same v_n. The equivalent series resistance (R_{ESR}) is frequency dependent and is defined at $f_0 = 100\,\text{Hz}$.

To evaluate a feasible scenario, a variable industrial load in [82] was assessed, and post-processed by reducing the number of possible power demand states, while achieving a high load excursion during the day and remaining unused for eight hours at night as shown in Fig. 2.16.

The control methods defined in Chapter 2.1 are evaluated where the "traditional" PFC control is coupled with the E-Cap and the novel control is coupled with the F-Cap. The simulation results in Fig. 2.17 and 2.18 exhibit the maximum and minimum load scenarios, and all other loads fall between these two. As shown in Fig. 2.17 it is clear that the output voltage ripple in F-Cap PFC is higher, however, even in the worst situation it respects the boundaries recommended by data-sheet summarized in Table 2.3. According to Fig. 2.18, it is possible to estimate the PF, which results $PF_E \approx 1$ in case of E-Cap PFC and $PF_F \approx 0.91$ in case of F-Cap PFC. This reduction in PF will result in an increment in current on the switching device.

By adopting a power MOSFET (IXFH78N60X3) [83] as a switching device, it is possible to evaluate the conduction current as shown in Fig. 2.19. The decrement in PF results in a current increase of 7.86%, which augments the conduction power losses by 16.3%. The power loss on the capacitors (P_{loss}) at different loads can be found as follow:

$$P_{loss} = i_C^2 R_{ESR} \tag{2.18}$$

Table 2.4: Proportional and Integral gain values used for the two different PFC control strategies defined in Chapter 2.1.

	Proportional gain	Integral gain
E-Cap PFC	$0.001\,(\text{S}/\text{V})$	$0.03\,(\text{S}/\text{Wb})$
F-Cap PFC inner loop	$0.05\,(\text{A}^{-1})$	$10\,(\text{C}^{-1})$
F-Cap PFC outer loop	$0.01\,(\text{S})$	$5\,(\text{A}/\text{Wb})$

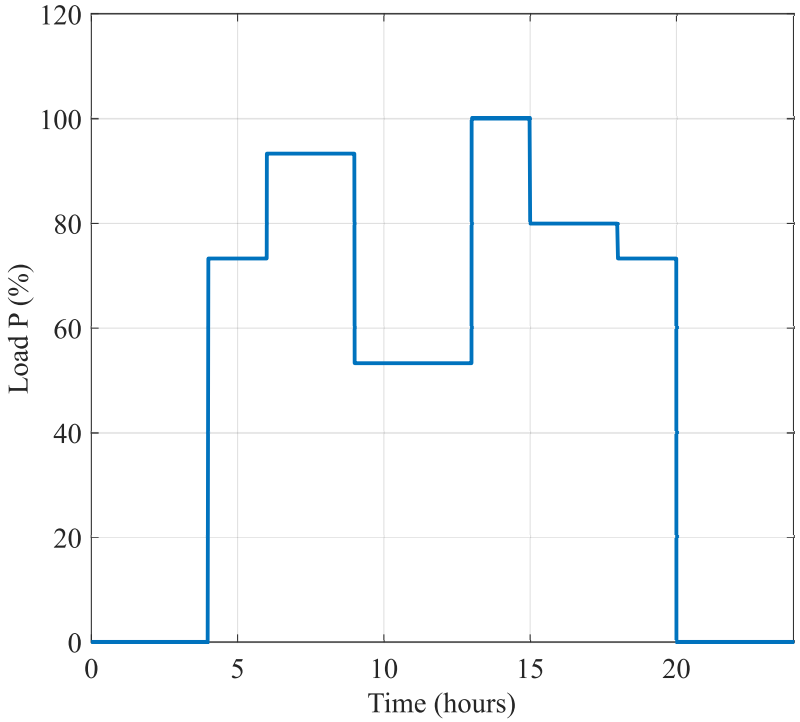


Figure 2.16: Mission profile of the converter, as load power demand during 24 hours with an interruption from 08:00 PM to 04:00 AM

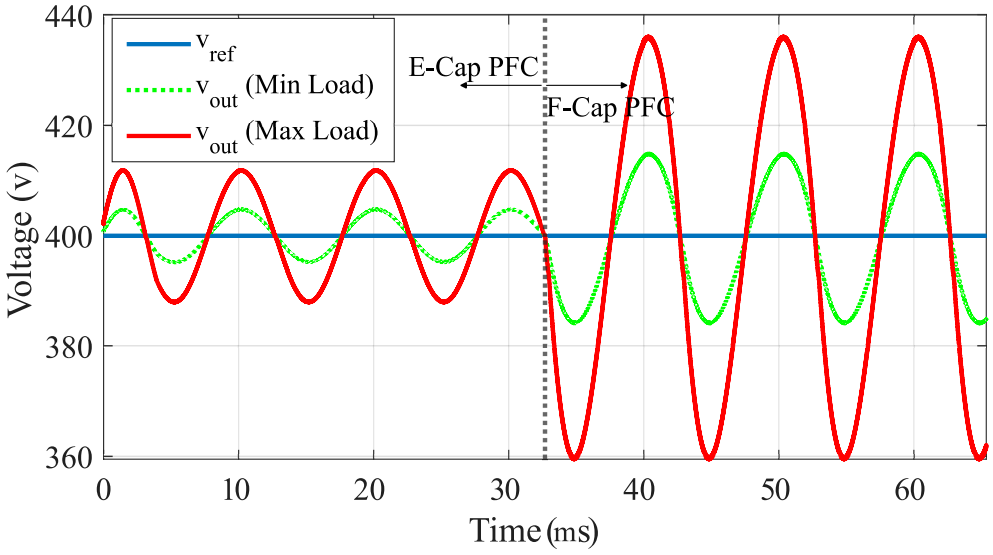


Figure 2.17: Output voltage comparison between E-Cap PFC and F-Cap PFC for maximum and minimum power load demand in steady state.

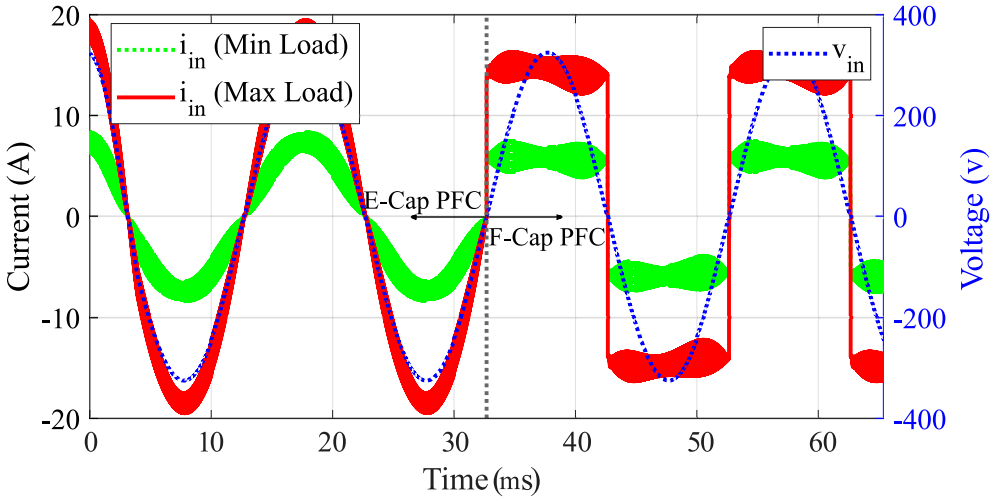


Figure 2.18: Input current and voltage comparison between E-Cap PFC and F-Cap PFC for maximum and minimum power load demand in steady state.

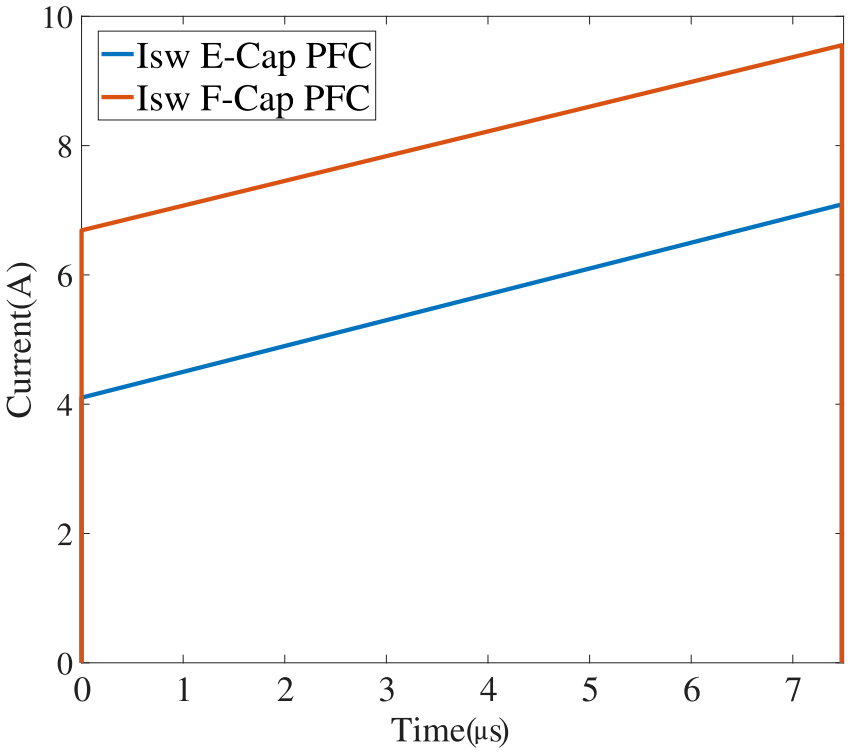


Figure 2.19: Conduction current on the switching power device using E-Cap PFC and F-Cap PFC.

where i_C is the current on the capacitor. According to [84], it is possible to define the R_{ESR} value as a function of frequency:

$$R_{ESR}(f_h) = A\,R_{ESR}(f_0)\left(\frac{1}{f_0} - \frac{1}{f_h}\right) \tag{2.19}$$

where $R_{ESR}(f_h)$ is defined in the range $f_h \in [10\text{Hz}; 100\text{kHz}]$ and $R_{ESR}(f_0)$ is generally provided by the manufacturer. A is the parameter determined by the capacitor type, which can be calculated using two different R_{ESR} at two distinct frequencies. In Fig. 2.20 the main i_C frequency components are identified, from which, it is possible to define P_{loss} as:

$$P_{loss} = \sum_{f_h} i_C(f_h)^2\,R_{ESR}(f_h) \tag{2.20}$$

2.3.2 Thermal Model

Applying P_{loss} calculated in the previous section, it is possible to obtain the temperature at its hottest point (T_{HS}) from the thermal network shown in Fig. 2.21, where R_θ is the thermal resistance defined in Table 2.3 and C_θ is the thermal capacitance which is usually not taken into account in data-sheets [80] and studies [84, 85]. However, in case of big capacitors, it must be considered [86]. T_{HS} can take up to hours to reach steady-state, impacting on lifetime. In this case of study the time constant $\tau = R_\theta\,C_\theta$ can be defined from a similar capacitor as $\tau_F = 2100\,\text{s}$ for F-Cap [87] and $\tau_E = 4000\,\text{s}$ for E-Cap [88]. From Fig. 2.21 the thermal differential equation is defined as:

$$\frac{dT_{HS}}{dt} + \frac{T_{HS}}{\tau} = \frac{R_\theta\,P_{loss}}{\tau} + \frac{T_{amb}}{\tau} \tag{2.21}$$

where T_{amb} is the ambient temperature, which varies daily during the year as shown in Fig. 2.24. Those data came from dataset [89] acquired in Basel (CH) during 2022. These data were post-processed with a constant temperature increment to simulate an enclosed working environment condition. Equation 2.21 is a simple first-order Ordinary Differential Equation (ODE), that can be straightforwardly solved using a Backward Euler approach. In order to evaluate the contribution of P_{loss} alone it is possible to exclude T_{amb} from the equation maintaining an error lower than 100 ppm,

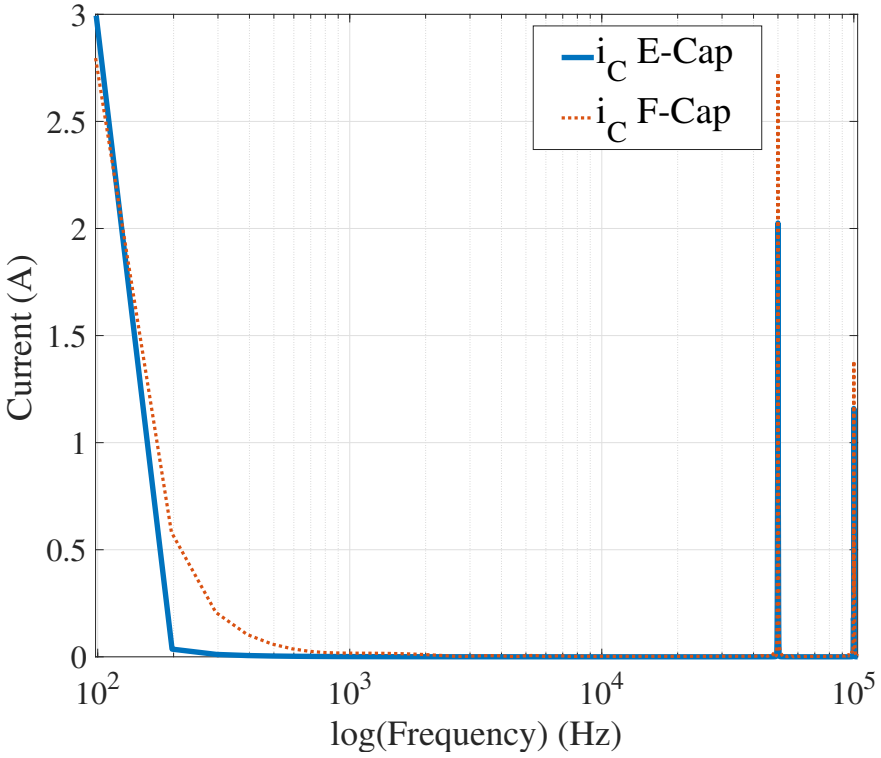


Figure 2.20: Capacitor current FFT for E-Cap PFC and F-Cap PFC. The main frequency components turn out to be at the fundamental frequency $f_0 = 100$Hz and at the switching frequency $f_{sw} = 50$kHz.

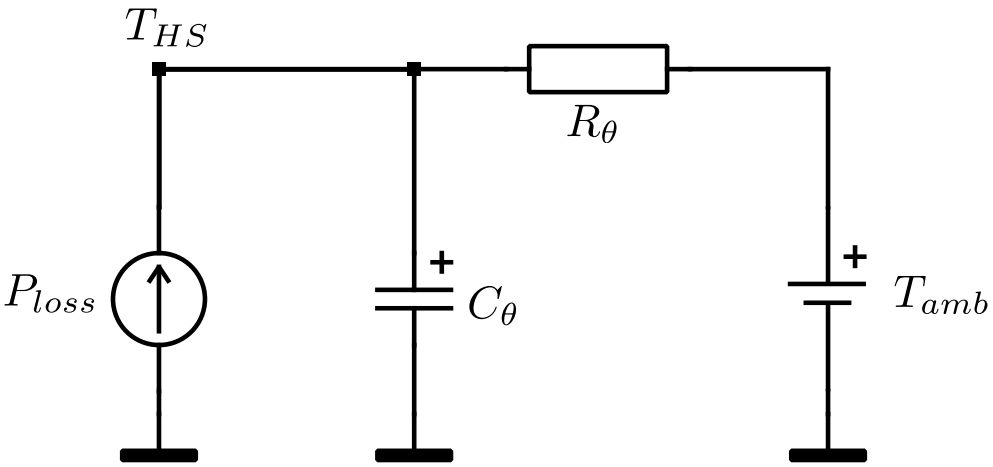


Figure 2.21: Capacitor thermal model based on first-order thermal Cauer network with thermal resistance extracted from data-sheets and thermal capacitance derived from similar capacitors.

resulting in:

$$\Delta T_n = \frac{\Delta t\, R_\theta\, P_{loss_n}}{\Delta t + \tau} + \frac{\tau\, \Delta T_{n-1}}{\Delta t + \tau} \tag{2.22}$$

where $\Delta t = 1$ s is the time step of the simulation. Regardless of T_{amb}, the temperature response ΔT for F-Cap and E-Cap are shown in Fig. 2.22 and 2.23, respectively. The daily ΔT profile is repeated for one year by applying the daily T_{amb} through the year, obtaining the annual temperature profile as:

$$T_{HS} = \Delta T + T_{amb} \tag{2.23}$$

2.3.3 Lifetime Estimation

Lifetime estimation based on thermal analysis of capacitors is imperative in assessing their reliability. The estimated lifespan of a capacitor is primarily influenced by T_{HS} [90]. It is generally assumed that the capacitor lifespan L_x is halved for every ten-degree rise in T_{HS}:

$$L_x = L_n 2^{(T_n - T_{HS})/10} \left(\frac{v_o}{v_r}\right)^{-n} \tag{2.24}$$

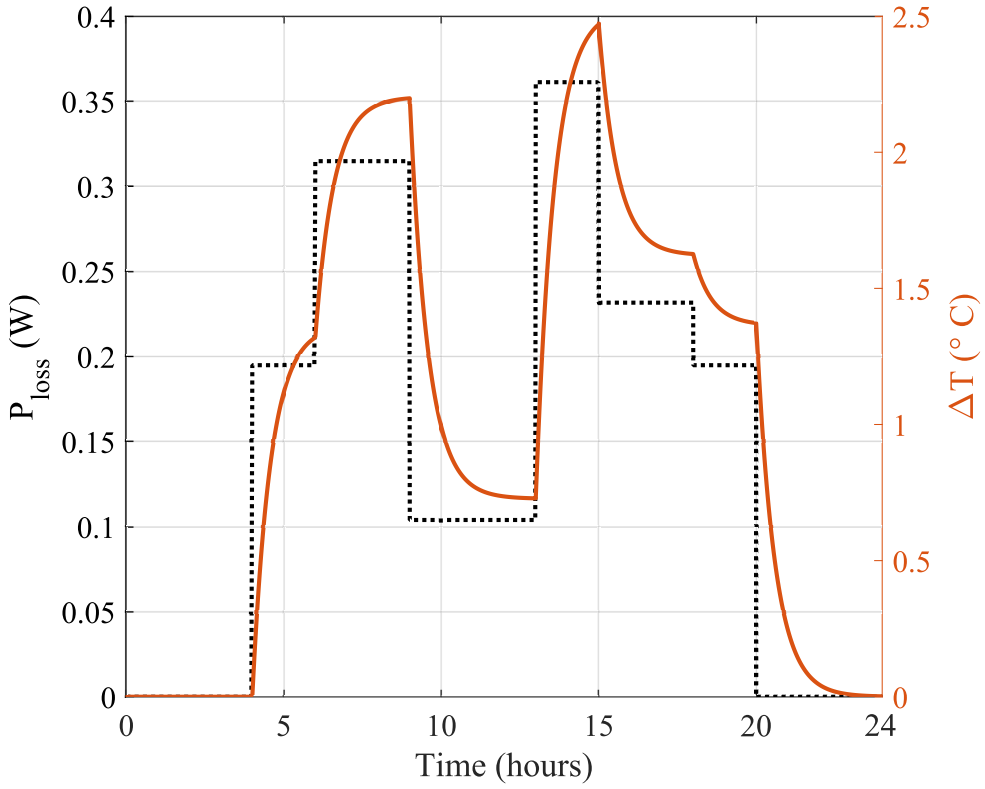


Figure 2.22: Power Loss (Black) and temperature variation (Orange) during the daily mission profile of Film Capacitor.

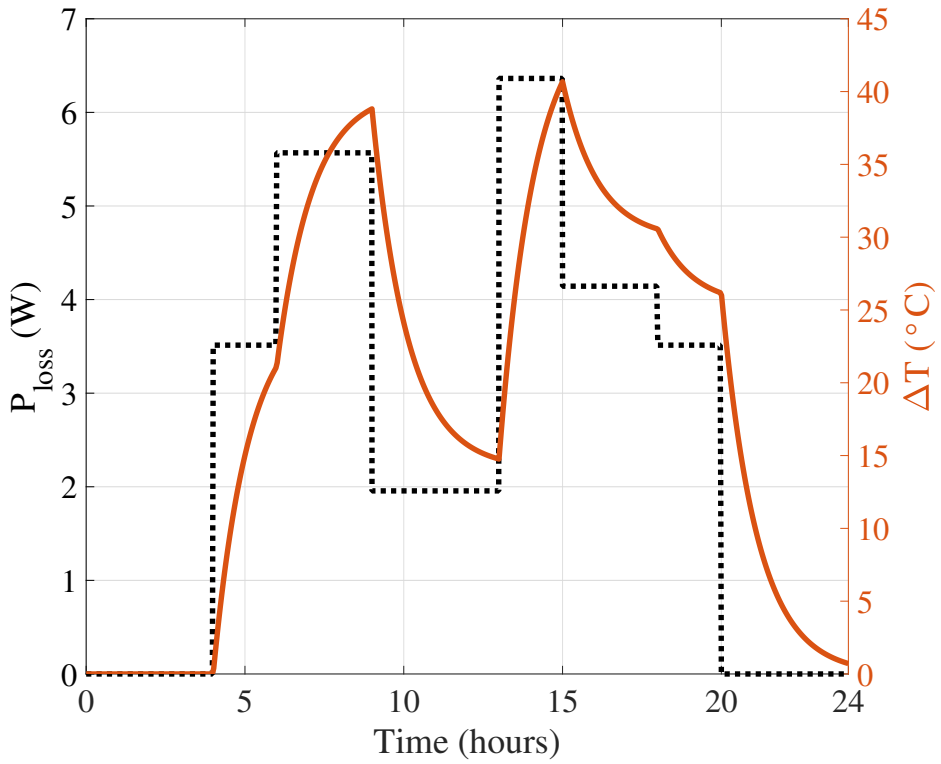


Figure 2.23: Power Loss (Black) and temperature variation (Orange) during the daily mission profile of Electrolytic Capacitor.

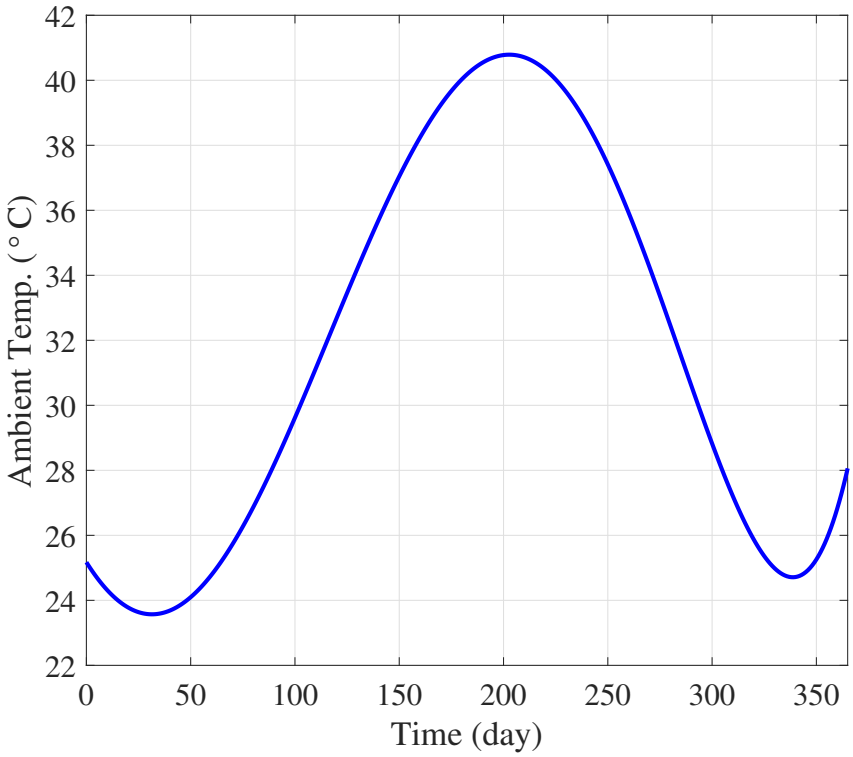


Figure 2.24: Ambient temperature of Basel (CH) in 2022; Post-processed to simulate an enclosed working environment condition.

where L_n is the reference lifetime achieved at temperature T_n defined in data-sheet. In this study, for F-Cap, $L_n = 100000$ hours at $T_n = 70°\text{C}$ and for E-Cap, $L_n = 200000$ hours at $T_n = 40°\text{C}$ [80, 81]. The expression v_o/v_r is the ratio between nominal and operating voltage, and n is the voltage coefficient. The lifetime dependency described by (2.24) does not describe well the behavior of Film capacitors since humidity dependency is not characterized and temperature dependency does not totally match [42]; However this model is generally utilized for both Film and Electrolytic capacitor types [90–93]. For this study, the two models are assumed to be the same. In Fig. 2.25, the reference lifetime curves are represented with dotted lines, extracted from F-Cap data-sheet [81]. Those curves are typically used to define capacitor lifetime based on (2.24). However, as shown with the hexagram lines, this can be true in only one region of the model. Ignoring the dependency of n on v_o/v_r and T_{HS}, assuming it as constant as generally assumed [84, 94], might result in overestimating L_x. From the fitted model, two diagonal blue and orange dashed lines have been defined depending on the intersection points of the different fitted lines for various temperatures. Consequently, three operative regions have been characterized. Those fitted curves have been appropriately scaled to an equivalent model based on E-Cap lifetime data reported on the data-sheet [80]. There are more comprehensive lifetime models that describe the voltage ripple component [84], however, the characterization of additional parameters is not trivial and is not evaluated in the data-sheets. Moreover, as described in [95], if the peak voltage value does not exceed the nominal, as shown in Fig. 2.17, this model component is negligible. For those reasons the standard model (2.24) is adopted, and L_x is calculated from this model at different temperatures during the year. Each calculated lifetime defined in hours, gets normalized in seconds and then, the total amount of accumulated damage (AD) is determined by adding up the inverses of the normalized L_x during the year:

$$\text{AD} = \sum_{k=1}^{t_f} \frac{1}{L_{x_k}} \tag{2.25}$$

where t_f is the last second of the year. Finally, the reciprocal of the total AD corresponds to the total lifetime of the capacitor.

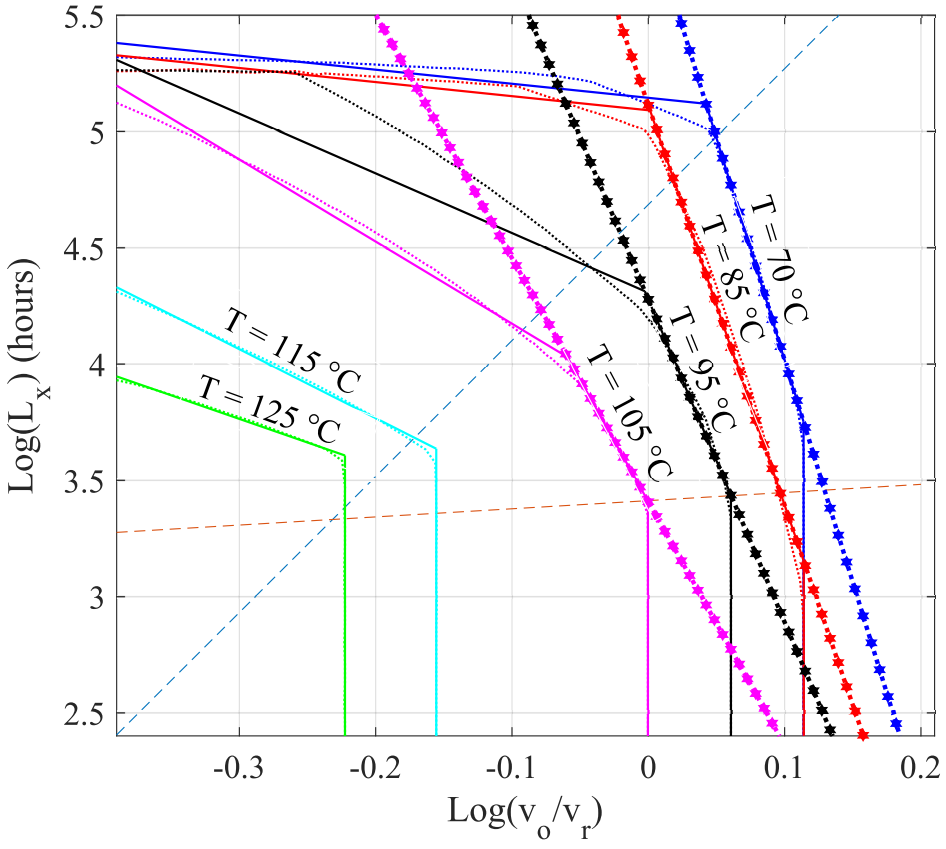


Figure 2.25: Lifetime estimation diagram: Original curves from data-sheet (dotted lines); Fitted model in the main working region for each temperature (hexagram lines); Piece-wise fitted model (straight lines); Upper and lower model boundaries (dashed lines).

Table 2.5: Statistical characterization of the converter lifetime, as resulting from a one-year-long operative time and Monte Carlo analysis.

	B_{10} (years)	μ (years)	σ (years)
F-Cap	7.56	12.56	3.97
E-Cap	4.09	6.8	2.15

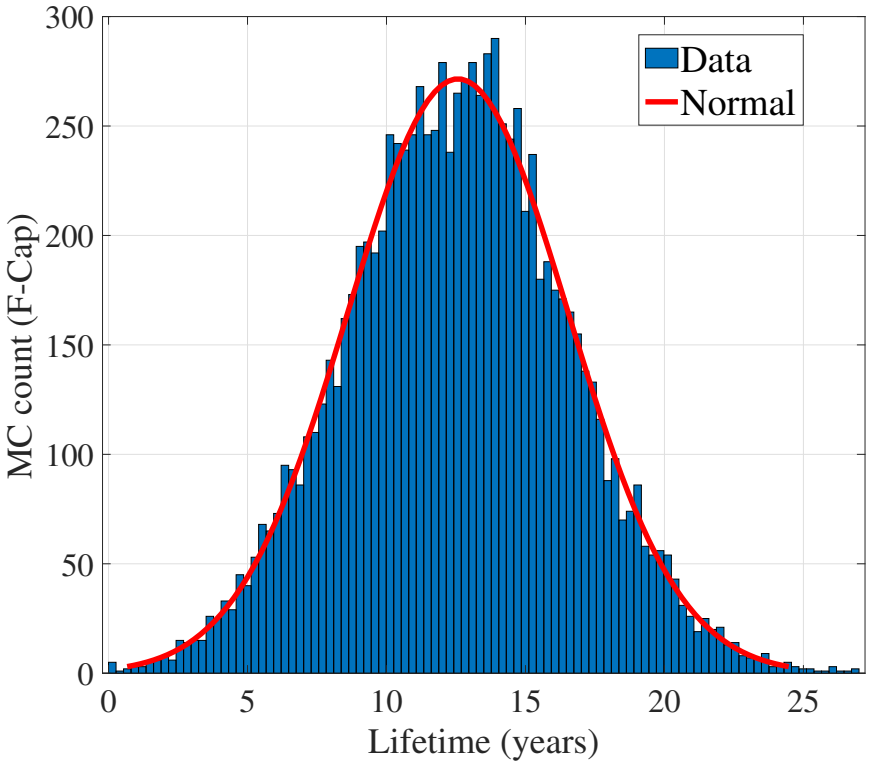


Figure 2.26: F-Cap lifetime histogram from Monte Carlo simulations and fitted as a normal distribution.

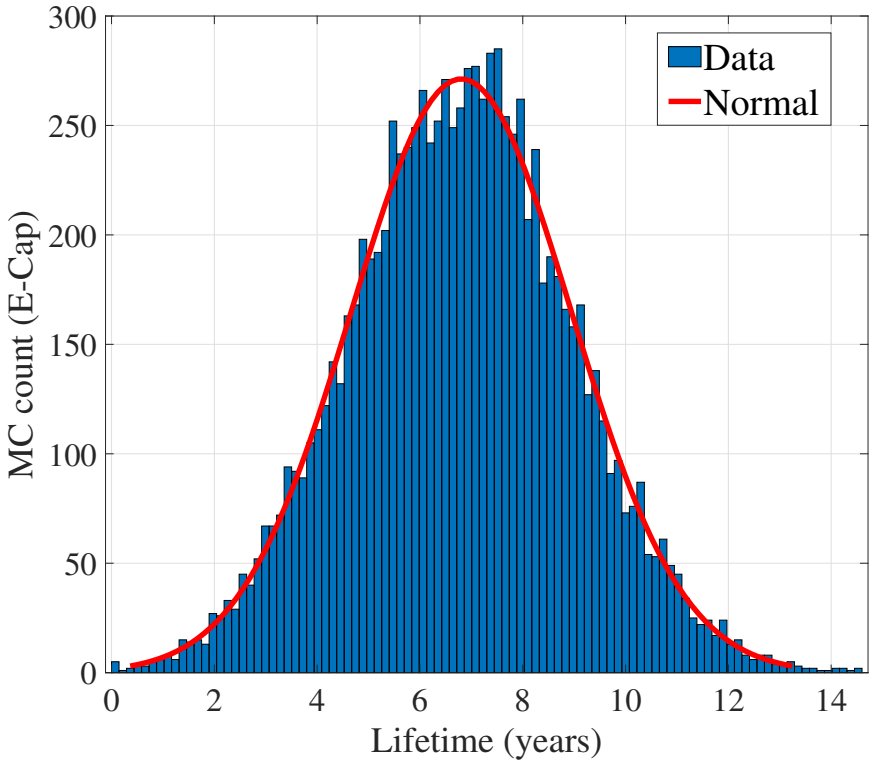


Figure 2.27: E-Cap lifetime histogram from Monte Carlo simulations and fitted as a normal distribution.

2.3.4 Montecarlo Analysis

The parameter L_n used in the reliability model (2.24) depends on a statistical distribution and is affected by uncertainty. Montecarlo analysis can be adopted to define the effects of reliability model parameter dispersion on L_n. Therefore, the related standard deviation can be obtained from statistical analysis of the fitted model in Fig. 2.25, which can then be used for Montecarlo method. From the Montecarlo data shown in Fig. 2.26 and 2.27 (10^4 runs), fitting a normal distribution allows us to determine quantitatively the statistically meaningful lifetime metrics. As reported in Table 2.5, B_{10} is the time in which 10% of the initial population has failed. From a practical point of view, this parameter can sometimes be more effective than a rough mean value in describing the expected lifetime. The mean (μ) and standard deviation (σ) are represented as well in Table 2.5. It can be seen that the technological change from E-Cap to F-Cap can extend the capacitor's expected lifetime by two times.

Chapter 3

Active Overcurrent Protection

This chapter presents the ILCL analysis and design. The implementation is described, and the basic equations are provided to facilitate the design, the prototype PCB has been developed and is shown in Fig. 3.1; the main components of this design are highlighted in red and those will be discussed in Chapter 3.2 and Chapter 3.3; also the control algorithm and its tuning are described and discussed in Chapter 3.3. A first validation has been performed through a non-ideal simulation using PLECS.

3.1 ILCL Concept

ILCL scheme is visible in Fig. 3.2, where M_1 is the bypass transistor, M_2 and M_3 are the switching transistors of the synchronous buck converter. C and R represent the load and L is the filter inductor.

As shown in Fig. 3.3, after the system startup the capacitor is initially discharged: to prevent the initial overcurrent, the system will control the capacitor charge limiting the inrush current. After reaching the nominal voltage, M_1 is turned on while M_2 and M_3 are turned off. If the current exceeds a predefined limit, M_1 is immediately turned off and M_2–M_3 start switching, to limit the fault current. This condition persists until the current falls below the minimum fault threshold, at which point the bypass takes over or when the trip-off time expires. The functioning parameters of

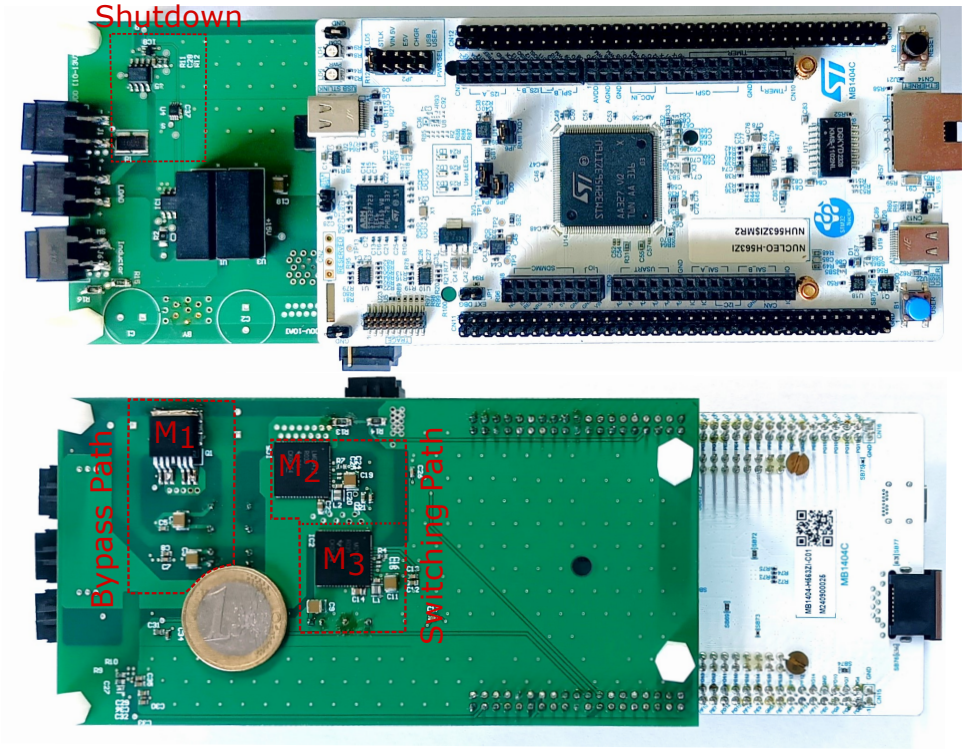


Figure 3.1: ILCL board Prototype, in red are highlighted the main points of the design.

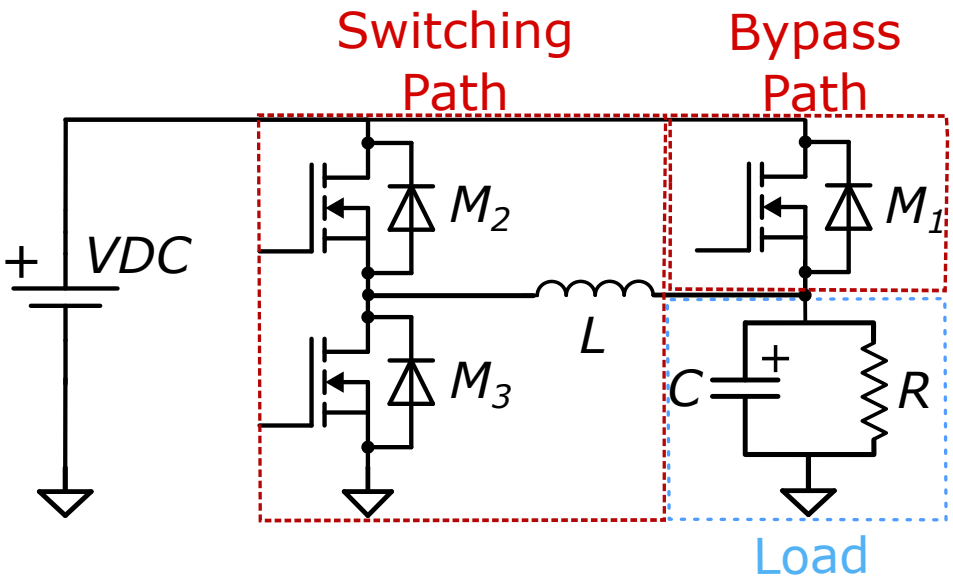


Figure 3.2: Industrial LCL Scheme. M_1 is the bypass transistor, M_2 and M_3 are the switching transistor of the synchronous buck converter combined with the inductor filter L; While R and C are the load components.

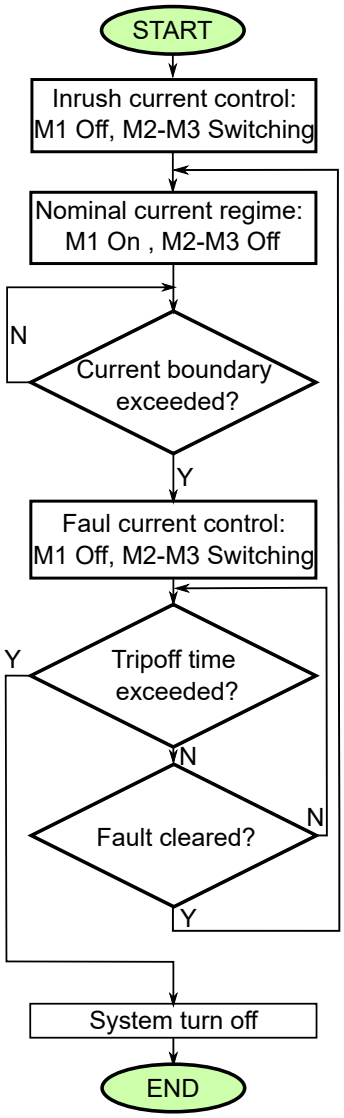


Figure 3.3: Flowchart describing the ILCL system operation.

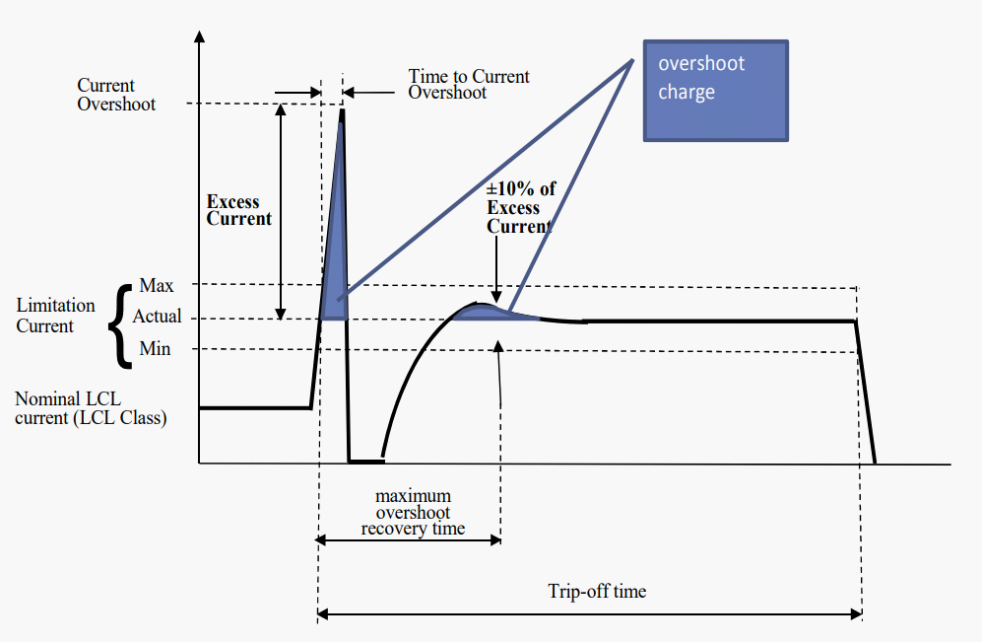


Figure 3.4: Typical LCL response during overcurrent, taken from ECSS-E-ST-20-20C.

the ILCL were taken from Aerospace standards since they are typically more strict than in the industrial field.

3.1.1 ECSS Regulation

The ECSS engineering standards establish technical criteria for space systems to create consistency within the European space industry. The ECSS-E-ST-20-20C [96] standard specifically addresses linear LCLs defining the requirements for current and time related to fault response depending on LCL class, which is defined form the nominal current. A typical LCL response related to a overcurrent condition is shown in Fig. 3.4 taken from ECSS-E-ST-20-20C [96].

If the current goes over “Min limitation current”, the first overshoot must be bounded behind the “Max Current overshoot”, after the first dynamic, the current

can drop to zero, and start limiting the fault between "Min" and "Max limitation current". The "Max overshoot recovery time" defines the max settling time to reach current regime after a fault occurs. The "Trip-off time" is the maximum duration for current-limited operation after a fault occurs; if the fault persists beyond this limit, the system will shut down. For this design we adopted as a target a class-10 LCL, which criteria are defined in Table 3.1.

3.2 Converter Design

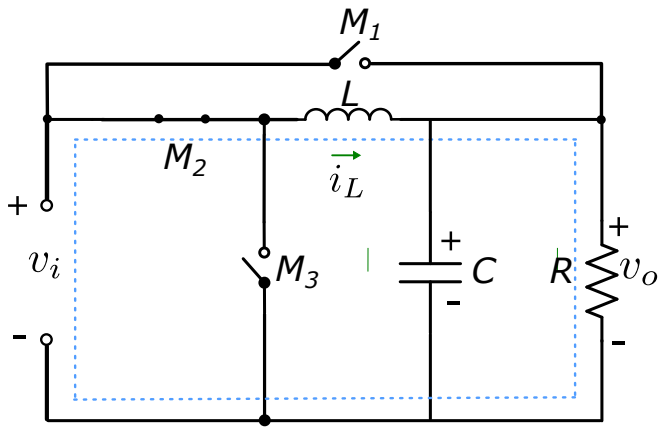
Due to the industrial application of this design, the power rating chosen is $P = 1\,\mathrm{kW}$, the current rating is defined by ECSS guidelines in Table 3.1, so the DC link voltage is $V_{DC} = 100\,\mathrm{V}$. Due to the unpredictable nature of a fault, the resistive load is supposed to vary between $R = 10\,\Omega$ in the nominal condition and $R = 0.1\,\Omega$ in case of a full short circuit, with admissible all intermediate cases. For simplicity of calculation, the resistive load will be stated as admittance $G = 1/R$. The chosen capacitance related to the value of V_{DC}, taking into consideration the capacitance value of industrial DC links [97], has been chosen as $C = 100\,\mu\mathrm{F}$.

In Fig. 3.5a and Fig. 3.5b the switching behavior in the on and off states of ILCL are described, from which is obtained, in the hypothesis of continuous conduction mode (CCM), the well known equations:

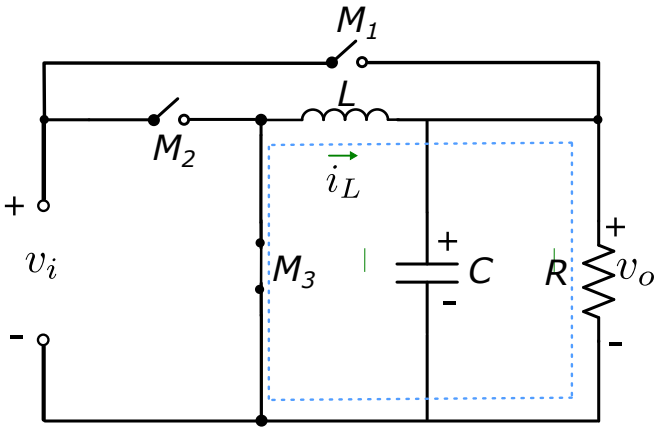
$$\begin{cases} \Delta I_{\mathrm{L\,on}} = \dfrac{v_i - v_o}{L} D T \\ \\ \Delta I_{\mathrm{L\,off}} = -\dfrac{v_o}{L} (1 - D) T \end{cases} \tag{3.1}$$

where v_i, i_L and v_o are the input voltage, inductor current and output voltage respectively and D is the duty ratio defined as $D = v_o/v_i$. It is possible to derive the minimum value of inductance to not exceed the maximum current ripple defined in Table 3.1 substituting D in (3.1),

$$\Delta I_{\mathrm{L\,on}} = \frac{T}{L} \left(v_o - \frac{{v_o}^2}{v_i} \right). \tag{3.2}$$



(a) Switch-ON



(b) Switch-OFF

Figure 3.5: ILCL converter scheme and equivalent circuits depending on the switch status.

By deriving $I_{\mathrm{L\,on}}$ as a function of v_o, it is possible to find the voltage ripple worst case $v_{o_{wc}}$ to calculate $L_{\min}$,

$$\frac{dI_L}{dV_{\mathrm{out}}} = \frac{T}{L}\left(1 - 2\frac{v_o}{v_i}\right) = 0 \Rightarrow v_{o_{wc}} = \frac{v_o}{2} \tag{3.3}$$

substituting $v_{o_{wc}}$ in (3.2) $L_{\min} = 8.33\,\mu\mathrm{H}$ can be obtained using the highest ripple possible defined by Table 3.1, applying a margin of safety, $L = 10\,\mu\mathrm{H}$.

3.2.1 Devices Selection

By differentiating the bypass (M_1) and switching (M_2, M_3) lines, the device sizing of the ILCL can be tailored. M_1 should be an high-current device with low R_{on} minimizing conduction losses and the occupied area, for which a high-current silicon device (IPF067N20NM6ATMA1) has been chosen. In nominal conditions $R_{on} = 2.1\,\mathrm{m\Omega}$, so the power losses at $I = 10\,\mathrm{A}$ are $P_j = 210\,\mathrm{mW}$ resulting in an efficiency $\eta = 99.98\%$; While during fault the operation takes place in a few milliseconds not affecting the overall efficiency. While M_1 should switch only once in a while, in case of fault or startup, with a very fast dynamic a low delay insulated gate driver (MAX22700EASA+) has been chosen.

Due to the short operating time of M_2 and M_3, it is possible to assume an adiabatic regime; the thermal behavior relies only in the transient resulting in the thermal network visible in Fig. 3.6. This allows optimizing the chosen devices considering the worst case of a single pulse of the trip-off time duration. This simplifies the calculations for the thermal design, while, knowing the power loss during the adiabatic regime only the junction to case resistance must be evaluated to know the temperature increment in the period,

$$T_j = \frac{R_\theta}{P_j} \tag{3.4}$$

In order to minimize losses, GaN transistors (LMG3422R030RQZT) at very high switching frequency, $f_{SW} = 1\,\mathrm{MHz}$, are chosen for the switching stage.

Table 3.1: LCL class-10 specifics from ECSS-E-ST-20-20C.

LCL class-10	
Nominal current [A]	10
Min limitation current [A]	11
Max limitation current [A]	14
Max current ripple [A]	3
Max Current overshoot [A]	50
Time to current Overshoot [µs]	5
Max overshoot recovery time [µs]	300
Trip-off min [ms]	1.5
Trip-off max [ms]	3

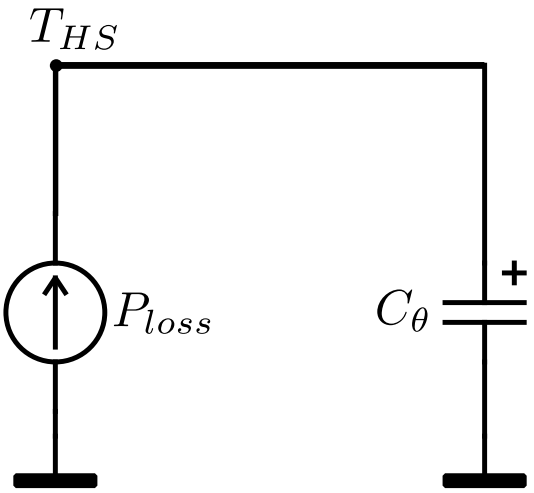


Figure 3.6: Thermal network of switching mosfets and inductor during switching operation in the hypothesis on adiabatic regime.

3.2.2 Inductor Sizing

A similar assumption can be made for the inductor L, for which it is possible to minimize its area occupancy by optimizing the temperature increment over the time span of operation. In order to properly design the power inductor, different boundaries must be taken into account.

This section is structured as a practical guide to achieve an optimal design in this peculiar thermal condition, as shown in Fig. 3.7, the design is structured as follows:

First of all, in the condition of adiabatic regime it is possible to find the optimal inductor wire size A_w combining the following equations :

1. Second Ohm's law to determinate the wire resistance:

$$R_w = \rho \frac{l_w}{A_w} \quad [\Omega], \tag{3.5}$$

   where l_w is the wire length, ρ is the conductor resistivity depending on the material and R_w is the total wire resistance.

2. Power dissipated on the inductor wire:

$$P_w = R_w I_0^2 \quad [\mathrm{W}] \tag{3.6}$$

   where I_0 is the average current on the inductor and P_w is the power dissipated by the inductor.

3. Inductor wire volume:

$$V_w = l_w A_w \quad [\mathrm{m}^3] \tag{3.7}$$

   where V_w is the wire volume.

4. Wire thermal capacitance equation:

$$C_{\theta w} = C_{\theta r} V_w \quad [\mathrm{J}/^\circ\mathrm{C}] \tag{3.8}$$

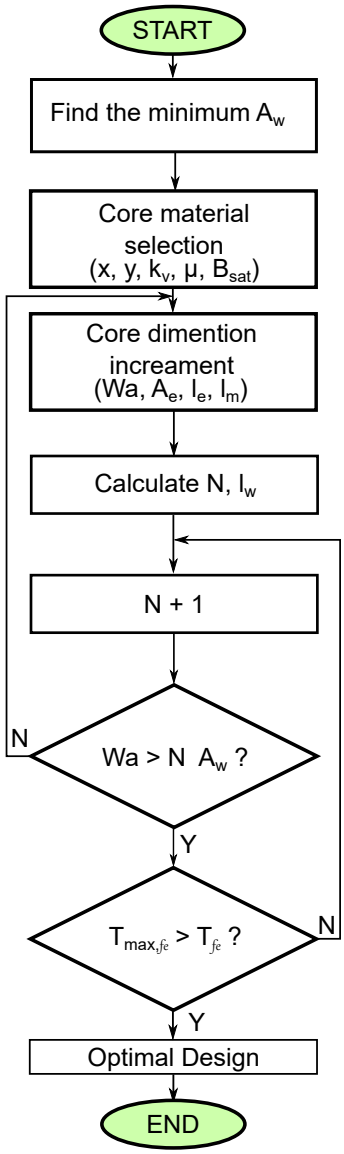


Figure 3.7: Inductor design workflow to achieve minimum area in the hypothesis of adiabatic regime.

where $C_{\theta rw}$ is the volumetric thermal capacity (specific) depending on the material, and $C_{\theta w}$ is the thermal capacity.

5. Conductor temperature rise:

$$\Delta T_w = P_w \frac{t_{on}}{C_{\theta w}} \quad [^\circ\mathrm{C}] \tag{3.9}$$

where t_{on} is the trip-off time and ΔT_w is the temperature linear rise during the period in adiabatic regime.

Substituting all the equations into (3.9) results,

$$\Delta T_w = \frac{\rho\, t_{on}\, I_0^2}{A_w^2\, C_{\theta r}} \tag{3.10}$$

from which emerges a significant result while in this condition ΔT_w is totally independent from l_w; so, defining $\Delta T_w = T_{\mathrm{max,\,w}}$ it is possible to minimize the copper area given a certain maximum temperature,

$$A_w \geq \sqrt{\frac{\rho\, t_{\mathrm{on}}\, I_0^2}{T_{\mathrm{max,w}}\, C_{\theta r}}}. \tag{3.11}$$

Then, the core material must be selected depending on the switching frequency f_{sw} and the saturation flux B_{sat} needed, knowing the material, the core losses can be derived from Steinmetz Equation,

$$P_{fe} = k_c \cdot f_{\mathrm{sw}}^x \cdot \hat{B}^y \cdot V_e \quad [\mathrm{W}] \tag{3.12}$$

where k_c is the core loss constant (dependent on core material and frequency) , x is the Steinmetz exponent (for frequency) and y is the Steinmetz exponent (for flux density) [98] and V_e is the core volume. The core volume can be calculated as,

$$V_e = A_e \cdot l_e \quad [\mathrm{m}^3] \tag{3.13}$$

where A_e is the core area and l_e is the core length given after selecting a core shape. The wide variety of shapes and sizes available in the market makes the core

selection a nontrivial choice; starting with a small core size and then increasing it if design limits are exceeded can be a winning choice. From the inductor flux equation,

$$\hat{B} = \frac{\hat{I}L}{NA_e} \quad [\mathrm{T}], \tag{3.14}$$

the minimum number of turns to achieve flux saturation N_{min} can be found choosing $\hat{B} = B_{sat}$ obtaining,

$$N_{min} = \frac{LI_{pk}}{B_{sat}A_e}. \tag{3.15}$$

To ensure that saturation is not reached, the effective number of turns $N = N_{min} + 1$. The total wire length l_w can be calculated as,

$$l_w = N(2l_m) \quad [\mathrm{m}], \tag{3.16}$$

where l_m is the mean section of the core of the core. The window area Wa, defined as the open section within the core of the transformer or inductor, through which the copper wire windings passes. This must be multiplied by a fill factor f_f, a safe margin needed while the wire cannot totally fill the area resulting in $Wa_f = A_w f_f$. The condition $Wa_f \geq NA_w$ must be satisfied or the core cannot fit the design and the core size must be increased. If the core satisfy the boundaries, the last check is related to the maximum core temperature,

$$\Delta T_{fe} = \frac{P_{fe} \cdot t_{on}}{C_{\theta fe}} \quad [^{\circ}\mathrm{C}]. \tag{3.17}$$

Substituting the equation in (3.12) results,

$$T_{max,fe} \geq \Delta T_{fe} = \frac{k_c \cdot f_{\mathrm{sw}}^x \cdot \hat{B}^y \cdot V_e \cdot t_{on}}{C_{\theta fe}}. \tag{3.18}$$

If this last condition is satisfied, the inductor design is optimized.

3.3 Control Design and Validation

In this application, the response time of the first overshoot is crucial since the bypass path cannot limit the current rise in any way. To achieve the response time criteria

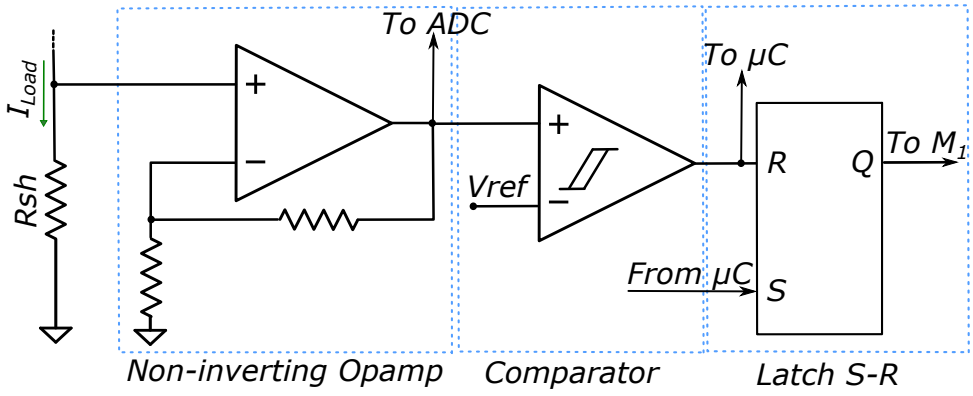


Figure 3.8: Analog shutdown scheme controlling the bypass transistor M_1 turn-on and turn-off.

defined in Table 3.1, the shutdown control should be analog in order to minimize the response time, while the current control could be digital, to maximize the performances, minimizing the number of components.

3.3.1 Analog Control

In Fig. 3.8 the analog control is visible. The load current is sensed by a shunt resistor and amplified by an operational amplifier (OPA354AIDDAR) in non-inverting configuration. The op-amp output signal is sampled by an ADC for the digital control and is the positive input of a comparator (TS3011ICT), when the current exceeds the minimum threshold defined in Table 3.1, the comparator output becomes active, resetting the S-R latch (SN74AUP2G02DCUR) and turning off M_1. The turn-on of M_1 is controlled by the microcontroller.

By choosing these components, also taking into account the shutdown time of M_1 comprehensive of opto-coupler and gate driver delay, the response time of the system is $t_d = 104\,\text{ns}$.

In order to limit the current during the first overshoot according to the specifica-

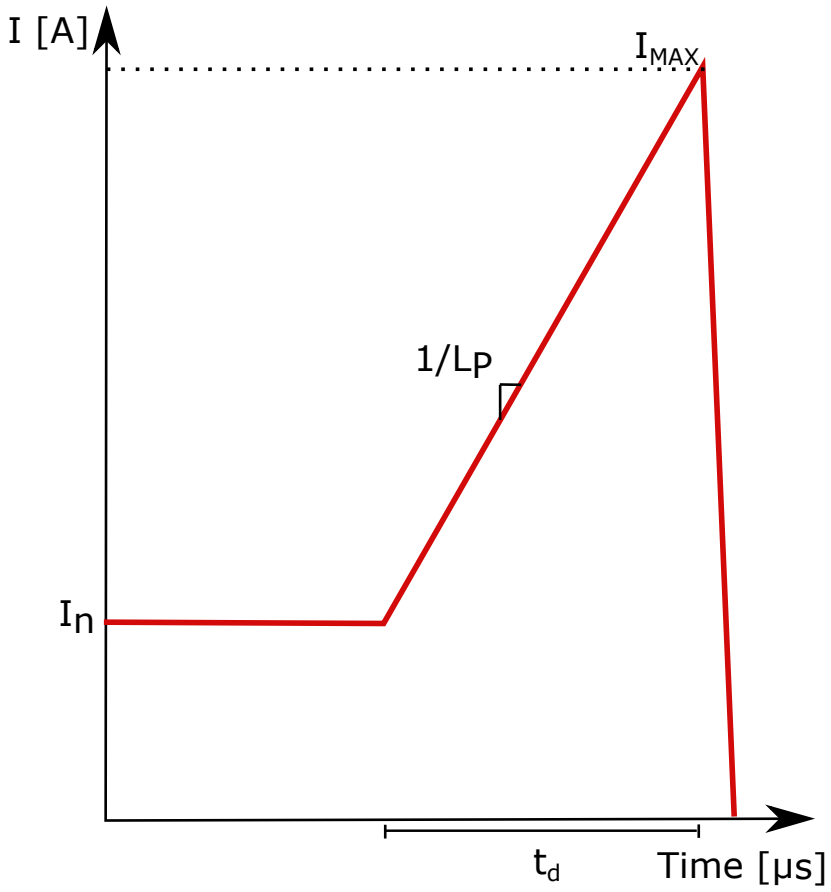


Figure 3.9: First overshoot dynamic after fault.

tion of Table 3.1 an inductance in series to the fault current path should be present to limit the current dynamic, it can be defined from the inductance voltage formula:

$$v_l = L\frac{di}{dt}, \tag{3.19}$$

as,

$$L_p = \frac{VDCt_d}{I_{MAX} - I_n} \tag{3.20}$$

as summarized in Fig. 3.9. From which emerges that $L_p = 260\,\text{nH}$ in the worst case scenario of a complete short circuit on the load. An inductor can be put in the current path or, while it is very small, it can be supplied by the parasitic inductance of the wiring harness.

3.3.2 Digital Current Control

For the digital control the Nucleo Board STM32 H563ZIT6U has been chosen. From (3.1) the general analytical average model of buck converter can be obtained and is represented in the following equations:

$$L\frac{di_L}{dt} = v_x - v_o; \quad C\frac{dv_o}{dt} = i_L - Gv_o \tag{3.21}$$

where $v_x = v_i D$ is the product of the inputs. The open loop transfer function is then obtained as

$$H(s) = \frac{I_L}{V_x} = \frac{G + sC}{s^2LC + sLG + 1}, \tag{3.22}$$

It can be seen that the system consists of a zero with negative real part, thus minimum phase, and two conjugate complex poles, resulting in an oscillating response. In order to properly control the system, a full state feedback system [99] can be implemented.

From (3.21) it is possible to define the state space equation as,

$$\begin{cases} \dot{x} &= Ax + Bv_x \\ y &= Cx + Dv_x \end{cases} \tag{3.23}$$

where $x = [i_l, v_c]^T$ are the system states needed to being sensed and v_x is the input, the state matrixes are

$$A = \begin{bmatrix} 0 & -1/L \\ 1/C & -G/C \end{bmatrix}, B = [1/L, 0]^T, C = I_2, D = 0 \tag{3.24}$$

which describes the different features of the system, in this particular case while C is the 2×2 identity matrix, the outputs are equal to the states. By using the pole placement technique, a pole-zero cancellation can be achieved, simplifying the system to a first-order model. Defining $A_{cl} = A - BK$, where $K = [K_1, K_2]$, it is possible to change the poles position rearranging the state matrix as follows:

$$\dot{x} = A_{cl}x + BK_r v_x \tag{3.25}$$

While the eigenvalues of A_{cl}, $\det(A_{cl} - \lambda I) = 0$ describes the poles, solving the following system it is possible to redefine the poles position,

$$\begin{cases} \lambda^2 + (1 + K_1)\lambda + (K_1 + 4K_2) = 0 \\ a\lambda^2 + b\lambda + c = 0 \end{cases} \tag{3.26}$$

it is possible to find a, b and c imposing the solutions $\lambda_{1,2}$ of the second degree equation, from (3.22) it is possible to find the exact value of the zero to perform the pole/zero cancellation with $\lambda_1 = -1100\,\text{rad/s}$ and $\lambda_2 = -20\,000\,\text{rad/s}$ to settle the remaining pole at the desired cutoff frequency, achieving the wanted settling time not to exceed the "Time to current Overshoot" defined in Table 3.1. Solving the system equation in (3.26) it is possible to find $K = [0.2, -1]$. While the DC gain of the output is not controlled, the DC gain of the step response K_{DC} can be found and finally $K_r = 1/K_{DC}$, that in this case is $K_r = 5$.

In Fig. 3.10 the comparison between the open loop and closed loop bode diagrams is shown, the latter is a first order response as expected.

Since the parameters value may be subject to tolerance and given the uncertain nature of the load during fault, a study based on Robust Parametric Control [100] has been conducted, to have the appropriate response to the different combination of parameters. For L and C a 20% tolerance of the nominal value has been chosen; the load G can vary as defined in Chapter 3.2. As shown in Fig. 3.11 all the possible

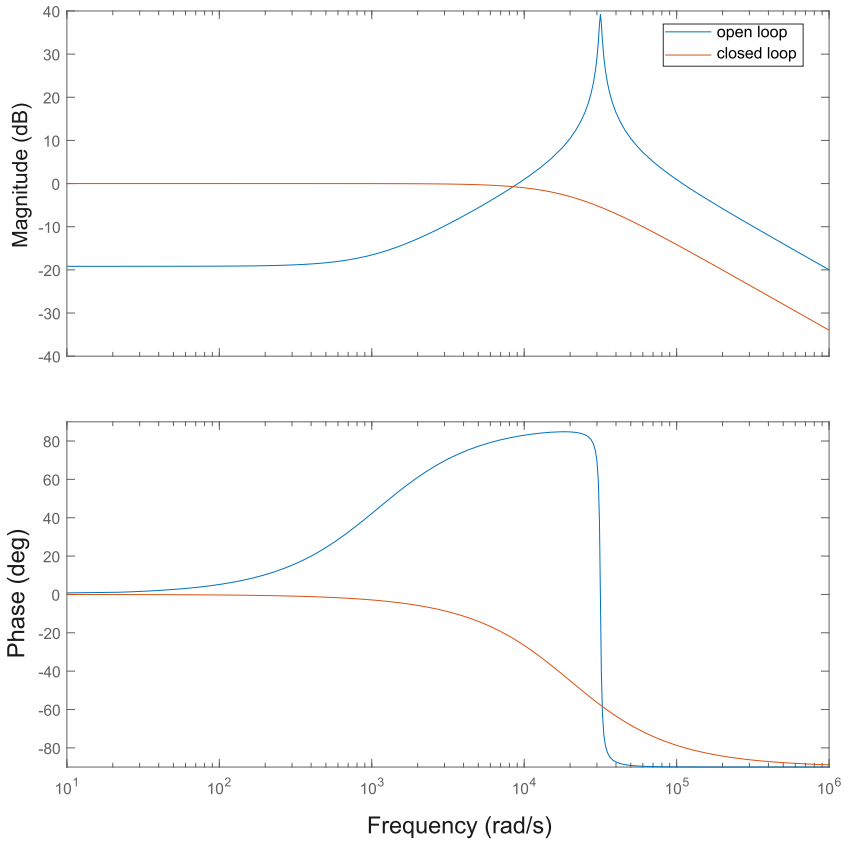


Figure 3.10: Bode diagram comparison between open loop and closed loop ILCL, in blue the open loop diagram and in red the closed loop one.

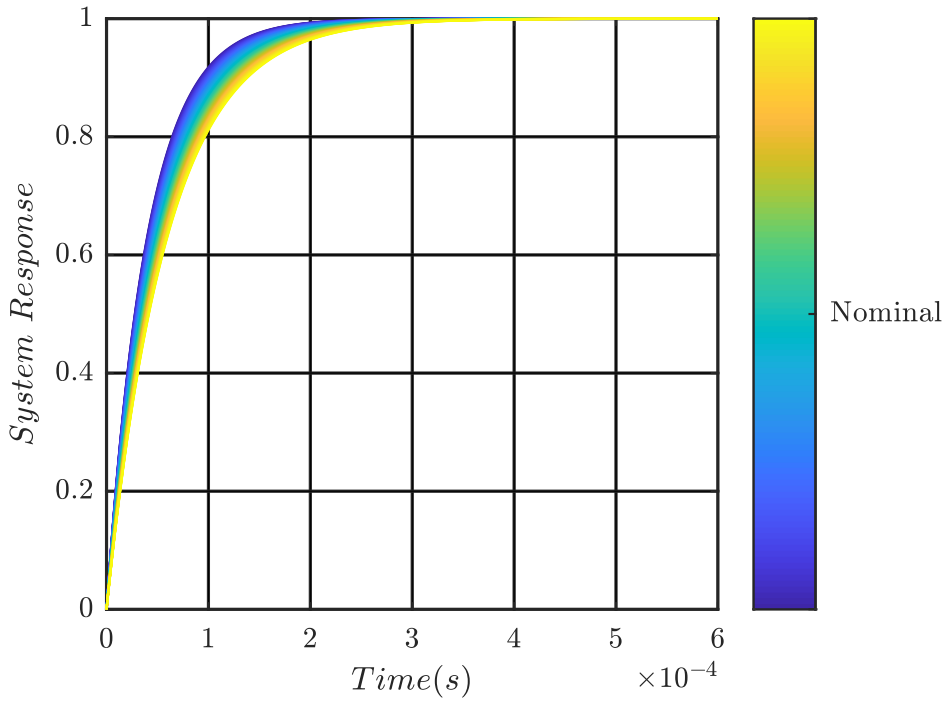


Figure 3.11: Step response of the system in different parameters settings, the color map defines the deviation from nominal values. The gradient defines how far the various tests deviate from the nominal situation of the parameters, blue defines lower values (on average) of the nominal, and yellow higher values.

combinations of parameters result in a stable system response, for clarity only 100 of these combinations are visible in the graph.

A PLECS simulation has been built to validate the proposed control, adding all the non-idealities related to a real system implementation as shown in Fig. 3.12. The simulation only regards the fault scenario with M_1 fully off. With a switching frequency of $f_{sw} = 1\,\text{MHz}$, the sampling frequency has been set at $f_s = 200\,\text{kHz}$, the delay chain related to the actuators (Opto-couplers, Gate drivers and devices) has been defined from datasheets as such as the ADC delay. The duty cycle is saturated

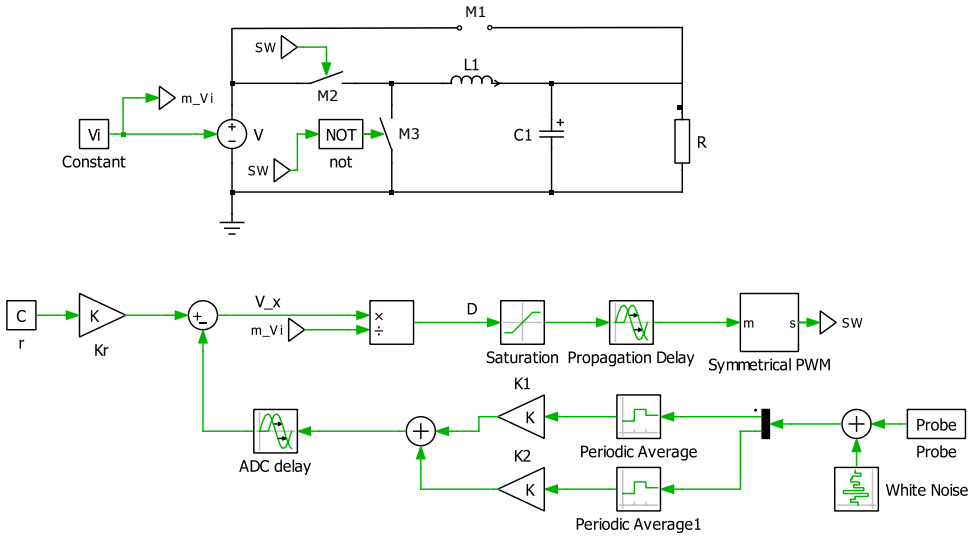


Figure 3.12: Detailed schematic of the proposed ILCL, for the validation of the system in simulation.

at $D = 0.95$ and some white noise on the sensed signals has been added.

The current curve can be seen in the Fig. 3.13 and is consistent with what was expected from the control design; the red curve represent the inrush current condition at full load, in this case the current setpoint is lower while the nominal current is 10 A. The green curve is the worst case fault scenario as defined in (3.3) while the blue curve represents a full short circuit condition. In all those cases the current ripple respects the criteria stated in Table 3.1.

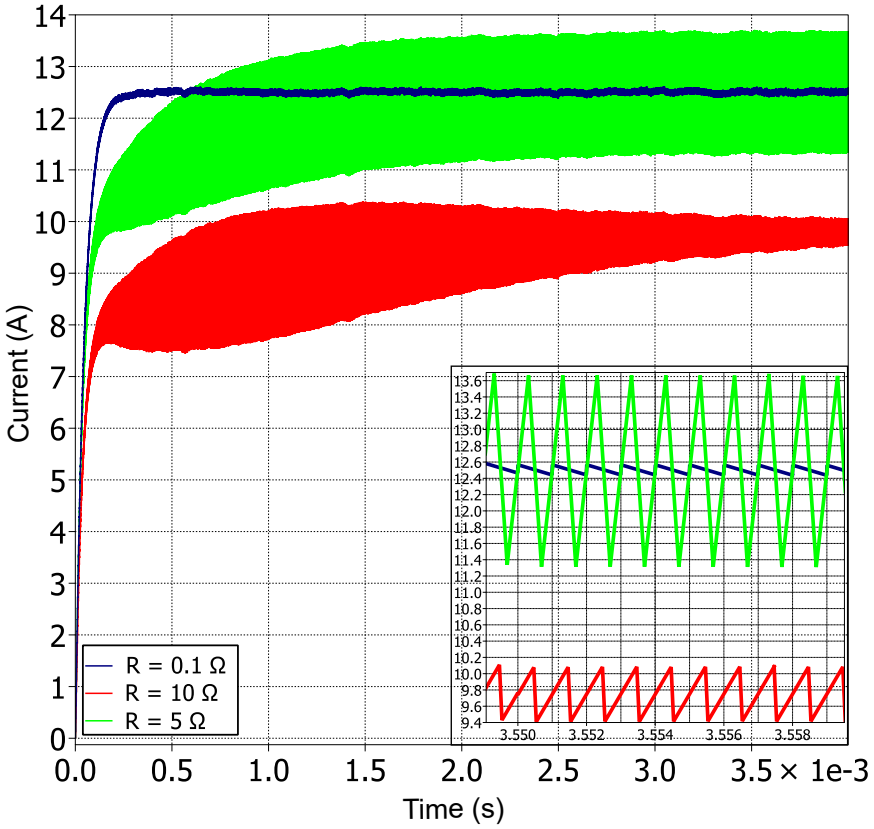


Figure 3.13: PLECS current scope data in different conditions, the blue curve represents a full short circuit condition with $R = 0.1\,\Omega$, the green curve represents a mid overcurrent condition with $R = 5\,\Omega$ and the red curve represents a full load condition with $R = 10\,\Omega$ in the situation of inrush current protection.

Chapter 4

Thermal Sensitive Electric Parameters

4.1 Temperature Measurement and Estimation

Real-time knowledge of the device junction temperature enables maximizing the power density of power electronic converters through active derating and dynamic overloading. Since direct measurement of junction temperature alters the device, Temperature-Sensitive Electrical Parameters (TSEPs) are used for indirect estimation. However, variations in device parameters influencing TSEPs require per-device characterization, limiting their use in commercial converters. This chapter discusses the on-state resistance TSEP for silicon-carbide MOSFETs and introduces a novel method for extracting characteristic curves. Notably, the proposed approach eliminates the need for a temperature-controlled environment by leveraging self-heating and modifying the cooling system. Self-heating is induced via the Controlled Shoot-Through (CST) technique, which operates without a connected load. The TSEP curves are characterized using repetitive sawtooth current pulses on an inductive load at various device temperatures, making this methodology ideal for end-of-line testing in production settings while experimental validation confirms the accuracy of the results against standard laboratory techniques. This study builds upon the work

of [101], refining the methodology using improved hardware and software platforms, increasing the temperature sensing accuracy, and discussing novel temperature estimation models considering the transistor's on-state resistance and conductance.

4.2 Junction Temperature Measurement and Estimation

4.2.1 Proposed Thermal Setup

Usually, to perform a TSEP calibration procedure it is necessary to measure the transistor junction temperature. Unfortunately, usually this quantity is not directly measurable without irreparable damage to the device package. Generally, a temperature sensor is placed in proximity to the junction itself to estimate the T_j. Depending upon the type of transistor, different options are available. When calibrating TSEPs in power modules, the embedded sensors are often used [74,75]. Conversely, in discrete components, a dedicated temperature sensor is usually attached to the device. This work focuses on discrete SiC power MOSFETs in TO-247 package (C2M0080120D by Wolfspeed), and the junction temperature is measured with a NTC sensor placed on the back side of the device using thermal grease.

Usually, when the power converter reaches the end-of-line in the production process, the cooling system (typically a metallic heatsink) is mounted. Unfortunately, performing the TSEP calibration with the heatsink already in place introduces some disadvantages. First, due to the large thermal capacity of the cooling system, a long time is needed to heat the DUT and reach thermal equilibrium. Furthermore, a temperature gradient is established between the junction and the measuring sensor. In fact, regardless of the heat origin (self-heating, or exogenous), if the system's thermal capacities are not in equilibrium, the residual heat flow among them produces a temperature difference between junction and sensor. This is undesirable during the calibration, because it makes the reference temperature sensor unreliable. To solve these issues, the authors decided to perform the TSEP calibration without mounting the heatsink and to thermally insulate the DUT using a specifically designed cork cap.

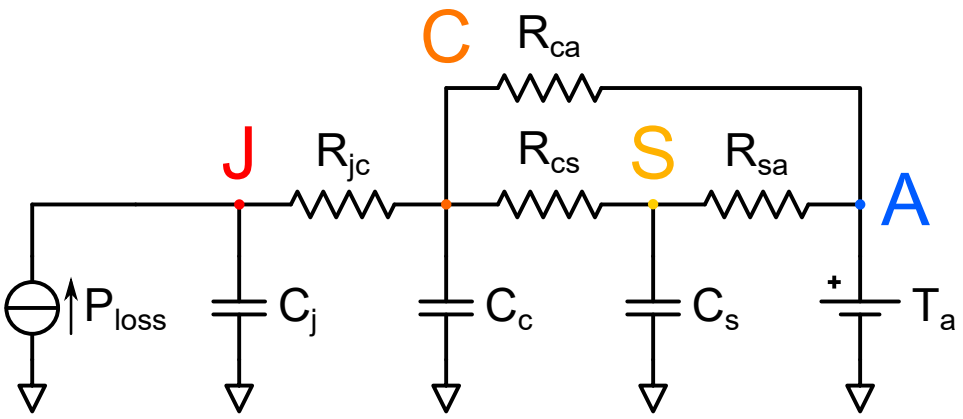


Figure 4.1: Thermal network of the device-heatsink/ambient-sensor assembly. P_{loss} represents the power loss by the device in case of self-heating; the other components are thermal resistances and capacities. The nodes in the thermal network represent the junction (J), the device case (C) with its back directly contacted to the ambient (A) or the heatsink and, the temperature sensor (S) attached between the case and ambient.

Fig. 4.1 shows a simplified thermal network describing the chosen measurement setup. It is important to note that the thermal resistance between case and sensor (R_{cs}) cannot be lowered below a certain value. However, using the proposed insulating cork cap, the thermal resistances R_{ca} (case to ambient) and R_{sa} (sensor to ambient) are significantly increased. This allows to interrupt most of the thermal paths toward the ambient, effectively stopping the heat flow as soon as the junction thermal capacity (C_j) goes in equilibrium with the case and sensor ones (C_c and C_s, respectively). Using this measurement setup the temperature difference across R_{cs} is then almost completely neutralized.

Fig. 4.2 shows the insulating cork cap enveloping the transistor under test and the NTC sensor. Cork has been chosen for its inexpensiveness, very low thermal conductivity ($< 65\,\text{mW}\,\text{m}^{-1}\,\text{K}^{-1}$) and high burning temperature ($> 200\,^{\circ}\text{C}$). In summary, the proposed hardware setup improves the accuracy of the junction tempera-

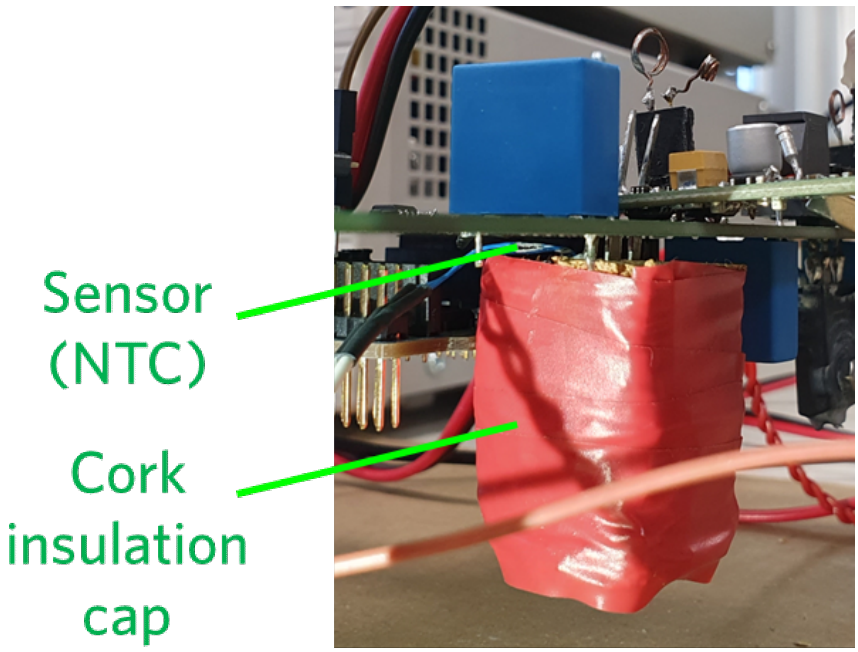


Figure 4.2: Photo of the cork cap (covered by tape, to avoid crumbling) installed on the device under test, with the NTC inside it and coupled to the device itself. No heatsink has been installed.

ture measurement during calibration and, with no heatsink, provides a faster heating phase.

4.2.2 Temperature Estimation Models

In order to estimate the junction temperature during the converter's normal operation, the calibration data needs to be properly processed and condensed into an appropriate model. Since the estimation algorithm needs to run in real time on a resource-constrained embedded system, it's imperative to minimize the model complexity and memory requirements, while also maximizing the prediction accuracy. Unfortunately, the transistor's on-state resistance does not only depend upon the junction

temperature, but also upon the drain current actually making it a nonlinear resistor: $R_{on} = f(T_j, i_d)$, and consequently: $T_j = f^{-1}(R_{on}, i_d)$. In the context of temperature estimation, the current dependency is undesirable, because requires a more elaborated calibration procedure where the R_{on} has to be sampled using many different i_d values.

Usually, the calibration data is rearranged into a two-dimensional lookup table (LUT) [73, 102] or fitted using an empirical polynomial model [72, 74]. In this work, these two established methods are compared against two other estimation approaches proposed by the authors. The aim is to investigate if the calibration can be performed using a very limited number of i_d values, without significantly impacting the estimation accuracy.

In addition, these models are evaluated with R_{on} and its mutual G_{on}, to explore possible advantages of this alternative problem formulation. In fact, considering the linear region and neglecting the effect of channel length modulation, it is possible to express the relationship between on-state resistance and drain current, using the classical Shichman-Hodges (SH) model:

$$i_d = \frac{\beta}{2}\left[2(v_{gs} - V_T)v_{ds} - v_{ds}^2\right] \tag{4.1}$$

$$R_{on} = \frac{v_{ds,on}}{i_d} \tag{4.2}$$

$$R_{on} = \frac{(v_{gs} - V_T)}{i_d}\left[1 - \sqrt{1 - \frac{2i_d}{\beta(v_{gs} - V_T)^2}}\right]. \tag{4.3}$$

Consequently, if the device follows the SH model, the on-state resistance is *not* a polynomial function of i_d. Alternatively, it is possible to start from (4.1) and express directly the on-state conductance G_{on} as a function of the on-state voltage:

$$G_{on} = \frac{1}{R_{on}} = \frac{i_d}{v_{ds,on}} = \frac{\beta}{2}\left[2(v_{gs} - V_T) - v_{ds}\right] \tag{4.4}$$

which *is* a polynomial function of v_{ds} (order one, i.e., a linear one). Moreover, G_{on} remains a polynomial function (of order two) even in case the channel modulation effect λ is considered:

$$G_{on} = \frac{\beta}{2}\left[2(v_{gs} - V_T) - v_{ds}\right](1 + \lambda v_{ds}) = \\ = \beta(v_{gs} - V_T) + \frac{\beta}{2}\left[2\lambda(v_{gs} - V_T) - 1\right]v_{ds} - \frac{\beta\lambda}{2}v_{ds}^2 \tag{4.5}$$

This is an important result because, since both v_{ds} and i_d must be measured at the same time, computing R_{on} or G_{on} does not imply any difference in implementation complexity. Conversely, expressing the on-state conductance as a function of the voltage, resulting in a polynomial, could reduce the fitting error on the acquired data, thus improving the accuracy.

4.3 Active Gate Driver

A dedicated test bench has been built to enable the present study. The hardware platform built specifically for this study is shown in Fig. 4.3, and the diagram of its circuit topology is depicted in Fig. 4.4. The chosen experimental setup consists of an half bridge converter with an inductive load $L = 120\,\mu\text{H}$ connected in pull-up configuration. Using this arrangement, the low side (LS) MOSFET is selected as the DUT under characterization, measuring its T_j, i_d, and v_{on}. The converter is controlled using a STM32 Nucleo-F446RE microcontroller unit (MCU) actuating two active gate drivers (AGD) specifically designed.

The idea of a new gate driver came due to the need to adopt a third, indipendent, gate level while commercial gate drivers do not consent this kind of operations. These AGDs enable the controlled shoot-through technique, in which the an additional gate driver voltage level (V_{ST}) along the usual on (V_{GH}) and off (V_{GL}) ones is introduced. This allows each device of the half bridge to be in ON state, OFF state or CST state [101].

The main AGD functional blocks are shown in Fig. 4.5. The goal of this design is to achieve a modular, isolated MOSFET driver capable of advanced control of the gate, and able to monitor the transistor's on-state voltage. This device is built around a low cost ARM-based MCU (STM32G031F8P6). The auxiliary microcontroller (AUX) manages the gate control, samples the on-state voltage via its internal

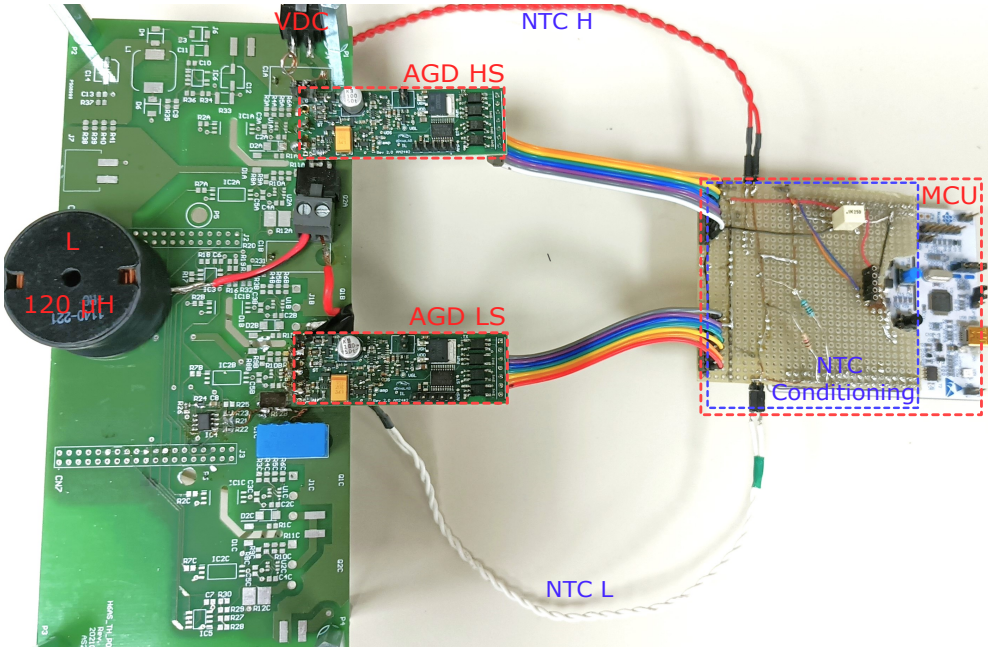


Figure 4.3: Experimental setup used in this study. It is possible to recognize: the high-side and low-side gate drivers, the inductive load (black cylinder), the STM32 MCU, and the NTC cables along with the conditioning circuit.

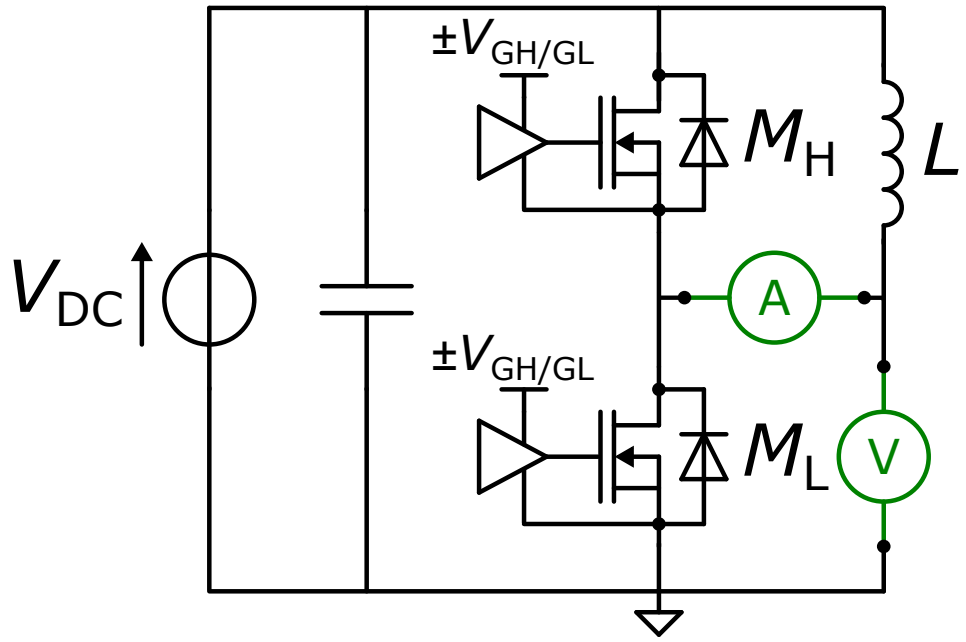


Figure 4.4: Circuit diagram of the proposed hardware platform. The half-bridge is loaded with a purely inductive load and driven by the author's AGDs. The electrical signals, i_d, and v_{on}, measured on the DUT during the experiment are highlighted in green.

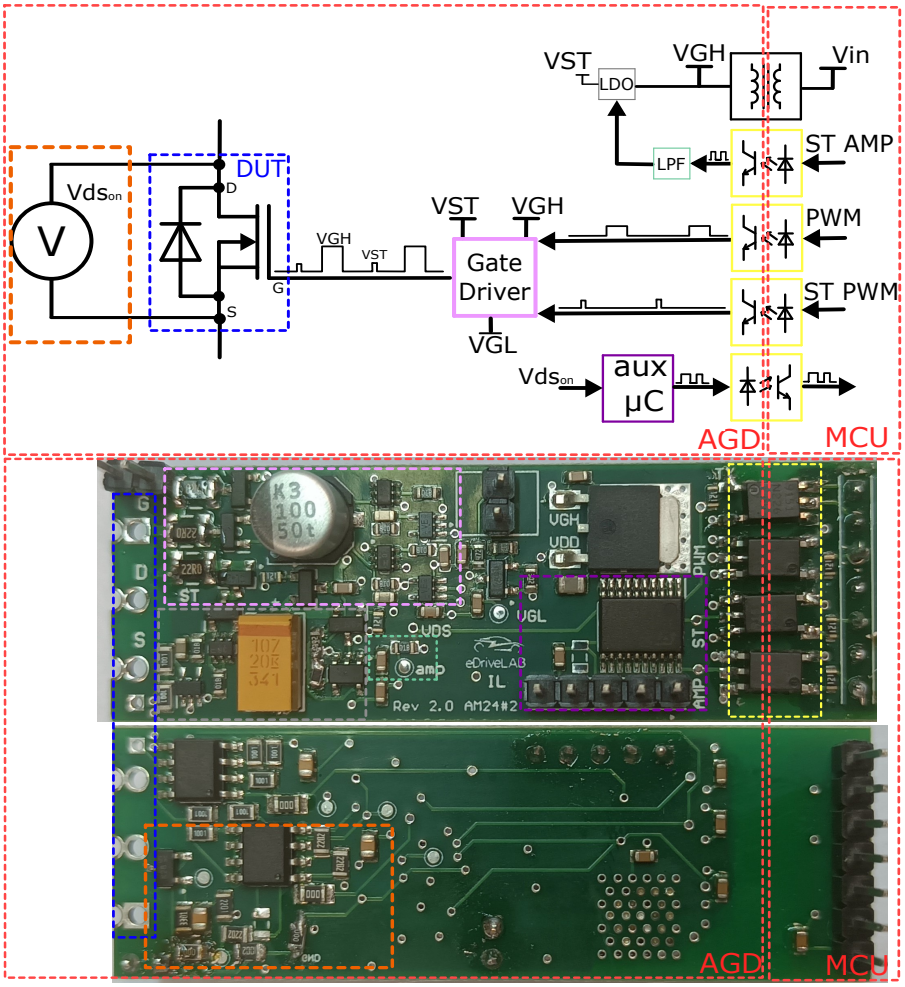


Figure 4.5: Active Gate Driver scheme (Top) and PCB, top and bottom layers (Bottom). All the features of the board are highlighted in different colors: the voltage clamper (orange), the gate driver circuit (pink), the insulated signal transmission (yellow), the auxiliary microcontroller (purple), the shoot-through voltage generation LDO and LPF filter circuits (grey and light green, respectively) and the device under test (blue).

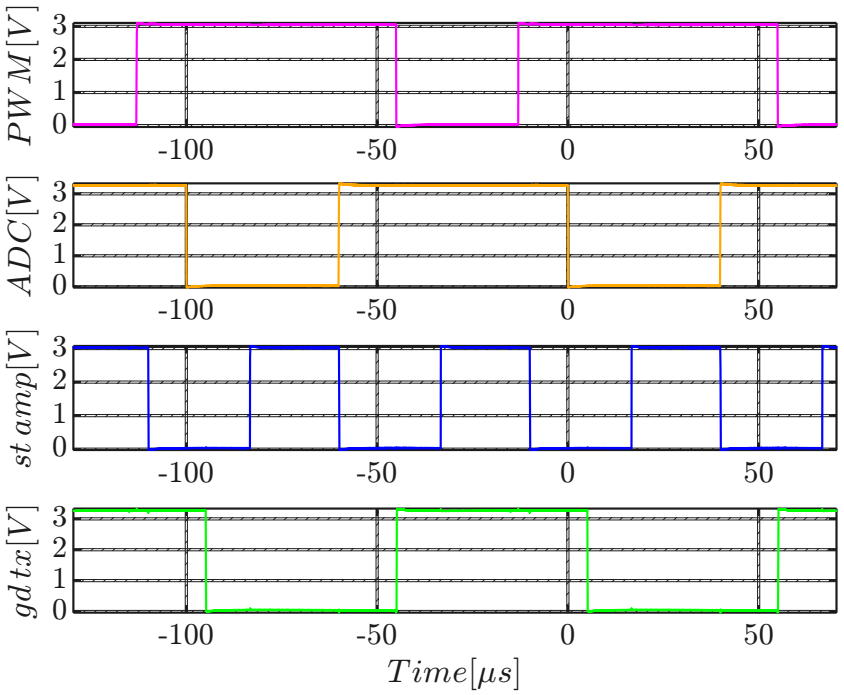


Figure 4.6: Main gate driver controlled signals: the main PWM comanding the AGD (magenta); the internal ADC samling synchronization (yellow); the ST voltage amplitude input signal ST AMP (blue); the digital data signal TX, from AGD to MUC (green).

ADC, and exchanges data or commands using an opto-isolated communication interface.

4.3.1 Auxiliary Microcontroller

In Fig. 4.6 the main signal to AUX synchronization are visible. The PWM signal is in center aligned mode and commands the effective AGD's turn-on and turn-off. The signal ST AMP besides being the voltage setpoint for V_st, it also works as the synchronization signal for the ADC trigger; every two falling edges of ST AMP, the

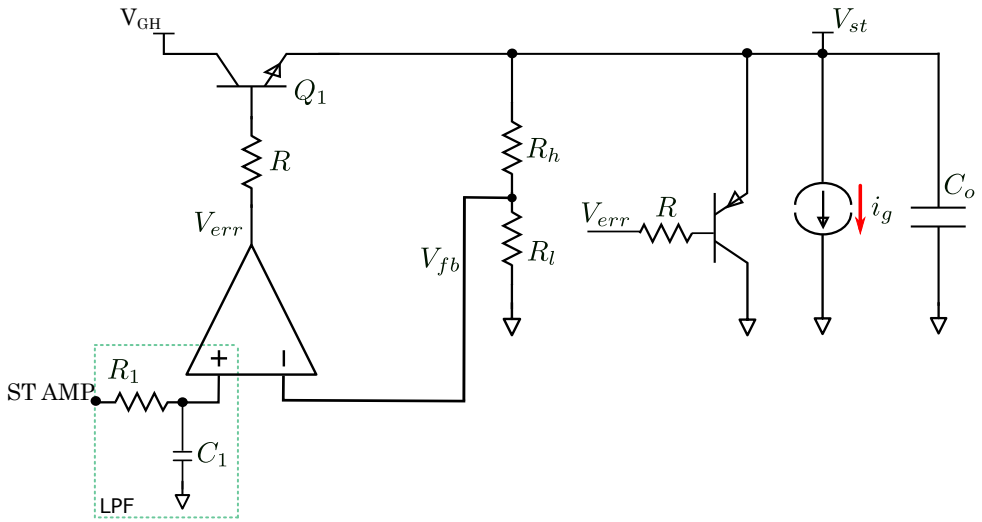


Figure 4.7: LDO ST schematic circuit, based on a common LDO circuit with fast sinking and sourcing capability. This circuit is command by the signal ST AMP processed through a low-pass filter to extract its average value.

ADC is triggered. After sampling the data, the digital information is sent trough the GD TX channel as a modulated square wave signal, while the information lies in the duty cycle. In order to properly insulate the AGD, a fast speed inverting optocoupler (PS9151-V-F3-AX) has been chosen.

4.3.2 LDO for Shoot-Through Voltage Generation

The author's gate driving circuit has been modified compared to canonical topologies [103], to enable an additional voltage level (V_{ST}) on the MOSFET gate. This extra turn-on voltage command can be customized in both amplitude and length (independently), programming the AGD embedded MCU.

The shoot-through pulse amplitude is set via a PWM signal processed through a low-pass filter (LPF) to extract its average value, creating in fact, a very simple DAC. This constant voltage is then used to control a modified LDO shown in Fig. 4.7, which is able to source and sink current rapidly on a capacitor to generate the desired

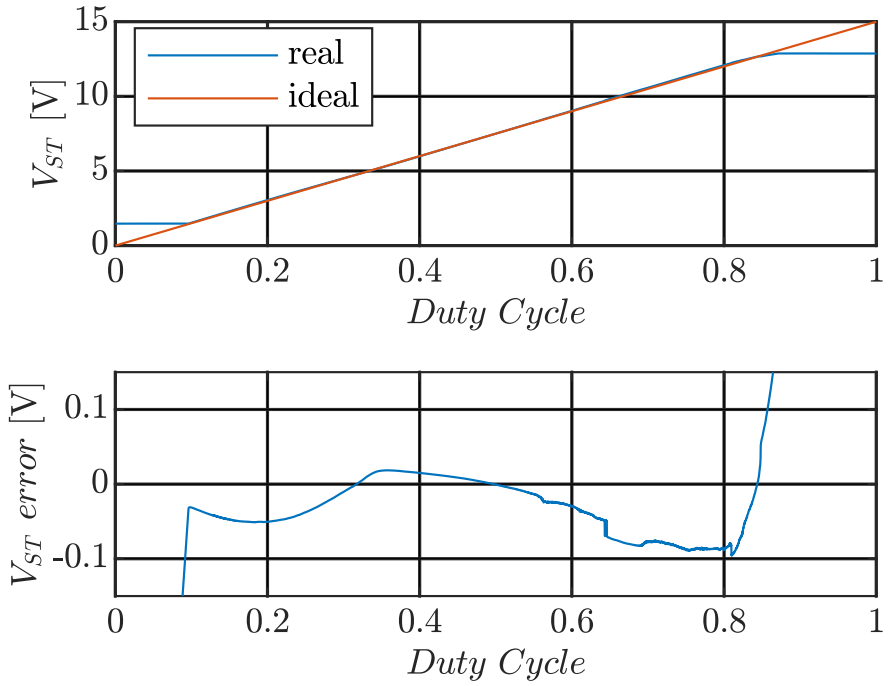


Figure 4.8: $V_{ST}(D)$ curve as a function of the duty cycle. On top is visible the real V_{ST} set by the modified LDO circuit versus the ideal gain linear function depending on the duty cycle defined in (4.6). On bottom the V_{ST} error defined as the difference between the ideal and real V_{ST} curve.

V_{ST}. From the scheme in Fig. 4.7 it is possible to derive $V_{ST}(D)$

$$V_{ST} = D V_{DD} \frac{R_h + R_l}{R_l} \tag{4.6}$$

where D is the ST AMP signal duty cycle and V_{DD} is the logic voltage supplying the PWM signals.

In Fig. 4.8 is visible the circuit behaves as designed in (4.6), and the voltage error is less than 0.1 V in the operating range. However, $V_{ST}(D)$ is no longer linear in the duty cycle extremes due to op-amp saturation; this is not a problem while the

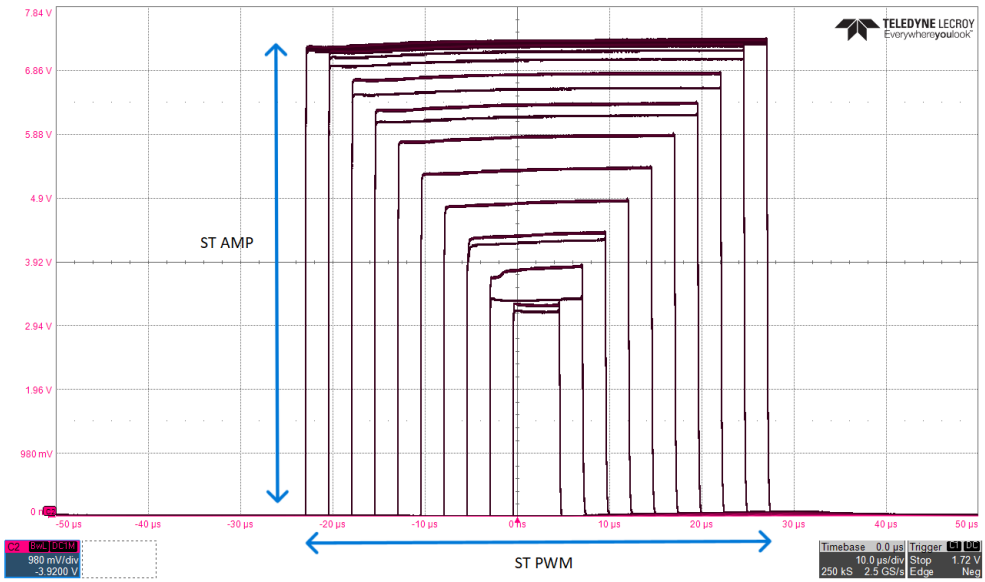


Figure 4.9: V_{ST} signal acquired from oscilloscope in persistence configuration. Different combinations of period and amplitude are shown.

V_{ST} operative range is between 3 V and 10 V depending on the device type and the wanted current.

Different combinations of V_{ST} and PWM ST are visible in Fig. 4.9 enabling a full control on gate voltage and period.

Furthermore, a power-on CST pulse is visible in Fig. 4.10, where the i_d current is totally dependent on the V_{ST}.

4.3.3 Gate driver

in order to adapt the CST functioning in a gate driver, a new topology has been built. As shown in Fig. 4.11, this gate driver in addition to working in the normal push-pull configuration, can work in a different voltage level due to the ST current path, allowing a third variable level gate voltage.

To do so it is important to synchronize the ST PWM signal and the normal PWM signal to avoid an internal short-circuit path, taking into account that the signals are

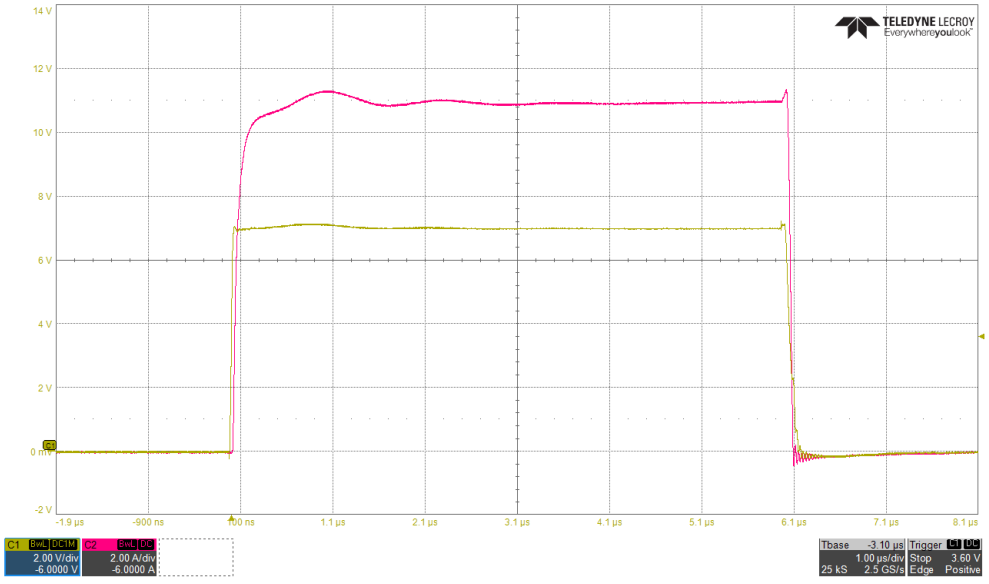


Figure 4.10: CST pulse acquired with the oscilloscope during device turn-off. The yellow curve is the modulated gate voltage with $V_{gs} = V_{ST} = 7\,\mathrm{V}$; while the pink curve is the injected CST current.

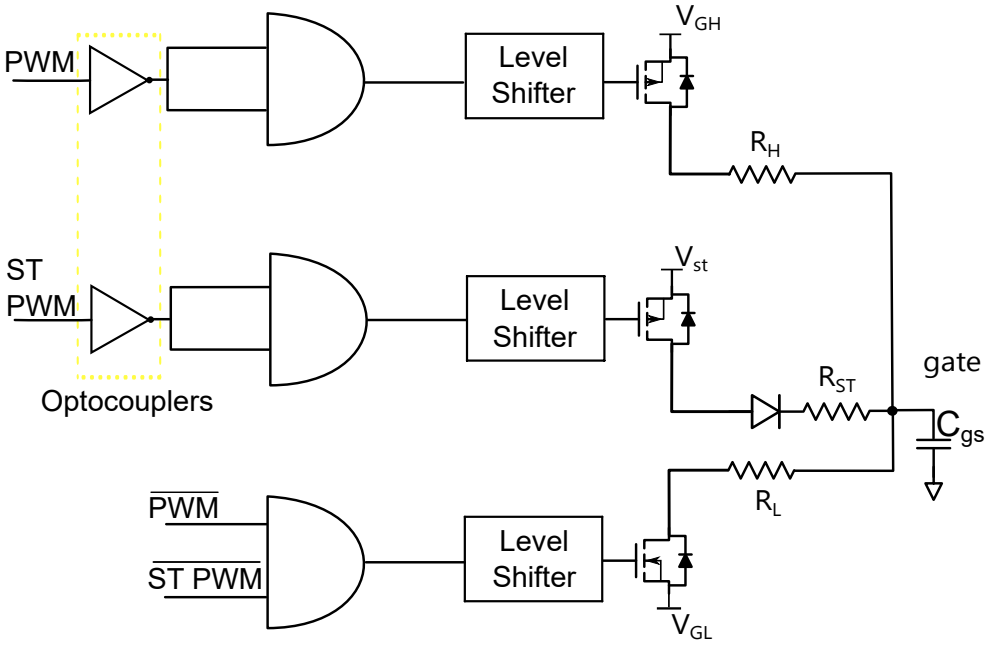


Figure 4.11: Gate driver scheme showing the modified ST branch and the normal push-pull path.

negated since the optocoupler is inverting, setting ST PWM and the PWM signals as inputs of an AND gate results sufficent to prevent undesirable conditions as visible in Fig. 4.12.

4.3.4 Voltage Clamper

In Fig. 4.13 the gate driver's embedded voltage clamper circuit as proposed in [101] is shown, M_C is the clamping MOSFET (with a breakdown voltage higher than V_{DC}) used to measure the DUT's v_{on} during its on-state and safely clamping the input DC voltage V_{DC} during its off-state. V_{ds} is the DUT's drain to source voltage (to be clamped or revealed), v_s is the sensed voltage and, V_B represents the biasing equivalent circuit of M_C and C_B is needed to desensitize biasing from the Miller current during rapid V_{ds} excursions. In this circuit M_C is always on. Its drain-source voltage is $v_{ds} = v_i - v_o$ and the gate-source voltage is $v_{gs} = V_B - v_o$. While $v_i > V_B - V_T$, M_C is in saturation region (DUT off or switching) and in linear region otherwise (DUT on). In the first case:

$$v_o^2 - 2v_o\left(V_B - V_T + \frac{1}{kR_d}\right) + (V_B - V_T)^2 = 0 \tag{4.7}$$

Choosing R_d and V_B such that $(kR_d)^{-1} \ll V_B - V_T$, obtaining $v_o \approx V_B - V_T$, the circuit clamps the off-state voltage. In the second case:

$$v_o^2 - 2v_o\left(V_B - V_T + \frac{1}{kR_d}\right) = v_i^2 - 2v_i(V_B - V_T) \tag{4.8}$$

which results in $v_o \approx v_i$, provided that the same approximation above holds. In this case the DUT's V_{on} is sensed. R_d value is chosen as a trade-off between the power dissipation of M_C and the requirement $R_d \gg [k(V_B - V_T)]^{-1}$.

4.4 Proposed Calibration Procedure

To use the selected TSEP as an online junction temperature indirect measurement, an individual device characterization is required, since even within the same production batch significant parameter dispersion may be observed [104]. The procedure

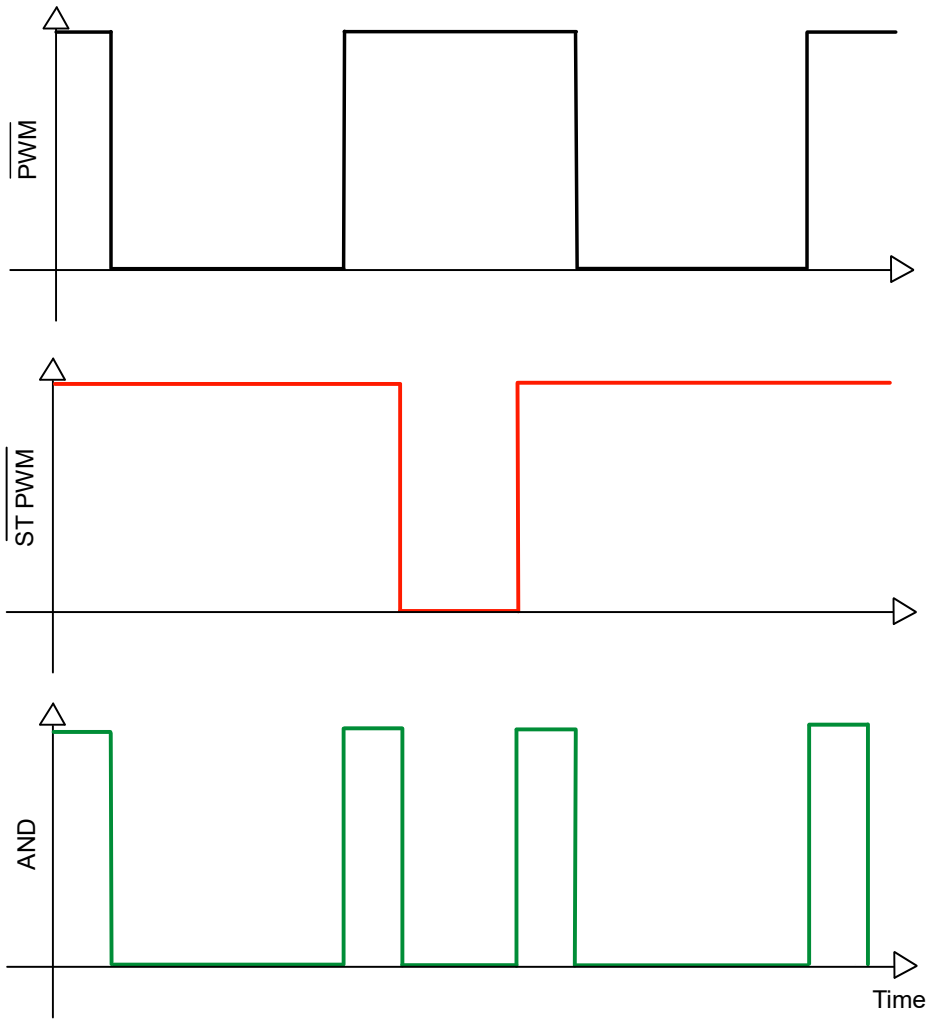


Figure 4.12: Logic operation of the circuit described in Fig. 4.11. In black the (negated) PWM gate driver control signal for normal switching operation. In red the (negated) ST PWM command signal defining the pulse for CST. In green, the logic AND between the two above-mentioned signals, which commands the gate drivers pull-down.

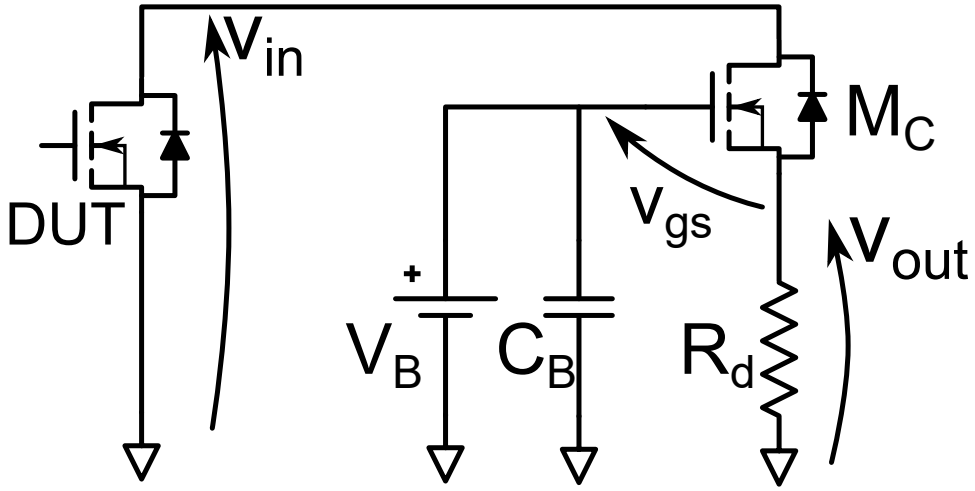


Figure 4.13: Clamping circuit Schematic adopted to read the on-state drain-source voltage V_{ds} of the DUT. MOSFET M_C acts as the clamping element.

is divided into two main phases: preliminary self-heating of the interested transistor, followed by a data collection phase during its natural cooling.

Fig. 4.14 shows a flowchart detailing the proposed calibration procedure, which starts by turning on the high-side (HS) device and commanding a repetition of shoot-through pulses for the low-side DUT, with frequency of 10 kHz, amplitude of 6 V, and duration of 2 µs. This gate pattern induces power dissipation in the transistor, steadily increasing its junction temperature until the desired maximum calibration temperature ($T_{j,max}$) is reached. Since the heatsink is not mounted, the heating process is quite rapid and requires very little power dissipation. Furthermore, with the insulating cap described in Chapter 4.2, the temperature difference between case and junction is reduced, enabling $T_{j,max}$ to be very close to the transistor maximum rated temperature (150 °C for the C2M0080120D).

Once the temperature measured by the DUT's NTC reaches $T_{j,max}$, the heating phase is concluded switching off the shoot-through pulse train. This starts the data acquisition process, where the junction temperature, drain current, and on-state volt-

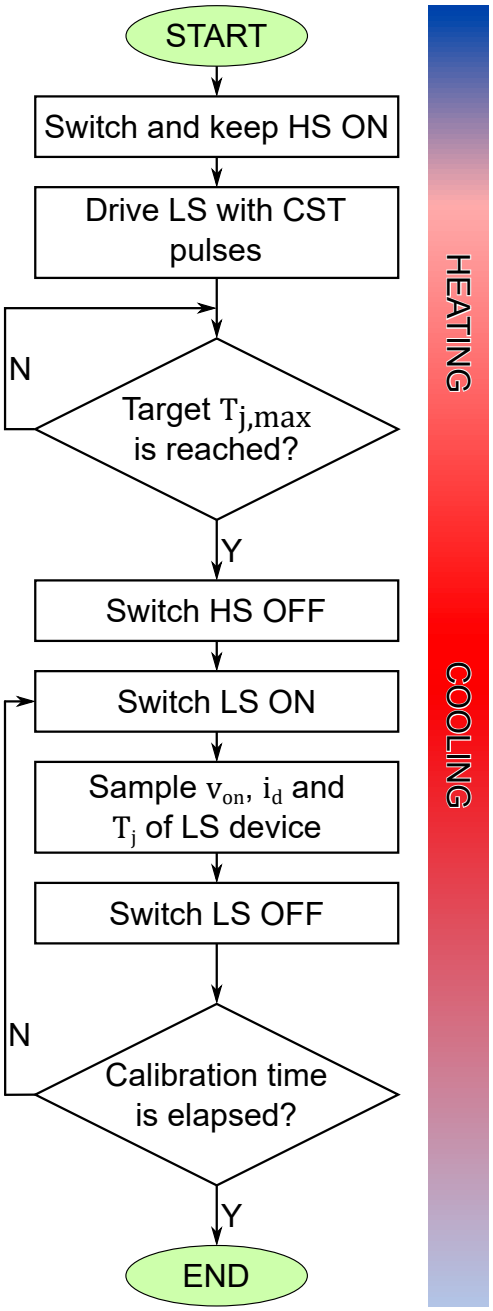


Figure 4.14: Flowchart of the CST-based characterization procedure. The DUT is initially heated using CST pulses, when the sensed temperature reaches $T_{j,max}$ the heating procedure stops. Then, during its cooling transient, a conventional PWM pulse is used to measure the on-state voltage, drain current and junction temperature.

age are simultaneously sampled using an oscilloscope. Furthermore, i_d is acquired using a dedicated current probe, while $v_{ds,on}$ is sampled directly at the output of the clamper circuit using a voltage probe. Regarding the junction temperature, the NTC is conditioned using a dedicated circuit and sampled with the ADC onboard the STM32F446 MCU. The microcontroller then sends the temperature information to the oscilloscope using a PWM signal. With this setup it is possible to synchronize the sampling of the calibration quantities, sequentially retrieving scope acquisitions while the DUT is cooling down. Thanks to the insulating cap, the cooling process is quite slow, allowing a low sample frequency of $1Hz$ for the present study.

Each second, the half bridge is driven with a conventional PWM pulse of 100 µs, where the HS device is off and the LS device is fully on. This imposes a constant voltage across the inductive load, producing a linearly increasing current with a final maximum value of around 20 A. This linear pattern is useful to sweep across the whole i_d range at each temperature point. After the aforementioned PWM pulse, the LS device is turned off and the measurement cycle starts again after the one second delay imposed by the selected sampling frequency. The cooling phase lasts a total of 15 min, after which the calibration procedure is complete, and all relevant data is saved and processed using MATLAB.

4.5 Experimental Results

All the considerations presented so far have been validated through several experiments, which results are reported here. Initially, the proposed procedure was tested along the peculiar thermal setup described in Chapter 4.2, to evaluate the adequacy of hardware and software platforms (Chapter 4.5.1). Using the collected experimental data, the different temperature estimation models, presented in Chapter 4.2, have been evaluated and compared (Chapter 4.5.2). Almost all of the post processing code necessary to achieve the results described in Chapter 4.5.1 and Chapter 4.5.2 has been developed by my colleague Enrico Panciroli. Finally, the proposed characterization technique is validated using a dedicated thermal chamber experiment (Chapter 4.5.3).

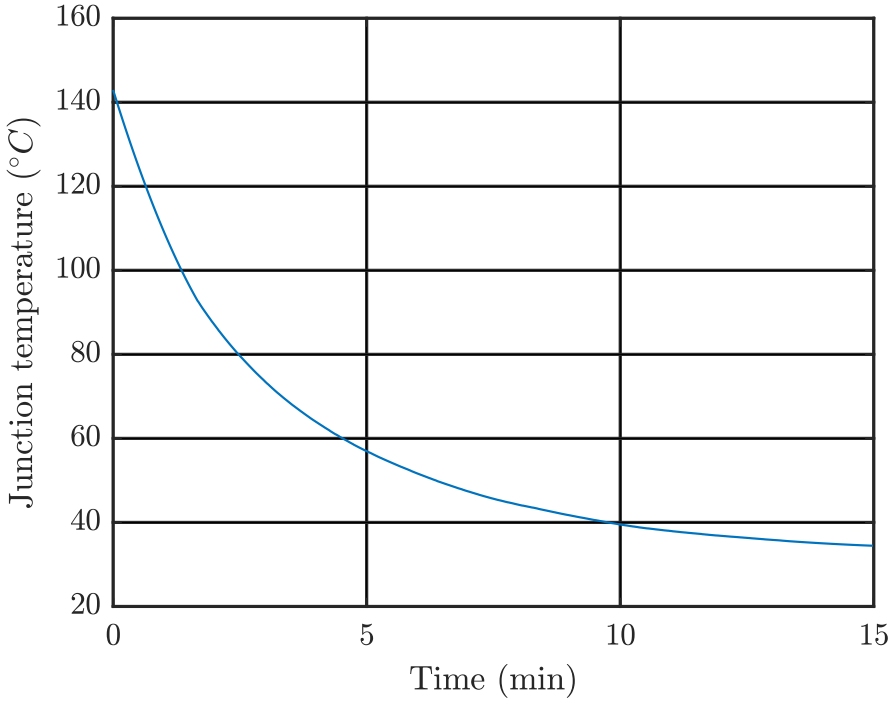


Figure 4.15: Junction temperature transient imposed on the DUT during the calibration procedure.

4.5.1 Device TSEP Characterization

A first experiment is performed to evaluate the effectiveness of the proposed hardware and software platform for transistor characterization. The half-bridge's low side MOSFET is heated using controlled shoot-trough pulses up to 145 °C and then cooled to 30 °C in the following 15 min. Fig. 4.15 depicts the resulting junction temperature transient acquired with the NTC sensor, where T_j is decaying exponentially with time. The temperature sensor is mounted on the metallic backside of the DUT, using a thin layer of thermal grease. The sensor and transistor combination is thermally insulated using the cork cap presented in Chapter 4.2.

While the DUT is cooling down, the on-state voltage is acquired using an oscil-

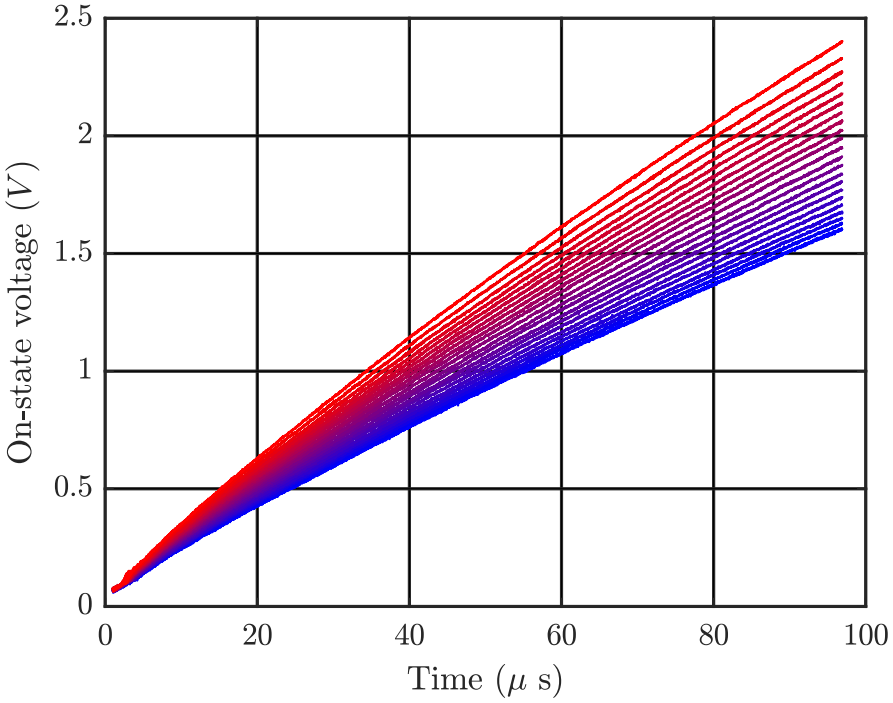


Figure 4.16: DUT on-state voltage v_{on} acquired during the calibration procedure.

loscope probe. Fig. 4.16 depicts the different v_{on} traces collected in the 100 µs PWM pulse showing a significant variation related to the temperature change.

At the same time, as shown in Fig. 4.17, i_d is increasing linearly during the calibration PWM pulse, exhibiting negligible temperature dependence.

Processing the voltage and current acquisitions, it is possible to obtain Fig. 4.18, depicting the MOSFET output characteristics. Only the linear operating region is visible due to the maximum test current of around 20 A. This upper limit is selected to contain the possible unwanted DUT self-heating occurring during the 100 µs measuring pulse.

Recalling (4.2), it is possible to obtain Fig. 4.19 detailing how the MOSFET on-state resistance is varying with current, through the various temperature acquisitions.

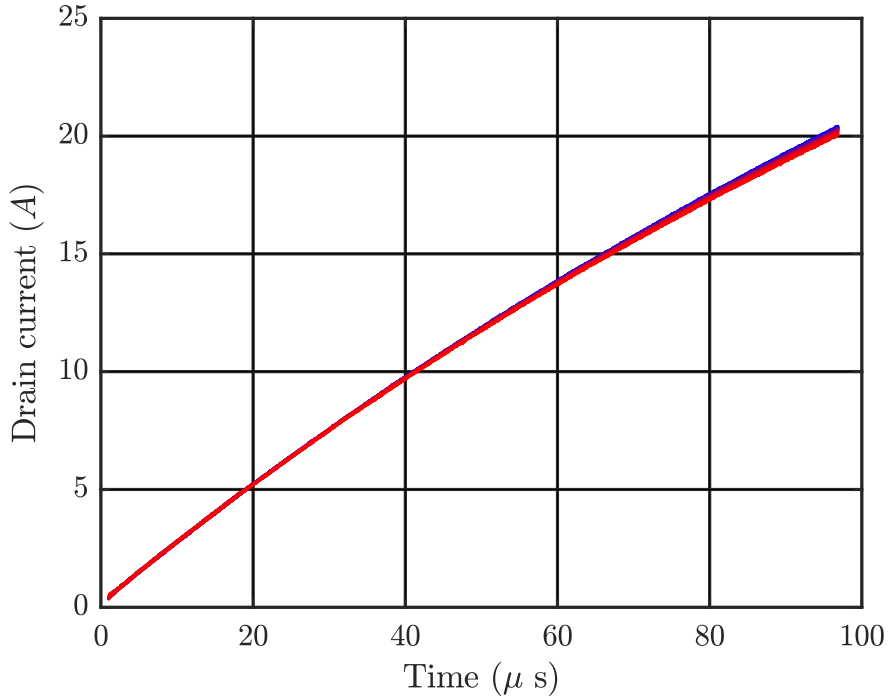


Figure 4.17: DUT current i_d acquired during the calibration procedure.

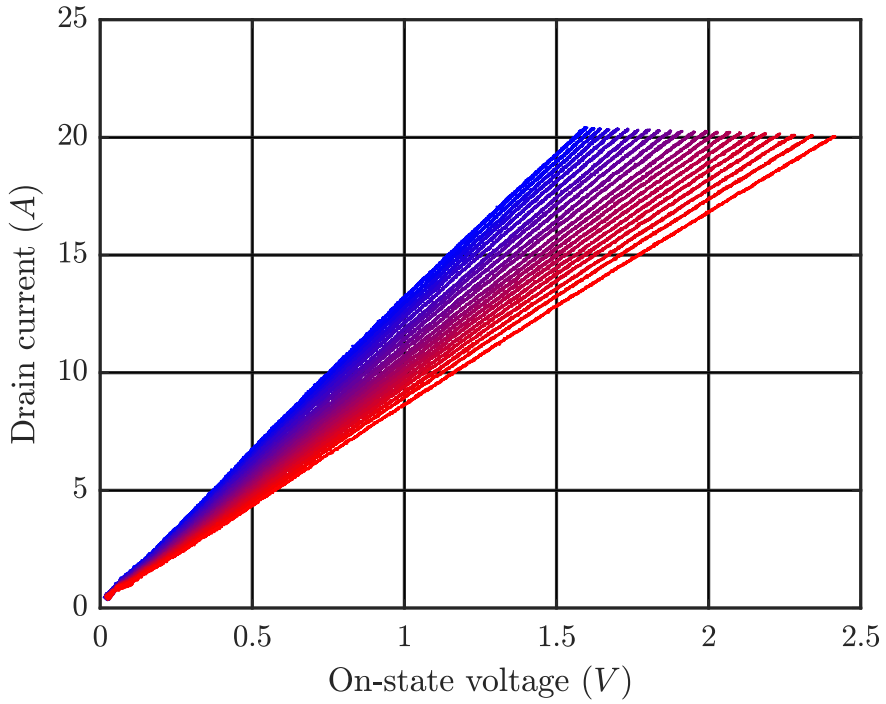


Figure 4.18: MOSFET characteristic reconstructed from the calibration data, evaluated at different temperatures, from blue (cold) to red (hot).

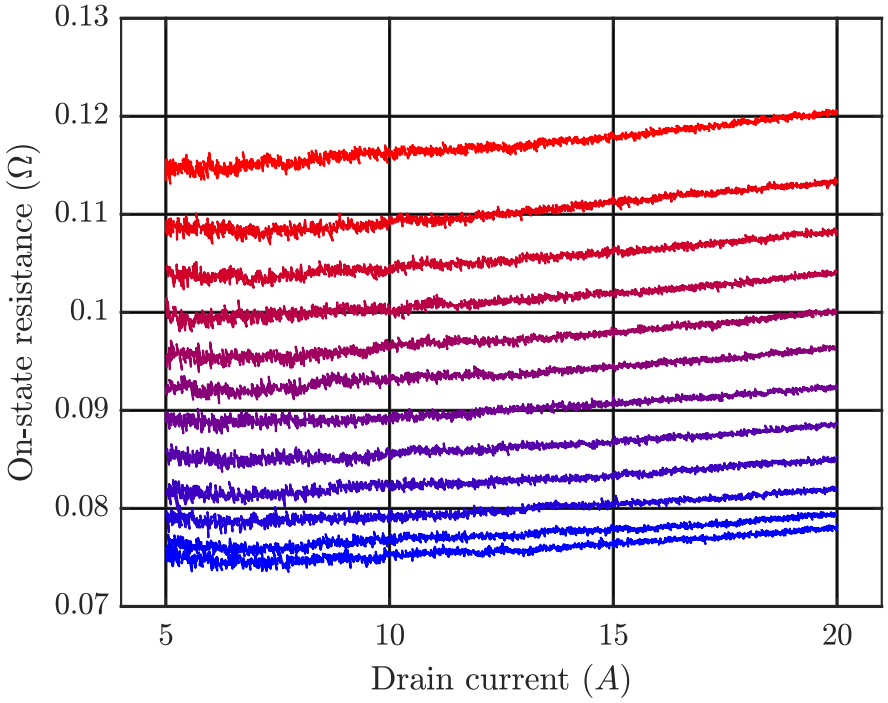


Figure 4.19: MOSFET on-state resistance as a function of drain current, evaluated at different temperatures, from blue (cold) to red (hot).

As anticipated, R_{on} shows a weak dependency upon the drain current, highlighting the intrinsic two-dimensional nature of the problem. The characteristic defined in Fig. 4.19 is only valid for the DUT and cannot be generalized for other SiC MOSFETs, not even from the same batch, so a similar calibration procedure will be needed for each MOSFET.

4.5.2 Temperature Models Comparison

In order to find the best temperature estimation approach, all the different models, listed in Chapter 4.2, are compared using the calibration data collected.

To obtain a more representative evaluation, the experimental dataset is divided in

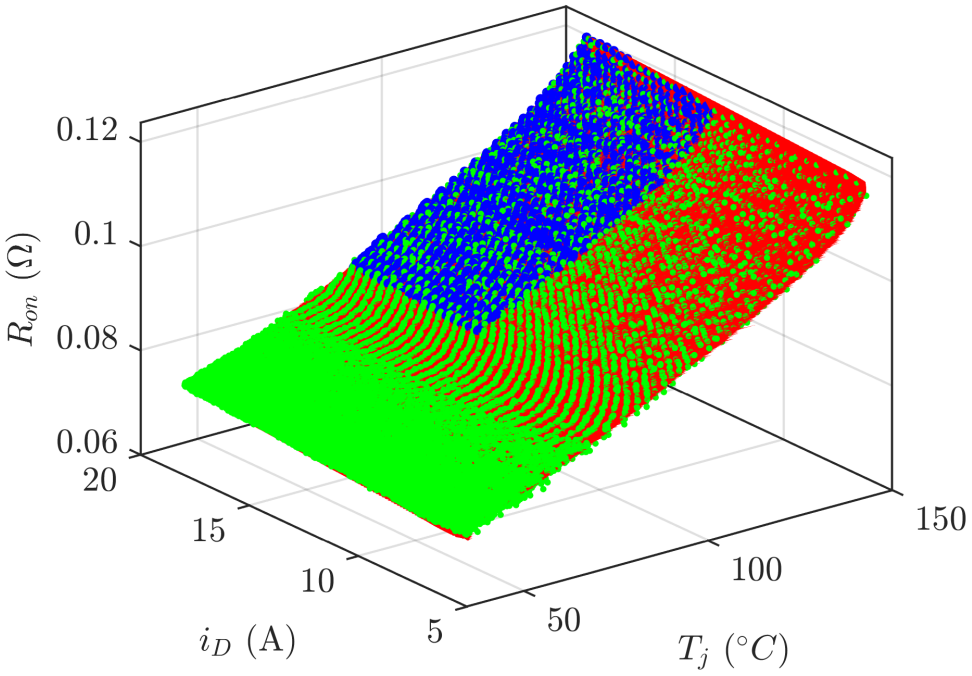


Figure 4.20: Full dataset of R_{on}–i_d–T_j triplets in green, the interpolated model in red and the restricted range validation dataset in blue.

two parts:

- **training dataset** comprising 2/3 of the experimental points shown in green in Fig. 4.20, used to synthesize the different models;
- **validation dataset** formed with the remaining 1/3 of those points, used to asses the performance of each temperature estimation model.

To investigate possible accuracy improvements, suggested by Shichman-Hodges, every model is evaluated twice: first considering the on-state resistance and using the drain current as the electrical quantity, and then considering the on-state conductance with the drain-source voltage as electrical quantity. Consequently, the compared models are: a two-dimensional interpolated look-up table (LUT), a fitted bivariate polynomial (BVP) model with second order on both temperature and the electrical quantity, and three "reduced" models (RM) constructed with just a few experimental points of the electrical quantity i_d or v_{ds}. The same fitting procedure is adopted for R_{on}–i_d and G_{on}–v_{ds} curves.

This comparison uses the root mean square (RMS) error on the junction temperature as figure of merit. The various models are stimulated using the validation dataset, using two different domain limitations. Initially, an extended range validation is performed, spanning from 5 A to 20 A in terms of drain current, and from 30 °C to 140 °C in temperature. The results of this test are listed in Table 4.1.

Furthermore, a restricted range validation is conducted, considering only the points of the calibration dataset for which i_d is above 12 A and T_j is over 80 °C as visible in Fig. 4.20. This second evaluation is used to investigate the behavior of each model simulating only the most thermically demanding scenario for the power converter. In these corner conditions, the accuracy of the junction temperature estimation is extremely important to maximize the output power without damaging the transistors. Table 4.2 reports the results of this second experiment.

Several interesting considerations emerged when analyzing the results of this comparison. First, using the on-state conductance instead of the on-state resistance (as suggested by the Shichman-Hodges model) does not yield any appreciable advantage. Even if SH suggests that on-state resistance is not polynomial in current,

Table 4.1: RMS errors of various models for the TSEP vs. junction temperature and current (or voltage). All the T_j points of the tuning dataset are used for all the models, while different numbers of electrical points, are used as specified. Errors are evaluated on a validation dataset, covering the whole domain of the functions.

Model	Number of i_d or v_{ds} points	i_d order/ v_{ds} order	T_j RMS error (°C) R_{on}	G_{on}
LUT	all	—	1.24	1.23
BVP	all	2	1.41	1.41
RM	3	2	1.83	1.84
RM	2	1	2.24	2.28
RM	1	0	4.94	5.12

Table 4.2: RMS errors of various models for the TSEP vs. junction temperature and current (or voltage). Errors are evaluated on a restricted validation dataset, considering a thermal and electrical worse case scenario.

Model	Number of i_d or v_{ds} points	i_d order/ v_{ds} order	T_j RMS error (°C) R_{on}	G_{on}
LUT	all	—	0.75	0.74
BVP	all	2	1.12	1.23
RM	3	2	1.67	1.70
RM	2	1	1.53	1.51
RM	1	0	1.91	2.08

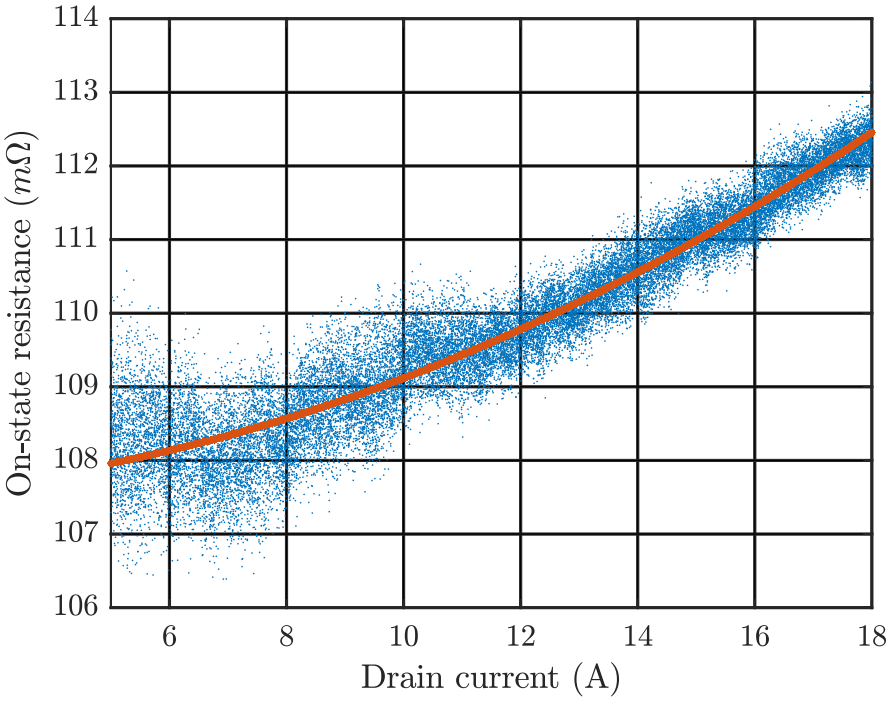


Figure 4.21: MOSFET on-state resistance as a function of drain current. Even if the Shichman-Hodges model foresees a non polynomial relationship, the second order polynomial fit (orange curve) well describes the experimental points (in blue), into the noise band of the measurement.

the error related to noise in the sampled quantities, is probably enough to mask a possible reduction in fitting error. This is further confirmed by Fig. 4.21, where the on-state resistance, supposed to follow (4.3), still fits very well with a second-order polynomial.

Furthermore, even the LUT-based model exhibits some error, slightly more than one degree in magnitude. This again is related to the noise affecting both voltage and current measurement, where the resulting error propagates to the inferred temperature.

Additionally, it is clear that increasing the number of calibration points used for the electric quantity yields a lower error. However, there is an outstanding result: even drastically reducing the number of current (or voltage) points has negligible impact on the overall accuracy.. Conversely, considering a limited number of electrical points dramatically simplifies the characterization procedure, which does not require a complete sweep on the current axis, but just a few strategically placed samples.

Concerning this matter, Fig. 4.22 shows how the RMS temperature error changes with respect to the current value used to synthesize the simplified reduced model. It is clear that the chosen current to evaluate the model strongly impacts the temperature error; in particular, it is notable how choosing a reduced evaluation domain biased to high current values goes to minimize the error precisely on the highest currents, which in dynamic diderating perspective turns out to be the optimal condition.

Finally, the evaluation performed considering the corner condition shows a reduced error. This is related to a lower SNR for both on-state voltage and drain current in the initial part of the current axis. As a result, all the models are intrinsically more accurate towards the upper portion of the temperature-current domain, when both quantities have higher magnitude. As mentioned before, this behavior is advantageous since the high current and temperature condition is the most stressful for the power converter.

4.5.3 Validation

As discussed in Chapter 4.2.1, being able to accurately sense the junction temperature, during the calibration procedure, is decisive to enhance the accuracy of the online estimation using the TSEP. In order to prove the effectiveness of chosen measurement setup, several dedicated experiments have been performed. In total, four different acquisitions are compared in Fig. 4.23.

The orange curve is obtained using a conventional thermal setup, in which the power device, in TO247 package, is attached with its back (metal side) to a heatsink via thermal interface material, and the NTC is placed on the top side of the device, where the die is covered by the epoxy.

The yellow and blue curves are obtained with the proposed altered thermal setup.

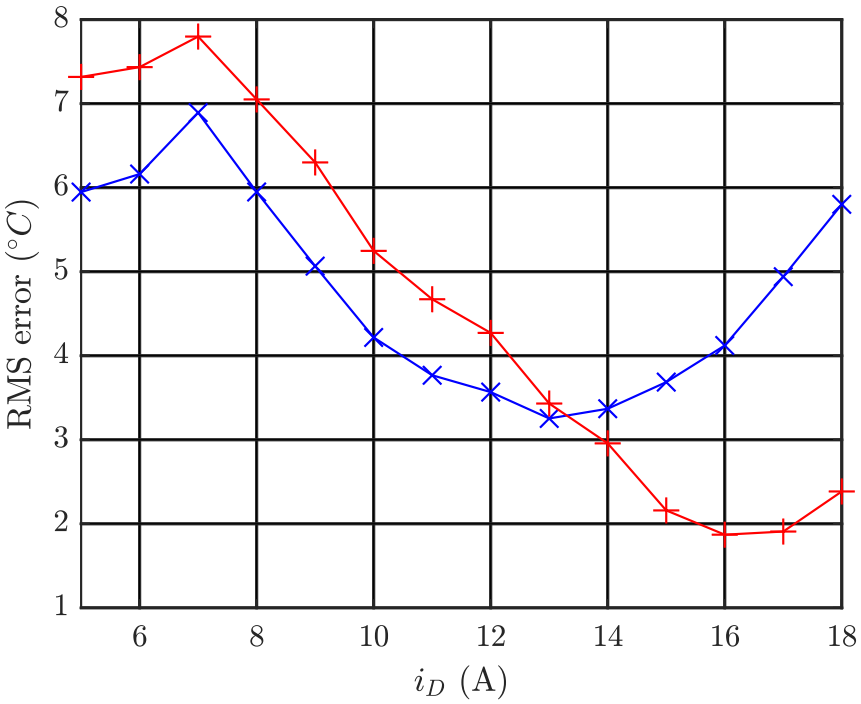


Figure 4.22: RMS error on the junction temperature as a function of the drain current value used to construct the reduced (simplified) temperature estimation model, in which R_{on} is considered constant with current. The blue curve refers to the error computed on the complete validation dataset, while the red curve considers only the restricted validation domain.

In this case the heatsink is not mounted, the power device and NTC sensor are coupled together and enveloped by the insulating cork cap. In particular, the blue trace is obtained attaching the NTC to the metal back side of the MOSFET, while the yellow one has the sensor connected on the top side.

Finally the purple curve is obtained placing the DUT and its NTC sensor inside a dedicated thermal chamber. In this test neither the heatsink nor the cork cap is mounted on the power transistor, and the NTC is attached to its back side with thermal grease.

Analyzing Fig. 4.23 various interesting results are observed. First, since the yellow and blue curves are almost superimposed, it is clear that the NTC positioning (top or bottom of the DUT), is irrelevant if the insulating cork cap is used. This indicates that such thermal setup is indeed able to reduce the heat flow toward the ambient, thus neutralizing any thermal resistance between junction and sensor.

Furthermore, even the purple curve is showing good agreement with the previous two. This result demonstrates that the insulating cap creates a thermal environment comparable with the one of the temperature-controlled chamber.

Conversely, the red curve appears dramatically discordant when compared with the rest. This is likely the result of a residual thermal path from the junction to the ambient, through the heatsink. The sensor occupies a side position (it is not part of the thermal path) and this results in a lower sensed temperature, for the same (real) junction temperature, i.e., for values with the same resistance. This proves that reference sensors must be placed in tight thermal contact of the device, and the cooling system must be modified to achieve practical results: here differences up to 40 °C are noticeable.

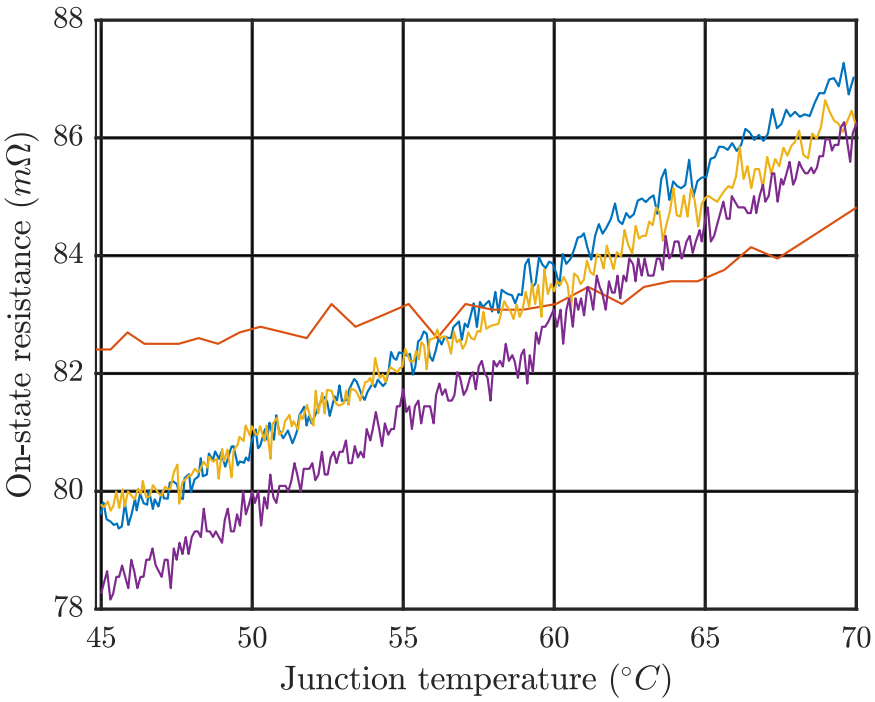


Figure 4.23: Coparison between $R_{on}(T_j)$ in different calibration setups: the proposed altered thermal setup adopting the cork cap with NTC attached on the device top side (yellow) and to the metal back side (blue). The DUT placed in the thermal chamber with NTC attached on the device back side (purple). The DUT attached with its back to a heatsink, and the NTC placed on the top side of the device (orange).

Conclusion

In this thesis a preliminary study on different aspects of an AC/DC/AC converter has been developed in perspective of a retrofit approach for reluctance motors.

Chapter 2 introduced a novel control methodology to regulate DC link voltage ripple using a standard boost front-end for Power Factor Correction (PFC), leveraging two separate duty cycle components to generate the switching command signal. This approach significantly reduced the required capacitance, enabling the use of long-life, low-ESR film capacitors instead of bulky electrolytic types, thereby enhancing reliability. A comparative simulation of five rectifier topologies demonstrates the proposed method's effectiveness across key performance metrics—including DC voltage stability, ripple reduction, power factor, and component sizing (inductor, capacitor, and RMS current). Additionally, a workflow for estimating capacitor lifetime in power converters is presented, with a focus on reliability improvements from substituting electrolytic capacitors with film capacitors as DC-link capacitors in boost PFC applications. In a case study, both capacitor types were evaluated as DC-link capacitors, examining power loss, thermal impact, and estimated lifetime under daily operating conditions. Monte Carlo analysis further confirmed the results, showing that film capacitors offer nearly twice the lifetime of electrolytic capacitors. Further work will deal with lifetime analysis for each component of the boost PFC, analyzing other aging mechanisms in order to define a complete reliability model for Boost PFC.

Chapter 3 presented the design and analysis of the Industrial Latching Current Limiter (ILCL), a converter topology that addresses the growing demand for fast fault detection and inrush current limiting in industrial power systems. The ILCL

offers high efficiency, fast switching speeds, and low power dissipation.

The design process involved optimizing the topology to handle over-current conditions and ensuring continuous operation under overloads. The inclusion of a bypass transistor and switching elements in a synchronous buck converter configuration allowed for both current limiting and fault management, while retaining the highest efficiency during normal operation. A hybrid control scheme, combining analog and digital elements, was implemented to ensure fast response times and precise control, further validating the effectiveness of the system.

The ILCL demonstrates interesting features, such as low power losses due to the bypass current path, enhanced reliability, and adaptability to industrial environments. Preliminary simulation results, using PLECS, validated the approach, suggesting the circuit feasibility for real-world applications. Future works will focus on optimizing the devices and inductor design to minimize area and further test the system to achieve full validation in industrial settings.

Chapter 4 proposed several ways that can be explored to improve the calibration procedure required to use the on-state resistance as TSEP for MOSFETs. The results presented in this study are helpful steps in achieving the ultimate objective: a completely in-circuit calibration.

Several novelty points have been proposed: the cooling system modification by using the cork cap, and some considerations about the best model to fit the acquired data, possibly reducing the number of current points.

The cork cap has been proven effective in cutting all the undesirable thermal paths and neutralizing the residual thermal resistance between sensor and junction. Additionally, it makes the heating and cooling phases much faster, since the heat capacity of the heat sink is not involved. The last test showed that there are no benefits in considering the conductance with respect to voltage instead of the resistance with respect to current, when extracting the model for the TSEP. However, we achieved a remarkable result: it is not necessary to sample the TSEP on all the current points, but only three of them are sufficient to narrow the error on the estimated temperature below 2 °C in absolute terms and 0.75 °C with respect to the LUT model, which expressed the baseline noise descending from the noise on the primary measured quantities. In summary, this work shows several improvements that can be applied in

the in-circuit characterization of the on-state resistance as TSEP, to achieve better accuracy. Future developments will focus on a new hardware platform to improve and accelerate the process to other transistor devices characterization. Futhermore a totally in-circuit methodology will be explored eliminating the needs for an expensive and not integrable oscilloscope.

This thesis touched on several topics, however, many things remain to be done, and further studies and developments can be carried out to improve the system's efficiency and integration. However, the studies carried out in this work can be a milestone for future developments.

Appendix A

List of Publications

- Alex Musetti, Hossein Sadegh Lafmejani, and Alessandro Soldati. Control and design of a boost-based electrolytic capacitor-less single-phase-input drive. Energies, 15(16), 2022.
- Alex Musetti, Hossein Sadegh Lafmejani, and Alessandro Soldati. From reliability study on front-end capacitorsin boost pfc architectures. In 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), pages 1–8, 2023.
- Alex Musetti, Enrico Panciroli, Hossein Sadegh Lafmejani, and Alessandro Soldati. A High-efficiency Resonant Driver and Soft Decoder Interface with Fast-dynamics PLL-Type Angle and Speed Tracking Observer for Resolvers," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 5087-5092.

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