UNIVERSITÀ DEGLI STUDI DI PARMA

Dottorato di Ricerca in Tecnologie dell'Informazione

XVIII Ciclo

Design Strategies and Modelling of Low-Power Sigma-Delta Analog-to-Digital Converters

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Gennaio 2016

To my love

To my family

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List of Abbreviations

ΣΔ	Sigma Delta	ΣΔ **FOM**	Sigma Delta FOM
ΣΔ**M**	Sigma Delta Modulator	**MASH**	Multistage Noise Shaping
PCM	Pulse Code Modulation	**A/D**	Analog to Digital
IC	Integrated Circuit	**ADC**	A/D Converter
AAF	Anti Aliasing Filter	**CIFF**	Cascade of Integrators with Feed Forward
S/H	Sample and Hold	**CT**	Continuous Time
FS	Full Scale	**D/A**	Digital to Analog
LP	Low Pass	**DAC**	D/A Converter
HP	High Pass	**DT**	Discrete Time
BP	Band Pass	**ENOB**	Effective Number of Bits
BS	Band Stop	**GBW**	Gain Bandwidth
MS	Mean Square	**SR**	Slew Rate
FOM	Figures of Merit		

PM	Phase Margin
CDS	Correlated Double Sampling
CHS	Chopper Stabilization Technique
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PSD	Power Spectral Density
SC	Switched Capacitor
STF	Signal Transfer Function
SNR	Signal to Noise Ratio
SNDR	Signal to Noise plus Distortion Ratio
DR	Dynamic Range
SFDR	Spurious-Free-Dynamic-Range
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration
KCL	Kirchhoff's Current Law
LHP	Left Half Plane
RHP	Right Half Plane
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ratio
CMFB	Common Mode Feedback
CM	Common Mode
QFN	Quad Flat No-leads
PCB	Printed Circuit Board
MIM	Metal Insulator Metal
FPGA	Field Programmable Gate Arrays
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
FIR	Finite Impulse Response

IIR	Infinite Impulse Response		Arithmetic
DA	Distributed	**LUT**	Look-Up Table

Nomenclature

f_B	Signal frequency band
f_{CK}	Sampling frequency
V_{CM}	Common mode voltage
V_{DD}	Power supply
V_{REF_P}	High reference voltage
V_{REF_N}	Low reference voltage
T	Absolute temperature
k	Boltzmann constant
f_t	Unity-gain transition frequency
ω_t	Unity gain transition angular frequency
v_{th}	Thermal voltage
ω_o	Natural angular frequency
ξ	Damping ratio
μ	Carrier electrical mobility
c_{ox}	Gate oxide capacitance per unit area
V_{cmfb}	Common mode feedback voltage

Abstract

Today, portable devices have become the driving force of the consumer market and new challenges are emerging to increase the performance, while maintaining a reasonable battery life-time. The digital domain is the best solution for implementing signal processing functions, thanks to the scaling of CMOS technology, which is pushing toward deep sub-micron integration level. Indeed, the reduction of the voltage headroom introduces severe constraints for achieving an acceptable dynamic range in the analog domain. Lower cost, lower power consumption, higher yield, and higher reconfigurability are the major advantages of using digital signal processing. Since more than a decade, several analog functions have been moved in the digital domain. This evolution means that the analog-to-digital converters (ADCs) are becoming the key components in many electronic system. They are, indeed, the bridge between the analog and the digital worlds, and therefore, their efficiency and accuracy often determine the overall system performance.

$\Sigma\Delta$ converters are the key block in high-resolution, and low-power mixed-signal interfaces. Efficient modelling and simulation tools are essential in the design flow. Although transistor-level simulation is the most accurate approach, this method is extremely time consuming due to oversampling nature of this converter type. For this reason high-level behavioural models of the modulator are mandatory for the designer in order to enable fast simulations and to identify the specifications leading to the required converter performance. The focus of this thesis is on behavioural modelling of $\Sigma\Delta$ modulator, addressing several nonidealities such as the integrator's dynamics and thermal noise. Results from transistor-level simulations and experimental data demonstrate the model to be valid and accurate when compared to behavioural simulations.

Chapter 1

Introduction

Engineering is a great profession. There is the fascination of watching a figment of the imagination emerge through the aid of science to a plan on paper. Then it moves to realisation in stone or metal or energy. Then it brings homes to men or women. Then it elevates the standard of living and adds to the comforts of life. This is the engineer's high privilege.

– Herbert Clark Hoover

Sigma Delta ($\Sigma\Delta$) data converters have received a lot attention in several fields of signal acquisition and processing, such high-quality digital audio, instrumentation and measurement, integrated transducer and sensor applications. With the scaling of Integrated Circuit (IC) technologies, digital signal processing systems have supplanted their analog counterparts in many applications. Indeed, digitally processed signals usually originate in the analog domain and once processed must be returned to the analog domain. The proliferation of digital processing systems has generated the need of high-performance Analog to Digital (A/D) and Digital to Analog (D/A) converters. The increase of signal processing rates, due to scaling of IC technologies, has led to the replacement of analog signal processing circuits by digital signal processing systems. In audio, video, communications and many other application areas, analog techniques have been replaced by their digital counterparts. Digital signal processing has numerous advantages over analog signal processing such as flexibil-

ity, noise immunity, reliability and potential improvements in performance and power consumption by IC technology scaling. The requirements of analog interface circuits between the analog world and the digital signal processing system in the form of A/D Converter (ADC)s, have become increasingly higher in terms of resolution and power consumption.

Sigma Delta Modulator (ΣΔM) finding an increase research field for high resolutions and narrow bands applications, such as sensor interface and digital audio applications. However designing a ΣΔM requires a proper understanding of its operation principle. In this Chapter a general background knowledge of the ΣΔ conversion and its benefits for medium-high resolution applications are explained. Furthermore, converter specifications, giving the general information and describing the features and limits of the modulator are discussed here.

1.1 A Brief Overview of ΣΔ Concepts

Applications such as sensor interface, digital audio and high resolution industrial measurement applications, where the signal bandwidth is much less than the operating speeds typical in digital circuits, take advantage of a technique called ΣΔ modulation can be used to achieve high resolution performance. The ΣΔ ADC architecture had its origins in the Pulse Code Modulation (PCM) systems. PCM is a method used to digitally represent sampled analog signals. It is the standard form of digital audio in computers, digital telephony and other digital audio applications. In a PCM stream, the amplitude of the analog signal is sampled regularly at uniform intervals, and each sample is quantized to the nearest value within a range of digital steps, Fig 1.1.

To be able to process data by digital techniques, we needs to transform the analog world to digital form, as depicted in Fig. 1.2a [1]. An example could be sensor data that have to be processed, signal $x_a(t)$. Best way to look into the data is often by digital signal processing, but sensors provide analog voltages (or current or charge) as data. Here one wants to convert these analog signals to digital discrete values. The analog signal is filtered by an Anti Aliasing Filter (AAF), sampled by Sample and Hold (S/H) circuit, divided into Discrete Time (DT) samples after quantization,

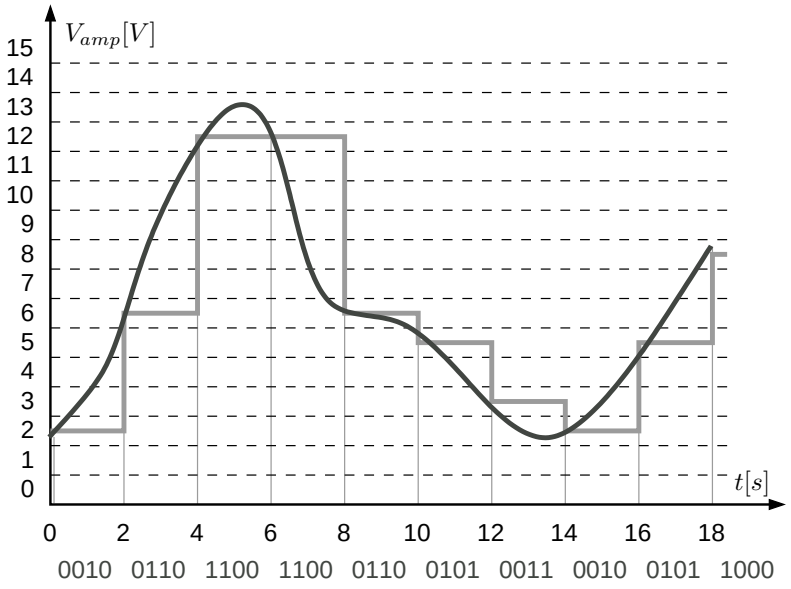


Figure 1.1: PCM sampling technique.

with the time of the sample period T_s between each sample. The digital data are samples quantized to 2^N discrete levels for N number of bits. The more bits, the more accuracy is achievable. Finally, the coder assigns a unique binary number to each level providing the output digital data. Fig 1.2b shows the fundamental process involved in an A/D conversion. The analog input signal, $x_a(t)$, passes through the AAF block. From the Nyquist sampling theorem, high frequency components of the input signal would be aliased into the signal bandwidth, f_B, thus corrupting the signal information. The band limited signal, $x_b(t)$, is sampled at frequency f_s by the S/H circuit, resulting in a DT signal, x_s. The quantizer maps the range of amplitudes into a discrete set of levels. The coder assigns a binary number to each level providing the output digital data.

The operation of ΣΔ converters relies on the combination of two signal processing techniques: oversampling and noise shaping. Both techniques, applicable to both A/D and D/A conversion, are related to the fundamental processes involved in an ADC. In a ΣΔ modulator, a combination of oversampling, negative feedback, and filtering

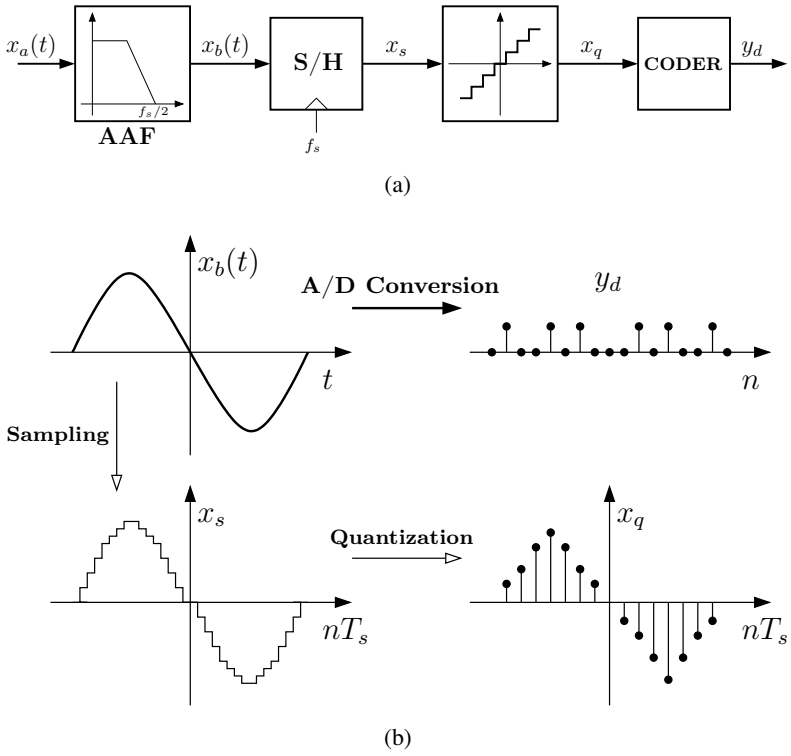


Figure 1.2: Conceptual ADC. (a) Basic block diagram. (b) Signal processing.

is used to trade speed for resolution.

1.1.1 Oversampling

The sampling process imposes a limit on the frequency band of the ADC, f_B, and hence on the maximum speed. According to the Nyquist theorem, setting the minimum value of the sampling frequency f_s equal to:

$$f_s = 2 \cdot f_B \tag{1.1}$$

Based on this criterion, (1.1) defines the Nyquist-rate ADCs, while in the cases where:

$$f_s > 2 \cdot f_B \tag{1.2}$$

the resulting ADCs are known as oversampling ADCs, and the Oversampling Ratio (OSR) is defined as:

$$OSR = \frac{f_s}{2 \cdot f_B} \tag{1.3}$$

One of the advantages of oversampling ADCs compared to Nyquist ADCs is that they relaxed the requirements placed on the AAF as illustrated in Fig. 1.3. Note that the AAF for a Nyquist converter must have a sharp transition band, which often introduces phase distortion in signal components located near the cut-off frequency [2].

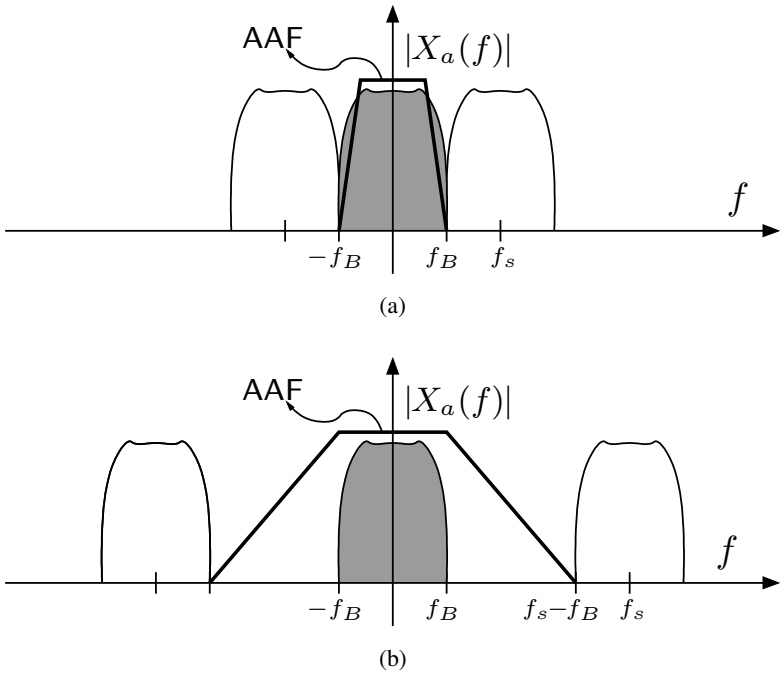


Figure 1.3: AAF requirements for Nyquist rate (a) and oversampling (b) ADCs.

1.1.2 Quantization Noise

The quantization introduces a limit on the maximum achievable resolution of an ADC. The conversion between continuous and discrete values generates an error,

commonly referred as quantization error [3]. Fig. 1.4a shows the transfer characteristic of an ideal quantizer, where k denotes the quantizer gain. $e_q(x)$, reported in Fig. 1.4b, stands for the quantization error. If x is confined to the Full Scale (FS) input range, $[-X_{FS}/2, +X_{FS}/2]$, the quantization error is bounded by $[-\Delta/2, +\Delta/2]$. Δ is the quantization step, defined as the separation between adjacent output levels in the quantizer. Consider Y_{FS} the FS output range of the quantizer and B-bit the nominal resolution of the quantizer, the quantization step is defined as $\Delta \equiv Y_{FS}/(2^B - 1)$. The overloading of the quantizer occurs for inputs outside interval $[-X_{FS}/2, +X_{FS}/2]$. In this situation the absolute value of $e_q(x)$ exceeds $\Delta/2$ and grows monotonically. Under some assumptions, normally met in practice [4], the quantization error is distributes uniformly in the range $[-\Delta/2, +\Delta/2]$, with a rectangular probability density $\rho_e(e_q)$ having a constant Power Spectral Density (PSD). Thus the quantization noise is modelled as an additive white noise source, e, called quantization noise, as represented in Fig. 1.5. The total quantization noise power, $\sigma^2(e)$, is uniformly distributed in the range $[-f_s/2, +f_s/2]$, its two-side PSD is given by:

$$S_E(f) \equiv \frac{\sigma^2(e)}{f_s} = \frac{1}{f_s} \cdot \left(\frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 \, de \right) = \frac{\Delta^2}{12 \cdot f_s} \tag{1.4}$$

The in-band noise power, calculated for Low Pass (LP) signals as:

$$P_E(f) \equiv \int_{-f_B}^{+f_B} S_E(f) \, df = \frac{\Delta^2}{12 \cdot OSR} \tag{1.5}$$

decreases with OSR at a rate of 3-dB/ocave. Intuitively, when an oversampled signal is quantized, the spectral components of the quantization error are distributed in a larger frequency band, as illustrated in Fig. 1.6. This effect effectively attenuated the in-band quantization noise power compared to Nyquist-rate ADCs. In fact assuming f_{s_1} the Nyquist sampling frequency, for an oversampled ADC with a sampling frequency f_{s_2} or f_{s_3} the in-band quantization noise is considerably attenuated.

1.1.3 Noise Shaping

The accuracy of an oversampling ADC is further increased by filtering the quantization noise in such a way that most of its power lies outside the signal band. This

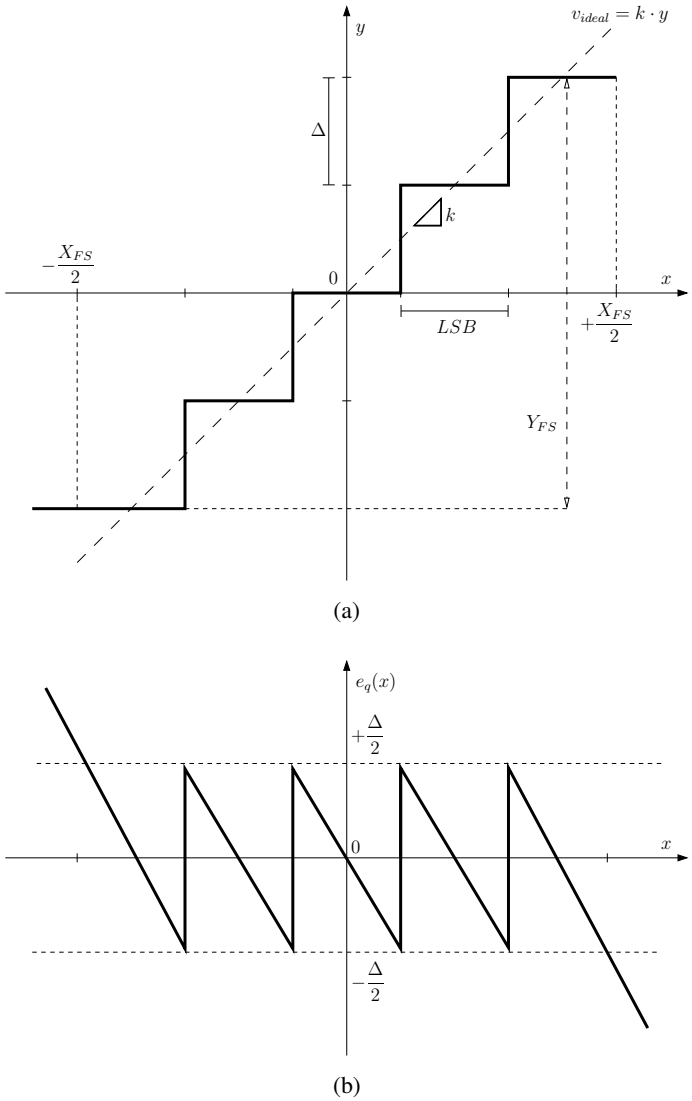


Figure 1.4: Quantization process. (a) Ideal characteristic. (b) Quantization error.

is illustrated conceptually in Fig. 1.7, where the quantization error, e_q, with white noise PSD is filtered by a transfer function called Noise Transfer Function (NTF). The NTF can be either High Pass (HP), for low frequency signals, or Band Stop (BS)

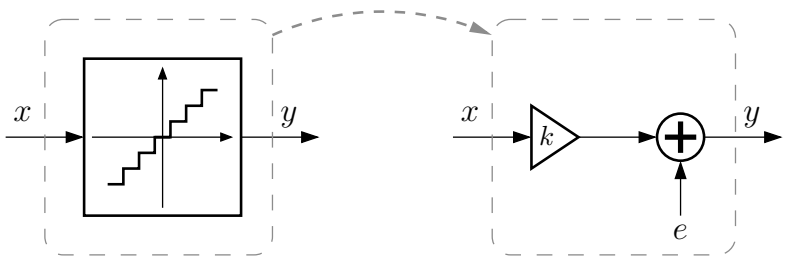


Figure 1.5: Equivalent linear model for the quantizer.

at a given frequency, for communications system. In the case of study, for LP signals, the Z-domain NTF is given by:

$$NTF(z) = \left(1 - z^{-1}\right)^L \tag{1.6}$$

were L stands for the filter order [3]. Taking into account that $z = e^{j2\pi f/f_s}$ and assuming $OSR \gg 1$, the in band filtered noise power can be approximated as [3]:

$$P_Q \equiv \int_{-f_B}^{+f_B} \frac{\Delta^2}{12 \cdot f_s} \cdot |NTF(f)|^2 \, df \simeq \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)\, OSR^{2L+1}} \tag{1.7}$$

which decreases with OSR by approximately $6L$ dB/octave more than just using only oversampling as in (1.5).

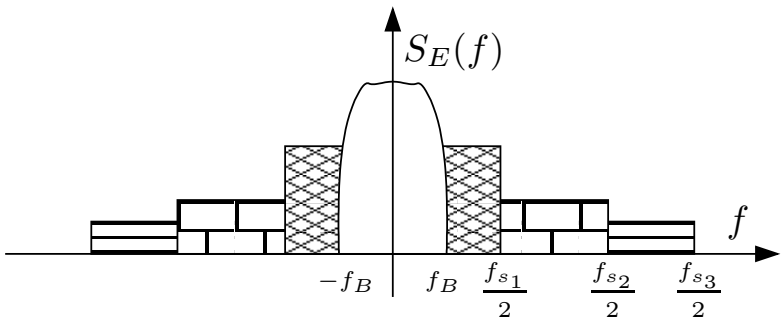


Figure 1.6: Oversampling effect on the in-band noise power.

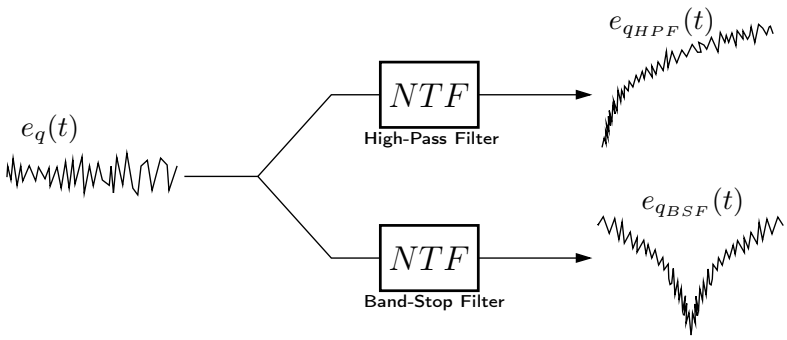


Figure 1.7: Noise shaping effect for quantization noise $e_q(t)$. HP or BS filtered.

1.1.4 ΣΔ Modulation

Both techniques, oversampling and noise shaping, with a quantizer in a feedback loop are used to build a ΣΔ ADC, as illustrated in Fig. 1.8. The loop filter has a gain, $H(z)$, large inside the signal band and small outside it. Under the assumption that the quantization noise is modelled as white noise, the system can be represented in the Z-domain [3]:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \tag{1.8}$$

where $X(z)$ and $E(z)$ represent the Z-transform of the input signal, $x(t)$, and of the quantization noise, $e(t)$. $STF(z)$ and $NTF(z)$ stand for the signal and noise transfer functions. Recalling the equivalence reported in Fig. 1.5, the $STF(z)$ and $NTF(z)$ are given by:

$$STF(z) = \frac{k \cdot H(z)}{1 + k \cdot H(z)} \tag{1.9}$$

$$NTF(z) = \frac{1}{1 + k \cdot H(z)} \tag{1.10}$$

Note that, if the loop filter gain $|H(f)| \to \infty$ within the signal band, then $|STF(f)| \to 1$ and $|NTF(f)| \to 0$. However the quantization error cannot be nulled because $H(z)$ has a limited gain.

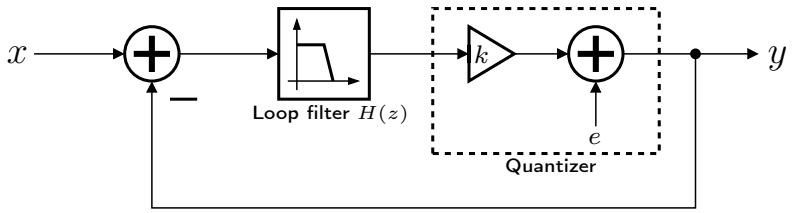


Figure 1.8: Conceptual block diagram for a generic ΣΔ modulator.

1.1.5 Architectures of ΣΔ ADCs

Fig. 1.9 shows the basic block diagram of a ΣΔ ADC for a DT implementation. In this case LP signals are considered. The converter is based on two main blocks: a ΣΔ modulator and a decimator filter. The sampling of the input signal is implemented through S/H at the modulator input. The output, y, is a DT signal and the conversion to Continuous Time (CT) signal is obtained by the D/A Converter (DAC). The output of the ΣΔM is a N-bit digital stream clocked at f_s. The decimator block is a digital circuit, removing the quantization noise at frequency components out of the signal band, f_B. It also decimates, in order to reduce the rate of the output stream y, down to the Nyquist frequency. Hence, the output is a digitized value of the analog input.

ΣΔMs reported in literature are usually implemented using Switched Capacitor (SC) circuits. However the increasing demand for ever faster and high resolution ADCs in broadband communication system has boosted the interest in CT implementations. These modulators are able to operate at higher sampling rates with low power consumption compared to their DT counterparts [5]. Also the architecture presents several differences. Apart from the CT circuit nature of the loop filter, the most significant differences are related to the point where the sampling process takes place, which constitutes one of the key advantages of the CT ΣΔM over their DT counterparts [6].

According to the nature of the signals being handled, a LP or Band Pass (BP) ΣΔM architecture is adopted. The number of bits of the internal quantizer divides ΣΔM into single-bit and multi-bit topologies. The number of the quantizers employed in the modulator give different topologies, namely: single-loop, cascade, dual quan-

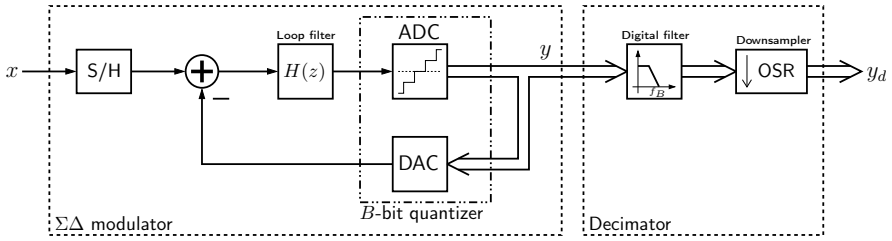


Figure 1.9: Generic block diagram ΣΔ modulator.

tization, etc. Describing all the possible ΣΔMs architectures is beyond the scope of this work, a detailed study of them can be found in [3].

1.1.6 Low-Order Single-Loop ΣΔ Modulator

Usually single-loop ΣΔMs use a 1-bit quantizer and DAC making the modulator insensitive to transistor mismatch, and inherently linear. The simplest ΣΔ architecture is shown in Fig. 1.10a. It is a first-order loop with a DT filter consisting of a single integrator with delay. The modulator implements the quantization function with a 1-bit ADC. By inspection of the circuit, the output of the modulator in the Z-domain can be obtained. The input signal is passed through a delay while the quantization noise is processed by the HP transfer function, $(1-z^{-1})$. This transfer function gives a first-order noise shaping behaviour, thus the architecture of Fig. 1.10a is called first-order ΣΔM. Higher order ΣΔMs can be obtained by adding more than one integrator in the forward path. These kinds of architectures obviously provide high-order noise transfer functions and give the potential of increased resolution, but at the same time raise special design challenges for stability [3]. Fig. 1.10b and Fig. 1.10c show the block diagrams of a conventional second and third-order modulator.

Fig. 1.11 shows the conceptual comparison of the noise shaping behaviour of the architectures of Fig. 1.10. Since with a first-order ΣΔM it is necessary to use high sampling frequencies to achieve high resolution, better performance and features are obtained by using two or three integrators in the loop. At low frequencies, the NTF of the first and second-order modulator are 20-dB/decade slope and 40-dB/decade slope

respectively, while the NTF of the third-order modulator has a 60-dB/decade slope.

1.1.7 High-Order Single-Loop ΣΔ Modulator

The concept underlying first, second and third-order single-loop ΣΔM can be extended towards *L*th-order filtering, thus resulting in the modulator topology shown in Fig. 1.10d. Using the linear model for the quantizer, the $STF(z) = z^{-L}$ and $NTF(z) = (1-z^{-1})^{L}$. However stability problems arise, and stability can only be guaranteed for a limited range of input amplitudes when $L > 2$ [3]. A common disadvantage is the increased circuit complexity due to the presence of a large number of analog blocks [7]. A well-known alternative to circumvent instability while obtaining high order noise shape consists of using the Multistage Noise Shaping (MASH) topology. Each stage, consisting of first or second-order single-loop ΣΔM, modulates a signal that contains the quantization error generated in the previous stage. This error is thus shaped by a transfer function whose order equals the sum of the respective orders of all the stage in the cascade. A detailed analysis is reported here [3].

1.2 Figures of Merit

At this point, it is convenient to define the Figures of Merit (FOM) commonly used to characterize the oversampling converters. These give general information and describe the features and limits of the modulator. The most popular specifications and its technical terms are explained as follows. Performance metrics Signal to Noise Ratio (SNR), Signal to Noise plus Distortion Ratio (SNDR) and Dynamic Range (DR) are conceptually represented in Fig. 1.12.

- **SNR**. The SNR defines how much a signal has been corrupted by noise. The SNR is defined as the power ratio between the signal and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the frequency band of interest. Moreover the SNR can depend on the frequency of the input signal and it decreases proportionally to the input amplitude. Because many signals have a very wide dynamic range, the SNR is often

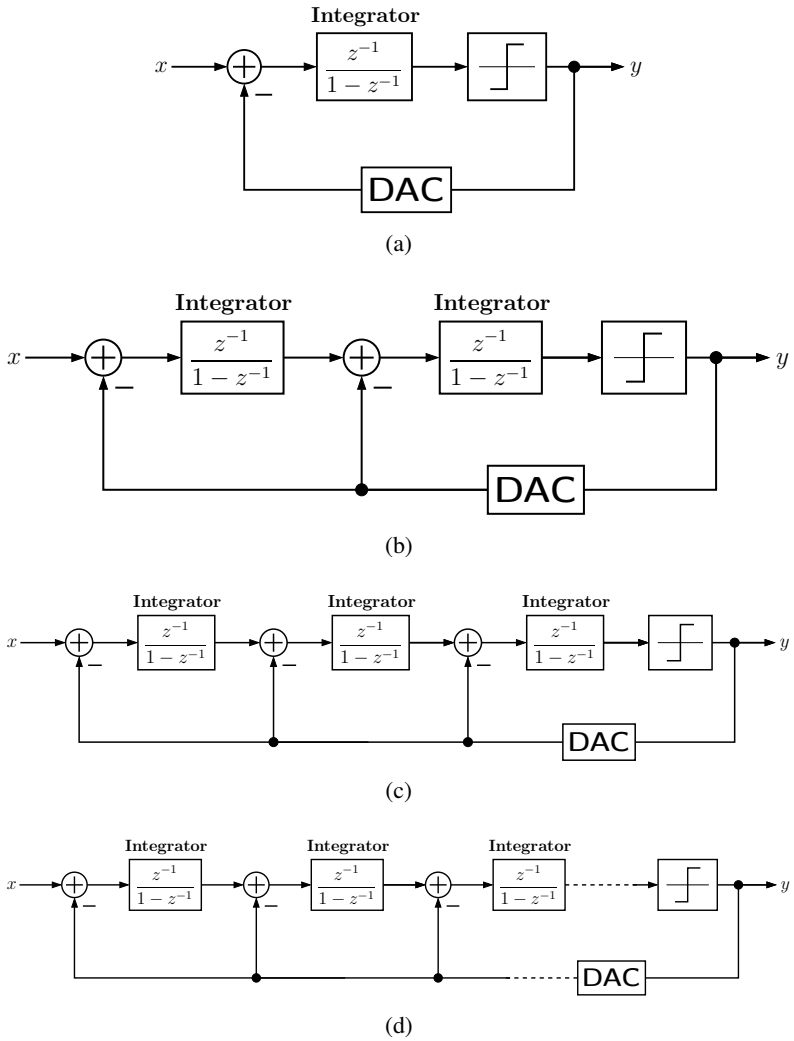


Figure 1.10: ΣΔMs architectures. (a) First-order ΣΔM. (b) Second-order ΣΔM. (c) Third-order ΣΔM. (d) *L*th-order ΣΔM.

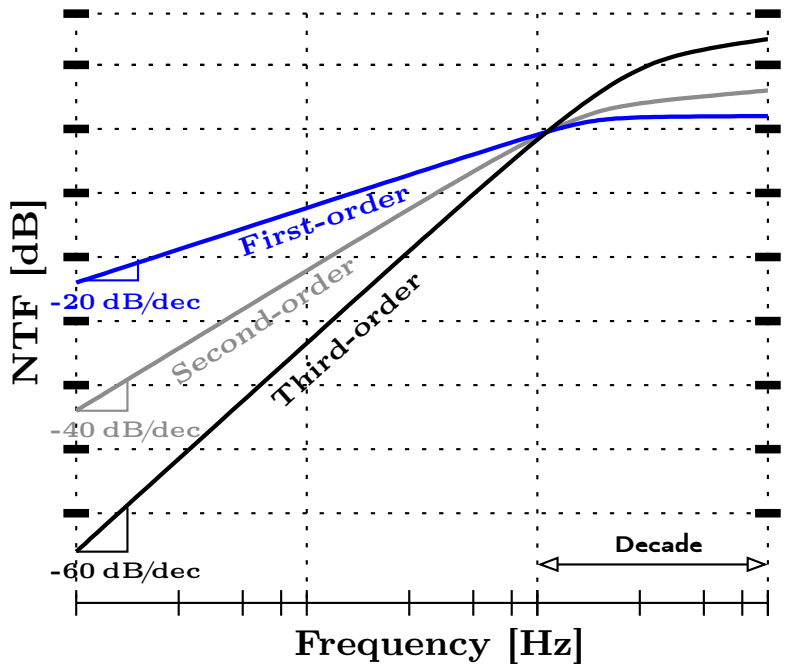


Figure 1.11: Conceptual noise shaping comparison.

expressed using the decibel scale (dB) and defined by:

$$SNR|_{dB} = 10 \cdot \log_{10} \frac{P_S}{P_N} \tag{1.11}$$

where P_S and P_N are the power of the signal and the power of the noise in the band of interest.

- **SNDR or SINAD**. If distortion contribution, produced by the ADC are considered together with noise, SNDR (or SINAD) must be used instead of SNR. The SNDR is defined as the ratio between the root-mean-square (rms) of the signal and the root-sum-square (rss) of harmonics components plus noise, but excluding the DC component. The SNDR is a good indication of the overall dynamic performance of an ADC because it includes all undesired components

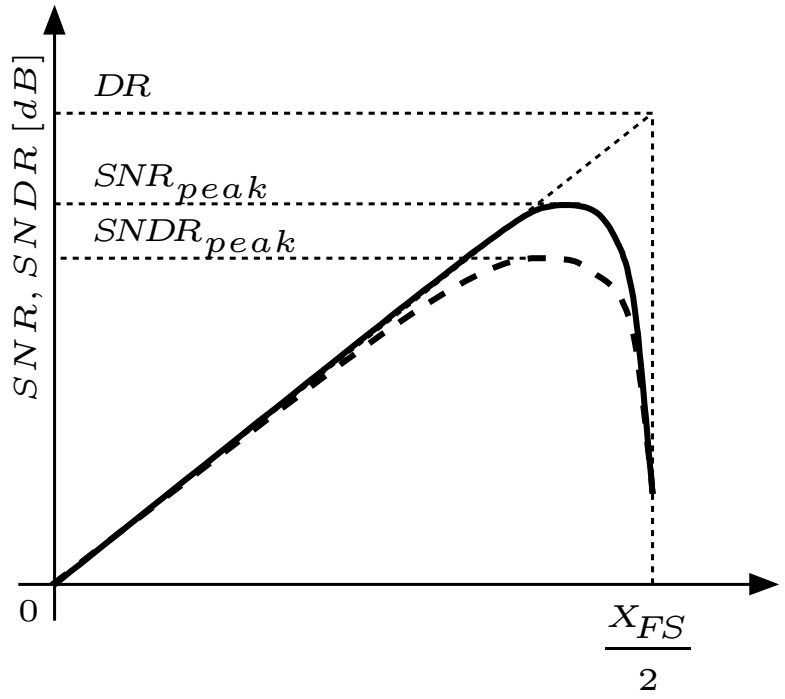


Figure 1.12: Basic performance metrics: SNR, SNDR and DR.

(i.e. noise and distortion). This parameter is often plotted for various input amplitudes and frequencies. It is usually given in dB.

- **DR**. Typically expressed in dB, is the value of the input signal at which the SNR is 0-dB. The DR specification is useful for ΣΔ architectures that do not obtain their maximum SNR or SNDR at full-scale input amplitude (0-dBFs).

- **Spurious-Free-Dynamic-Range (SFDR)**. Is the ratio between the rms of the signal and the rms of the highest spurious spectral component in the first Nyquist band. With large input signals the highest (or worst) component is given by one of the harmonics of the signal. Quoted in dB, the SFDR is an important specification in communications systems because it represents the smallest value of input signal that can be distinguished from a large interfering signal.

- **Total Harmonic Distortion (THD)**. Is the ratio between the power in all the harmonics components and the signal power. In oversampled systems only the harmonic power in the band of interest is included in the calculation. The THD value relates to the linearity of a converter, i.e. a lower THD value means less signal dependent distortion. The THD is often a function of the input signal amplitude. In ΣΔ converters large inputs typically cause circuits to saturate or clip and therefore generate distortion. Determining the THD accurately can be difficult when the harmonic distortion components are of the same order of magnitude as the random noise components. In order to get accurate results the technique of coherent averaging can be used. The result of this process is that random frequency components are suppressed while coherent (signal) components are not. It is worth to be noticed that every doubling of the number of averages reduces the random signals by 3-dB.

- **Effective Number of Bits (ENOB)**. This parameter measures the SNDR (or SINAD) using bits. An often used definition for ENOB, where the SNDR is expressed in dB, is:

$$ENOB = \frac{SNDR|_{dB} - 1.76}{6.02} \tag{1.12}$$

  The above equation is obtained from the theoretical SNR of an ideal N-bit ADC converter with a sine-wave excitation [3].

- **Sigma Delta FOM (ΣΔ FOM)**. This parameter establish the power effectiveness of the modulator. The ΣΔ FOM used in this thesis work is expressed in pico-Joules by conversion-level (pJ/conv-level) and is given by the following expression [8]:

$$FOM = \frac{P_w}{2^{\frac{DR-1.76}{6.02}} \cdot 2f_B} \cdot 10^{12}\,[pJ/conv] \tag{1.13}$$

  where P_w is the total power consumption of the modulator, f_B is the bandwidth of the input signal and DR is the dynamic-range of the ADC described before. The ΣΔ FOM is independent on the architecture of the modulator and on the

CMOS technology. Moreover, there are several definitions of the ΣΔ FOM, in some cases the SNR is used instead of DR.

1.3 Thesis Organization

This thesis work describes low-power single-loop ΣΔM addressing low power strategies. Before describing in detail the design, in order to determine the best ΣΔ topologies for the application, **Chapter 2** presents the specifications design of a third-order single-loop ΣΔM, suitable for sensor interface requirements. The specifications of the given application are also outlined.

Chapter 3 will focus on a new high-level behavioural model that take into account other second order effects, not covered by the sate-of-the-art model. A comparison of the results obtained with the new proposed model, implemented with Matlab/Simulink, and with transistor-level simulations confirm the effectiveness of the model.

In **Chapter 4** the first prototype of ΣΔ ADC designed in 90-nm CMOS technology will be described. Measurements results are discussed.

In **Chapter 5** a novel low power op-amp suitable for implementation in a ΣΔM is presented. A detailed small-signal analysis and design strategies are discussed. The op-amp is used in the second ΣΔ ADC prototype, realized in 90-nm CMOS technology. Measurements results are discussed.

In **Chapter 6** the main results achieved in this work are summarized.

Additional material is included in two appendices. **Appendix A** focuses with several recommendations for the design of multilayer boards used for testing data converters, thus the test board used for the measurement results reported in this thesis work is shown. **Appendix B** deals the design strategies and implementation of a decimation filter for a given ΣΔ converter.

Chapter 2

A Third-Order ΣΔ Modulator for Sensor Interface Applications

Scientists study the world as it is, engineers create the world that never has been.

– Theodore von Kármán

This Chapter presents the main requirements of a third-order ΣΔM to be used as sensor interface in a 250-Hz signal band. Among different ADC topologies, the ΣΔ ADC efficiently trades speed for accuracy, providing an effective way to implement high resolution ADCs without stringent matching requirement or calibration in a low-voltage environment. Meanwhile, the use of an intrinsically linear single-bit quantizer exempts the stringent matching requirement. For high resolution ADCs, the ΣΔ ADC is more power-effective and robust compared to other architectures.

2.1 Modulator Topology Selection

A single loop topology is preferable for low-voltage low-power designs since it is less sensitive to circuit non-idealities, where their impact on the performance of high resolution ADC become important, especially for harmonic distortion. The ΣΔ ADC is

known for its high tolerance for circuit non-idealities compared to other ADC architectures. However, in a low-voltage environment and nanometer technologies, circuit non-idealities become more severe and their impact on the ADC performance should be reconsidered. A third-order single-loop topology was chosen in this design, shown in Fig. 2.1. A Cascade of Integrators with Feed Forward (CIFF) topology, with a single-bit quantizer and DAC is used. Modulator loop coefficients were calculated by means of the Delta Sigma Toolbox [9] and reported in Tab. 2.1. Adjusting the dynamically scaled modulator coefficients to rational quantities, allows the designer to use the same capacitor unit element, leading to higher precision in the integrator gain and less capacitor mismatch. More importantly, this topology is quite tolerant to the inaccurate coefficients caused by capacitance mismatches.

Moreover, the choice of these modulator coefficients increase the overload level, which is good for expanding the input voltage range of the modulator in low-voltage environments. However, if the signal swing is not scaled down with the supply voltage the design of the op-amp input stage is critical. Furthermore, in presence of a

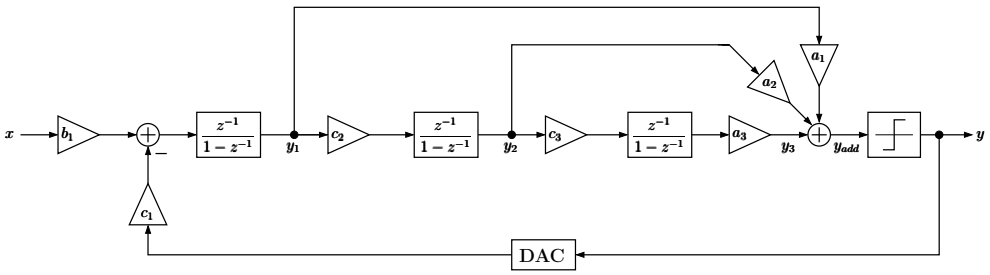


Figure 2.1: Third-order CIFF modulator architecture.

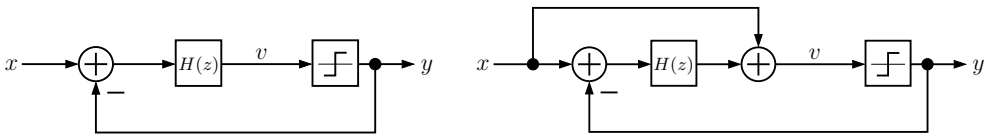
Table 2.1: Modulator Coefficients.

Stage	**Inter-stage coeff.**	**Feed-forward coeff.**	**Feed-in coeff.**
1^{st} Int.	$c_1 = 0.5$	$a_1 = 0.2$	$b_1 = 0.5$
2^{nd} Int.	$c_2 = 0.0625$	$a_2 = 0.2$	-
3^{rd} Int.	$c_3 = 0.021$	$a_3 = 0.3$	-

large output swing (compared to the supply), the op-amp output transistors exhibit a relevant variation of their source-drain conductance, thus affecting the voltage gain of the amplifier. This effect contributes to the overall harmonic distortion of the modulator. If the signal swing is scaled with the supply the linearity requirements on the op-amp are relaxed, but the modulator noise floor must be scaled down too, in order to maintain the modulator SNR unchanged. This design strategy must be discarded since it leads to a higher power consumption. The best solution in terms of linearity and power consumption trade-off is a relatively large input signal swing with a limited signal swing at the output of the integrators (i.e. CIFF architecture).

The input-feedforward path in CIFF architecture, illustrated in Fig. 2.2b, further relaxes the requirements on analog blocks. Note that the loop filter, $H(z)$, has to process the quantization noise only, compared to CIFF architecture without input-feedforward path, illustrated in Fig. 2.2a. On the other hand, without the input feedforward, the loop filter has to process the quantization noise in addition to the input signal. The removal of the input signal component reduces the swing at the internal nodes of the modulator which relaxes the headroom requirements, and allows for more efficient op-amp architectures to be used. However, the input-feedforward path needs the analog adder at the quantizer input [10], increasing area and power consumption. Moreover, with the input-feedforward path, the signal amplitude at the input of the quantizer increases, leading to more stability issues for an input signal close to the reference voltage. For this reason in this design the single loop architecture of Fig. 2.2a is preferred.

The specifications of the proposed modulator are shown in Tab. 2.2. A behavioural simulation with a −0.92-dBFs input signal is performed: the integrators output swing are shown in Fig. 2.3a and in Fig. 2.3b. The presented modulator is optimized to use the feature of low-voltage swing at the outputs of the integrators. As can be seen, the largest output swing is observed at the output of the first-integrator, but it is still within 30% about of the reference voltage, V_{REFP}. This allows the op-amp, which is the key component of the integrator, to have relaxed requirements in terms of output headroom and a Slew Rate (SR) in a context of low-power design, without increasing the harmonic distortion.



(a) (b)

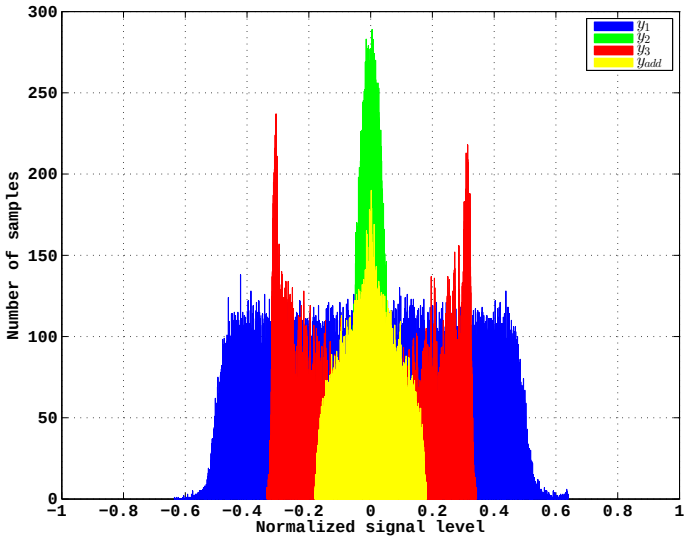
Figure 2.2: Single loop feedback architecture. (a) Single feedback topology. (b) Single feedback topology with a feedforward path.

Table 2.2: Specifications of the modulator.

Parameters	**Symbol**	**Value**	**Unit**
Sampling Frequency	f_{CK}	250	kHz
Signal Bandwidth	f_B	250	Hz
Oversampling Ratio	OSR	500	-
Common Mode Voltage	V_{CM}	0.5	V
Full Scale	FS	1	V
Power Supply	V_{DD}	1.2	V
High Reference Voltage	V_{REF_P}	1	V
Low Reference Voltage	V_{REF_N}	0	V
Effective Number of Bits	ENOB	16	bit

2.2 Noise Transfer Function with Mason's Rule

In a ΣΔM not only the quantization noise is present as noise source. Many noise sources and of different nature are present in every electronic circuit so different NTF, from each internal stage to the output, need to be obtained. The commonly used method to find the NTF is the Mason's rule [11]. The modulator of Fig. 2.4 is analyzed. The noise sources are highlights: n_1, n_2 and n_3 represent the noise introduced by the integrators stages, e stands for the quantization noise source while n_4



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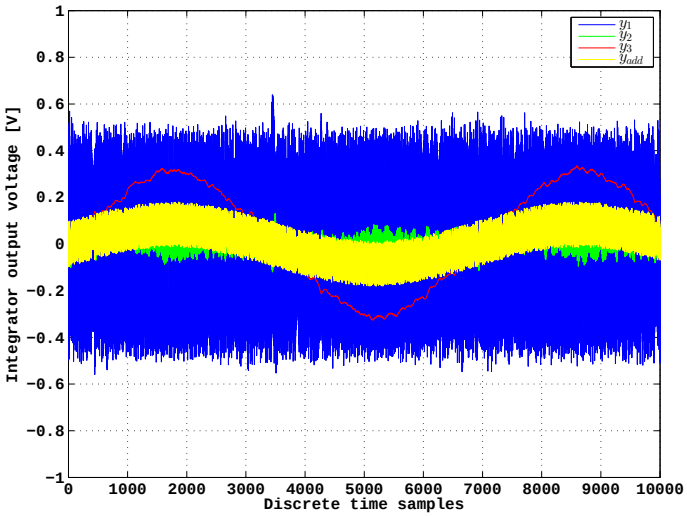


(b)

Figure 2.3: (a) Histogram of the integrator output swings. (b) Integrator output swings with a 35-Hz full-scale input signal.

represents the noise introduced by the references. Taking into account that $b_1 = c_1$, three loop transfer functions, from $n_{1\ldots3}$ to y, are obtained:

$$L_1(z) = \frac{-c_1 \cdot z^{-1}}{1-z^{-1}} \cdot \frac{c_2 \cdot z^{-1}}{1-z^{-1}} \cdot \frac{c_3 \cdot z^{-1}}{1-z^{-1}} \cdot a_3 = \frac{-a_3\, c_1\, c_2\, c_3 \cdot z^{-3}}{(1-z^{-1})^3} \tag{2.1}$$

$$L_2(z) = \frac{-c_1 \cdot z^{-1}}{1-z^{-1}} \cdot \frac{c_2 \cdot z^{-1}}{1-z^{-1}} \cdot a_2 = \frac{-a_2\, c_1\, c_2 \cdot z^{-2}}{(1-z^{-1})^2} \tag{2.2}$$

$$L_3(z) = \frac{-a_1\, c_1 \cdot z^{-1}}{1-z^{-1}} \tag{2.3}$$

The NTF of the quantization noise is obtained:

$$NTF_e(z) = \frac{y}{e} = \frac{1}{1 \underbrace{-L_1(z) - L_2(z) - L_3(z)}_{L(z)}} =$$

$$= \frac{(1-z^{-1})^3}{(1-z^{-1})^3 + a_3\, c_1\, c_2\, c_3 z^{-3} + (1-z^{-1})\, a_2\, c_1\, c_2\, z^{-2} + (1-z^{-1})^2\, a_1\, c_1\, z^{-1}} \tag{2.4}$$

Taking into account the high OSR of this design, in the frequency band of interest, f_B, the approximation $f \ll f_{CK}$ is still valid, and then:

$$z^{-1} = e^{-j2\pi f/f_{CK}} \xrightarrow[f \ll f_{CK}]{} \approx 1 \tag{2.5}$$

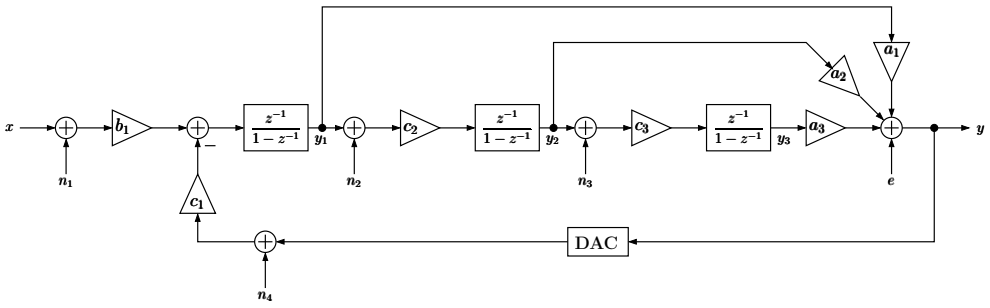


Figure 2.4: Third-order modulator. Noise sources are highlighted.

Thus, (2.4) in the signal bandwidth can be approximated as:

$$NTF_e(z) \simeq \frac{(1-z^{-1})^3}{a_3\, c_1\, c_2\, c_3\, z^{-3}} \tag{2.6}$$

For similar considerations, the NTFs from the three integrators inputs to the output result:

$$NTF_3(z) = \frac{y}{n_3} = \frac{c_3\, a_3 \cdot \dfrac{z^{-1}}{1-z^{-1}}}{1+L(z)} \simeq \frac{(1-z^{-1})^2}{c_1\, c_2} \tag{2.7}$$

$$NTF_2(z) = \frac{y}{n_2} = \frac{c_2\, c_3\, a_3 \cdot \dfrac{z^{-1}}{1-z^{-1}} \cdot \dfrac{z^{-1}}{1-z^{-1}} + c_2\, a_2 \cdot \dfrac{z^{-1}}{1-z^{-1}}}{1+L(z)} \simeq \frac{1-z^{-1}}{c_1} \tag{2.8}$$

$$NTF_1(z) = \frac{y}{n_1} = \frac{-L_1(z) - L_2(z) - L_3(z)}{1+L(z)} = \frac{L(z)}{1+L(z)} = \frac{v}{x} = STF(z) \tag{2.9}$$

Then more a node is internal at the feedback loop, higher is the order of its NTF. Thus its contribution to the overall noise is less significant. Then there are less stringent requirements for the integrators inside the loop in terms of noise performance and distortion compared with the performance of the first integrator which are dominant. The noise introduced by the references, $NTF_4(z)$, is equal to:

$$NTF_4(z) = \frac{v}{n_4} = \frac{L_1(z) + L_2(z) + L_3(z)}{1+L(z)} = \frac{-L(z)}{1+L(z)} = \frac{v}{x} = -NTF_1(z) \tag{2.10}$$

Thus $|NTF_4(z)| = |NTF_1(z)|$ and the noise shape effect is the same. However, as described in Section 2.4, this noise source is not subjected to folding and its overall impact is not so significant, as that of the first integrator, for the noise performance of the modulator.

2.3 Scaling of Integrators

One of the most interesting properties of the ΣΔM is the noise suppression inside the loop. Utilizing this feature a significant power saving can be obtained. For a single-loop ΣΔM, the noise suppression in node k can be calculated by [7]:

$$F_{sup,k} = \frac{OSR^{2k+1}}{\pi^{2k}}(2k+1)\prod_{i=1}^{k} c_i^2 \tag{2.11}$$

where F_{sup} is the noise suppression factor and c_i denotes the inter-stage coefficient, reported in Tab. 2.1, of the i-th stage. For the proposed topology, the noise suppression of the first, second and third stage is 70-dB, 116-dB and 162-dB respectively. This allows the sampling capacitors of these stages to be scaled down proportionally to corresponding ratios. This results into a reduction of the load capacitance of the op-amp, during the integration phase, and reduces the power consumption.

2.4 Noise Folding

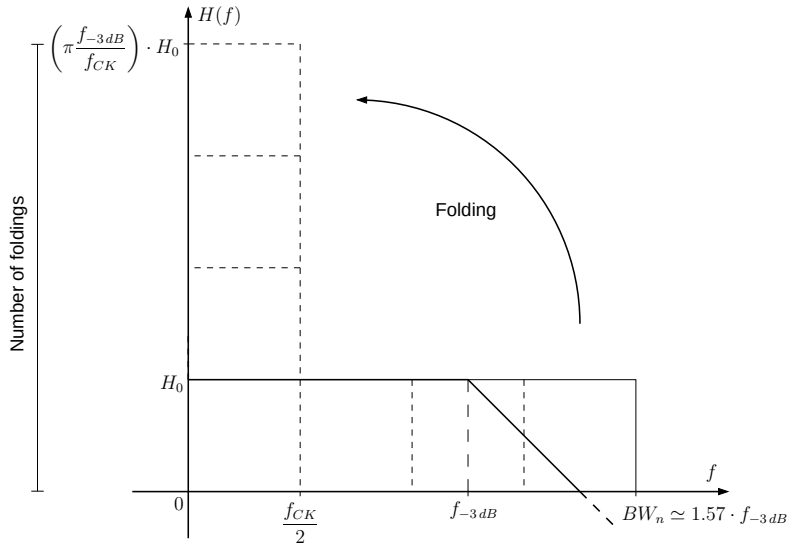


Figure 2.5: Equivalent noise bandwidth, BW_n, for single-pole approximation.

In every SC circuit, the wideband thermal noise (with time-varying and random nature), is subjected to sampling. This results into replicas of the original spectrum shifted by an integer of the sampling frequency, f_{CK}. The fold-over component can

easily be calculated if the circuit's broadband white noise is filtered by a low-pass filter with a transfer function $H(f)$, with a DC-gain H_0 and a one-pole approximation. The pole frequency typically corresponds to the amplifier gain-bandwidth product when the noise is sampled with an op-amp in unity-gain configuration. Also, during any sampling phase the thermal noise of switches is sampled on the sampling capacitor. This can be approximated as a one-pole system and is subjected to folding. Fig. 2.5 clearly shows the effect of oversampling the broadband white noise, considered as an ideally LP filtered white noise having a bandwidth equal to BW_n: the original noise power spectrum is shifted by multiples of the sampling frequency and summed. Applying the definition and recalling that the PSD of the white noise is constant over frequency, this results in a white noise PSD of value approximately equal $n \cdot H_0$, where n is the integer closest to the undersampling factor defined by $2 \cdot BW_n / f_{CK}$ [12].

For a first-order LP filtered white noise system BW_n is defined as [12]:

$$BW_n \equiv \int_{-\infty}^{+\infty} |H(f)|^2 df = \frac{\pi}{2} \cdot f_{-3dB} \tag{2.12}$$

where f_{-3dB} is the 3-dB noise bandwidth.

As shown in Section 2.2 the $|NTF|$ of the reference voltage and the first integrator are equal. The impact of their noise sources is equal, but the thermal noise introduced by the reference voltage is not subjected to sampling and thus its PSD is not multiplied by the folding number. Assuming the SC integrator, single-ended version, in Fig. 2.6. V_R is the reference voltage and implements the subtraction function in presence of feedback. This functions is implemented by the first integrator in the proposed ΣΔM. When the integrator works in sampling mode, $\phi_1 = 1$ and $\phi_2 = 0$, the input signal V_{in} is stored on C_s. During the integration phase, $\phi_1 = 0$ and $\phi_2 = 1$, the voltage noise of V_R is reported at the output of the integrator but not stored on C_s. Since in the next sampling phase the capacitor charge is updated to a new V_{in} value.

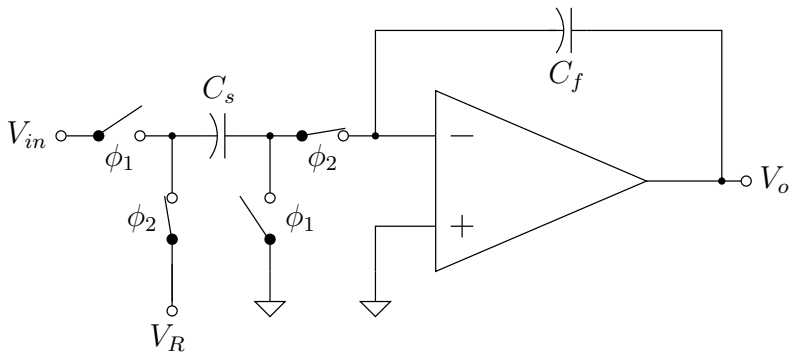


Figure 2.6: Basic SC integrator. The noise on the reference voltage, V_R, is not subjected to folding.

2.5 Noise Analysis in SC Integrator

2.5.1 Thermal Noise

Fig. 2.7 shows thermal noise contributions in a SC integrator. Assuming that the conducting switches in sampling and in integration have the same on state resistance, they have been replaced by their noise voltage sources and on-resistances [3]. Since two operating phases are present in a SC integrator, the analysis has to be divided in two parts. In sampling phase the op-amp is disconnected from the integrator's input and C_s. What remains is an RC circuit, Fig. 2.7b, with a time constant $\tau_1 = 2R_{on}C_s$. Therefore the well-known formula about thermal noise based on first order dynamic model (e.g. noise folding or bandwidth BW_n) can be used.

$$S_{sw}(f) = 4kT \cdot (2R_{on}) \tag{2.13}$$

where T is the absolute temperature and k is the Boltzmann constant. The Mean Square (MS) value of the sampled thermal noise voltage caused by switches results:

$$\overline{v_{n1,sw}^2} = 8kTR_{on} \cdot BW_n = \frac{8kTR_{on}}{4 \cdot \underbrace{(2R_{on}C_s)}_{\tau_1}} = \frac{kT}{C_s} \tag{2.14}$$

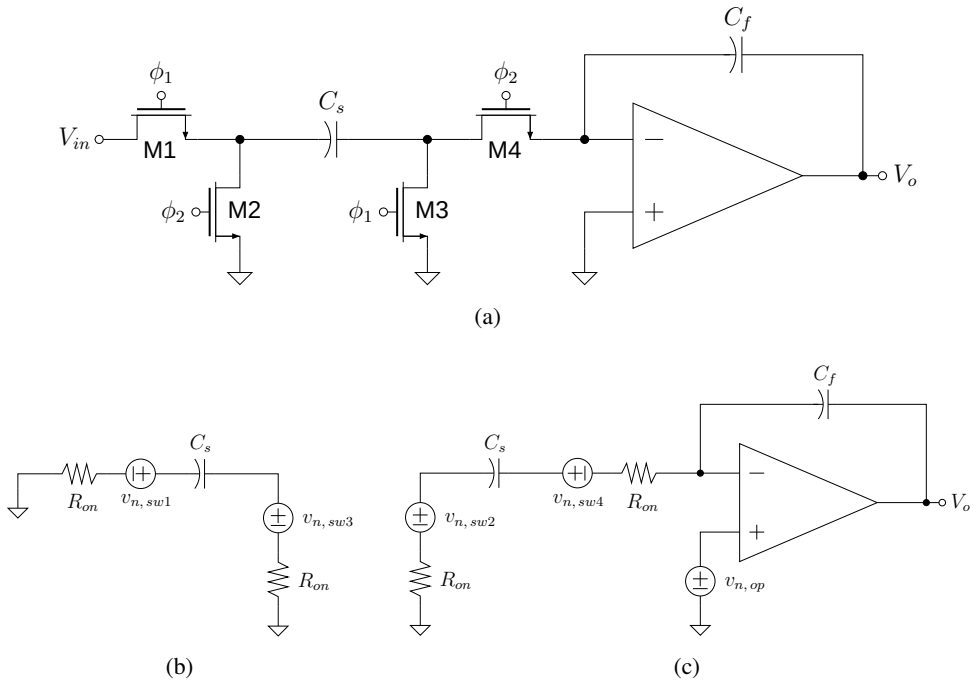


Figure 2.7: (a) SC integrator. (b) Noise sources in sampling phase (ϕ_2). (c) Noise sources in integration phase (ϕ_1).

During the integration phase, the equivalent circuit is more complex, Fig. 2.7c. Normally, the op-amp has many poles (and eventually zeros), indeed, so a first order model is not compatible. However, the $f_{-3dB,int}$ of the integration phase can be approximated as:

$$f_{-3dB,int} = \frac{f_t}{2} \cdot \tan(PM) \tag{2.15}$$

where f_t and PM are the unity-gain transition frequency and phase margin of the op-amp. Defining τ_2 as the time constant of the integration phase, the MS noise voltage $\overline{v_{n2,sw}^2}$ results:

$$\overline{v_{n2,sw}^2} = \frac{8kTR_{on}}{4\tau_2} = \overline{v_{n1,sw}^2} \cdot \frac{4\tau_1}{4\tau_2} = \overline{v_{n1,sw}^2} \cdot \frac{f_{-3dB,int}}{f_{-3dB,sam}} \tag{2.16}$$

where $f_{-3dB,sam}$ is the f_{-3dB} of the sampling phase. The total MS voltage of thermal

noise from switches results:

$$\overline{v_{n,sw}^2} = \overline{v_{n1,sw}^2} + \overline{v_{n2,sw}^2} = \frac{kT}{C_s} \cdot \left(1 + \frac{f_{-3dB,int}}{f_{-3dB,sam}}\right) \tag{2.17}$$

In integration phase there is also another important noise term, the input-referred op-amp's thermal noise, whose PSD is N_{op}.

$$\overline{v_{n,op}^2} = N_{op} \cdot \left(\frac{\pi}{2} \cdot f_{-3dB,int}\right) \tag{2.18}$$

Finally the total noise is the sum of this different noise sources:

$$\overline{v_{n,int}^2} = \overline{v_{n,sw}^2} + \overline{v_{n,op}^2} = \overline{v_{n1,sw}^2} + \overline{v_{n2,sw}^2} + \overline{v_{n,op}^2} \tag{2.19}$$

2.5.2 Flicker Noise

For a LP ΣΔM, to be interfaced to a low-frequency signal source (i.e. a sensor), the low-frequency noise such as flicker ($1/f$) and offset voltage from the first op-amp seriously degrades the SNR. Techniques such as Correlated Double Sampling (CDS) or Chopper Stabilization Technique (CHS) can be used to suppress the $1/f$ noise in the first-stage output signal.

Using CDS technique at the op-amp input, the input noise may be stored and then subtracted from the signal path. This introduces an HP filtering of the noise, and suppresses it effectively at frequencies which are much lower than the sampling frequency. CHS can be used to modulate the $1/f$ noise out of the signal band. CHS doesn't introduce aliasing of the broadband noise. Choosing the chopper frequency equal to the amplifier corner frequency, the white noise PSD increase of about 6-dB [12]. Due to the nonidealities of CHS modulation, as clock feed-through and charge injection, a residual DC offset appear at the modulator output. The harmonic distortion produced by CHS are related to the chopping frequency. Due to the significant spurious content, that would limits its use in high resolution applications, a notch filter is usually required to attenuate chopping noise, with an increase of complexity and area occupation [13]. To overcome this problem, related to harmonic distortion and residual DC offset, being mandatory requirements in sensor signal interface, CDS technique was adopted.

CDS technique is widely used in the SC circuits, but unlike CHS technique, CDS introduce aliasing of the broadband noise. A CDS based integrator, introduced by [14], is shown in Fig. 2.8. The op-amp low frequency input noise and offset is stored in the sampling phase, $\phi_1 = 1$ and $\phi_2 = 0$, on a dedicated capacitor, C_{CDS}, and then subtracted from the sampled input signal in the subsequent integration phase, $\phi_1 = 0$ and $\phi_2 = 1$. For minimum harmonic distortion in the output spectra the value of C_{CDS} capacitance must be set equal to C_s [15]. The detailed noise analysis of this circuit, is presented in Chapter 3.

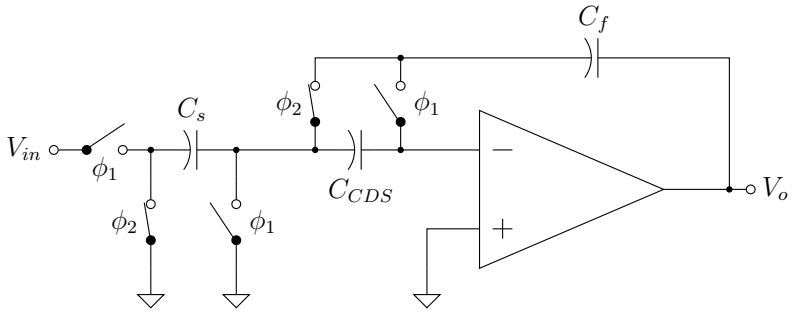


Figure 2.8: Switched-capacitor CDS integrator.

2.6 Noise Analysis in SC Adder

The CIFF topology requires an adder before the quantizer to perform the weighted feedforward summation, Fig. 2.1. In some implementations, this adder is done passively, Fig. 2.9a. This reduce the power dissipation compared to an active implementation, Fig. 2.9b, but could lead to an incomplete charge transfer and thus incomplete settling. The voltage noise of the analog adder, is typically referred at the output, $\overline{v_{n,add}^2}$. For the circuit of Fig. 2.9a, assuming for simplicity an equal bandwidth for the sum phase, $\phi_1 = 1$ and $\phi_2 = 0$, and for the reset phase, $\phi_1 = 0$ and $\phi_2 = 1$. The thermal noise is sampled in both phases on the input capacitors, $C_{s_{a1}}$ $C_{s_{a2}}$ and $C_{s_{a3}}$.

The output noise voltage is obtained:

$$\begin{aligned}\overline{v_{n,add}^2} &= 2\cdot\frac{kT}{C_{s_{a1}}}\cdot\left(\frac{C_{s_{a1}}}{C_{f_a}}\right)^2+2\cdot\frac{kT}{C_{s_{a2}}}\cdot\left(\frac{C_{s_{a2}}}{C_{f_a}}\right)^2+2\cdot\frac{kT}{C_{s_{a3}}}\cdot\left(\frac{C_{s_{a3}}}{C_{f_a}}\right)^2 \\ &= 2\cdot\frac{kT}{C_{f_a}}\cdot(a_1+a_2+a_3)\end{aligned} \tag{2.20}$$

where the factor 2 arises from the approximation of an equal bandwidth for the sum and reset phase.

For the circuit of Fig. 2.9b the contribution of the op-amp noise must also be included in the output noise voltage $\overline{v_{n,add}^2}$.

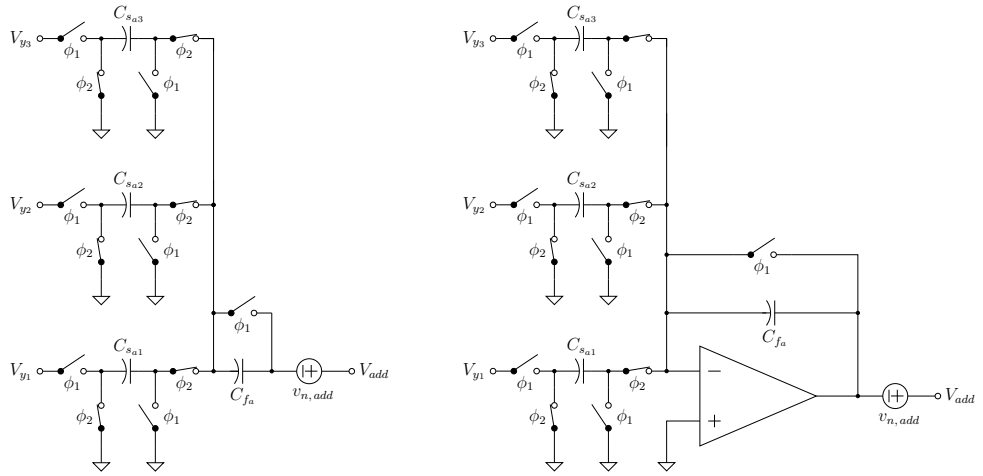


Figure 2.9: (a) Passive SC adder. (b) Active SC adder.

2.7 Noise Budget

The sampled thermal noise, defined as kT/C noise, is a major limitation of SC circuits, and must be taken into account in the design. This unavoidable limit is due to the sampling switch. Considering the noise voltage as $\sqrt{kT/C}$, sampling any signal

using a sampling capacitance of 1-pF leads to 64.5-μV noise voltage. If the sampling capacitance increases by α factor, the noise voltage is reduced by $\sqrt{\alpha}$. When designing a ΣΔM, it is important to find a good balance between the contributions of all noise sources. It means that all noise sources are scaled in a way that makes the circuit implementation affordable for the required application. A defined FS input, V_{FS}, and a given N-bit resolution establish the total noise power budget defined by [3]:

$$\overline{v_{n,budget}^2} = \frac{V_{FS}^2}{12 \cdot 2^{2 \cdot N}} \tag{2.21}$$

After having identified and quantified any thermal noise sources, the capacitors could be sized. Other noise sources, such as power supply noise and substrate noise,

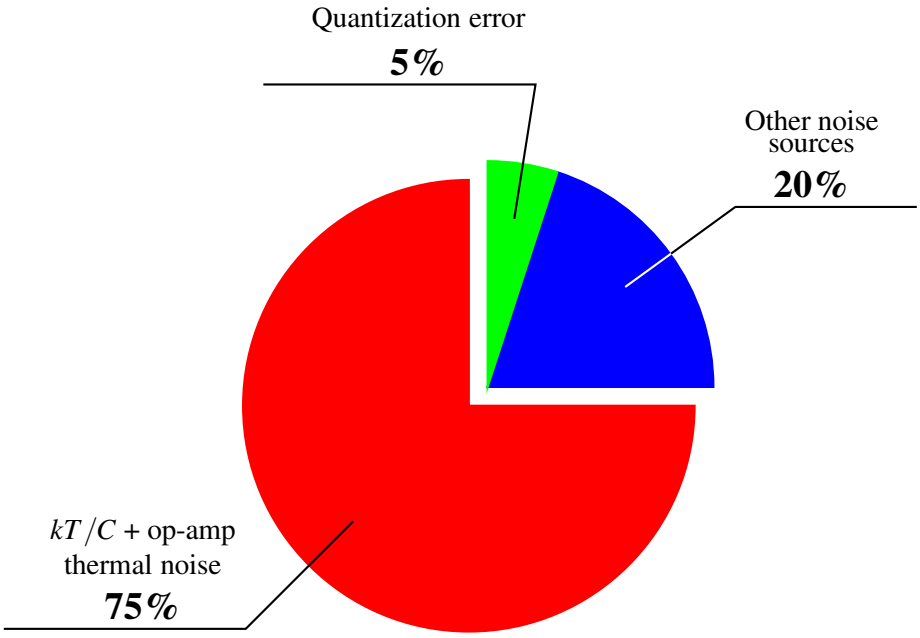


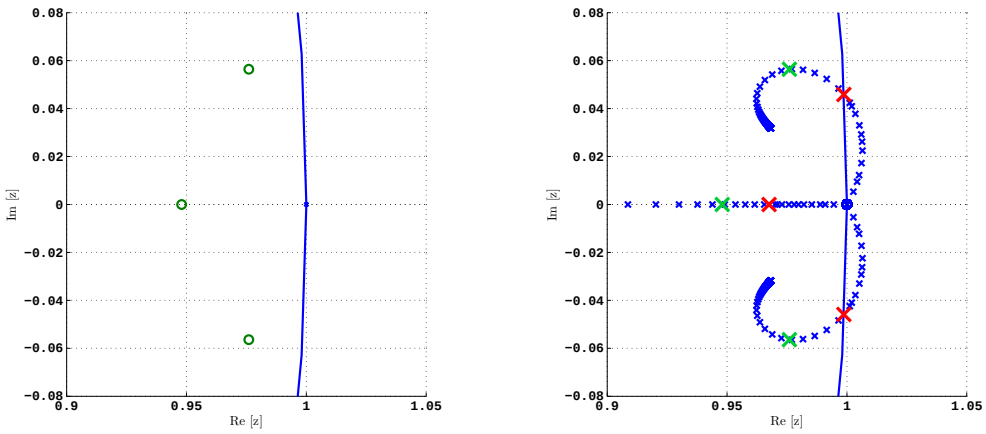
Figure 2.10: Noise budget.

are well suppressed by differential design and can be included in a noise margin estimations. A proposed noise budget from [3], sets the thermal noise power to the 75% of the whole degradation of SNR, the quantization noise power to the only 5%, and then a 20% margin for other noise sources, such as reference noise source. The noise floor is set by the power sums up from its three sources: quantization noise, thermal noise and a noise margin. An equivalent representation of the three noise sources is shown in Fig. 2.10.

2.8 Stability Analysis

The proposed third-order ΣΔM is simulated, at the behavioural level, by means of the Delta Sigma Toolbox [9]. The zeros and poles placement depends on the accuracy of the capacitor values implementing the coefficients of the modulator. Typical modern CMOS technologies ensure capacitors matching within $\pm 0.02\%$ [16].

The zeros of $H(z)$ are distributed on the circle centred at $z = 1$, Fig. 2.11a. The root locus of the characteristic equation, $1 + kH(z)$, of the Signal Transfer Function (STF), (1.9), can be plot for k changing from zero to infinity. The root locus originates on the poles ($k = 0$) and terminate on the zeros ($k = +\infty$) of $H(z)$. In general, for high-order ΣΔMs, their roots stay inside the unit circle only for certain ranges of k [3]. Fig. 2.11b shows the root locus of the proposed modulator, it crosses the unit circle when k approaches zero. The value of k is referred to as k_{max} when k approaches infinity and the root locus intersects the unit circle at the crosspoint. When $k_{min} < k < k_{max}$, roots lie inside the unit circle. With $k > k_{max}$, due to the relative large feedback magnitudes compared with the quantizer input, the modulator is stabilized. When the ΣΔM operates with a quantizer gain smaller than k_{min} over several consecutive clock cycles, the quantizer input tends to increases with no upper limit, and the modulator is driven into the overload instability region [17].



(a) (b)

Figure 2.11: (a) Zeros and poles locations of the open-loop transfer function $H(z)$. (b) Root locus of the characteristic equation, $1+kH(z)$.

Chapter 3

ΣΔ Modelling at Black-Box Level

Scientists dream about doing great things. Engineers do them.

– James Michener

The analysis of non-ideal effects in a SC ΣΔM allows us to derive accurate equivalent models for the op-amp ΣΔ building blocks. This Chapter shows how these effects influences the performance of the ΣΔM and are considered for improving the accuracy and computational efficiency of system-level simulations compared to transistor level simulations.

The op-amp is the most important component in a SC ΣΔ circuit. Op-amp performance greatly affect the SC ΣΔ linearity and noise thus is crucial at system level to be able to obtain the op-amp performance requirements. For this reason, a black-box model of the op-amp is useful for simulating the impact of op-amp performance on ΣΔM. An accurate ΣΔ model allows therefore to simulate the ΣΔ behaviour before the transistor level implementation of the op-amp. The achievement of a sufficiently high op-amp DC-gain for most SC applications is not a major design challenge, even for low voltage applications. On the other hand, the achievement of an optimized settling performance is a much more complex task. A new model is presented to aid the analysis of non-linear settling effects, such as the input transconductance variation of the op-amp input pair. The minimization of settling time by the correct balance of

capacitive loading and op-amp dimensioning is discussed. The modelling approach presented here is independent by the op-amp architecture resulting in tractable expressions for SC amplifier design at black-box level.

Starting from previous state-of-the-art model [18], [19], [20], [21], an improved new behavioural model of the SC integrator is proposed [22]. Collecting the error sources that induce harmonic distortion in SC circuits, the third and fifth harmonic of distortion, are in strictly good agreement with transistor-level simulation results. The model was validated in the design of a third-order ΣΔM in 65-nm STM technology. The simulated spectra of the modulator are in extremely good agreement with the results returned by transistor-level simulations, thus proving the effectiveness of the added features, being mandatory in a very low power design. The sources of harmonic distortion taken into account are:

1. discontinuous variation of integrator's node voltages at the switching transition, due to charge conservation principle, as discussed in Sec. 3.3;

2. transconductance variation during the charge-transfer transient, as discussed in Sec. 3.4;

3. finite gain and non-linear static I/O characteristic of the op-amp, as discussed in Sec. 3.5;

3.1 Design Process

The most common approach used for the systematic design of high-performance ΣΔM is based on the well-known top-down/bottom-up hierarchical synthesis methodology, conceptually illustrated in Fig. 3.1 [23]. In this approach, a given system is divided into several hierarchical levels so that at each abstraction level of the system hierarchy, a design (or sizing) process takes place, thus mapping the system specifications in a hierarchical way, from the top level to the bottom level. The reverse path in Fig. 3.1 corresponds to the hierarchical bottom-up verification process of the system performance.

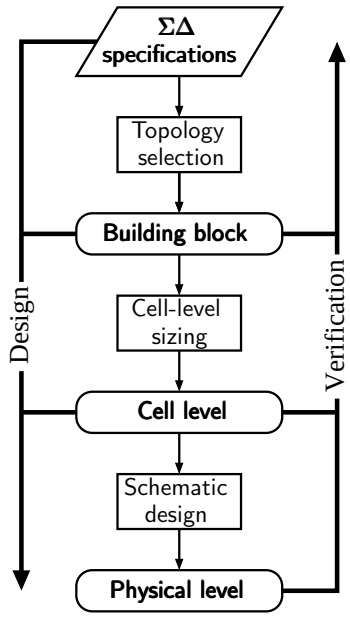


Figure 3.1: Hierarchical synthesis methodology commonly used in ΣΔM.

The design process of a ΣΔM starts from the system-level specifications, that is, the effective resolution, ENOB, and the signal bandwidth, f_B. The first goal is to find out the best modulator topology that fulfils these specifications. Usually, there are several topologies being a priori good candidates to fulfil a given set of modulator specifications. To this purpose initial ideal design equations of NTF, based on a linear model of the embedded quantizers described in Chapter 1, are used for calculating approximate values for the main parameters: OSR and the modulator order. Once these parameters are known, the architecture topology can be synthesized using more accurate non-linear model equations. To this purpose, Delta Sigma toolbox [9] is widely used.

The building block level consists in the high-level sizing of the op-amp, comparators, capacitors, switches. Cell level is the circuit topology of a given building block, and its design at transistor-level. This abstraction level, as physical level, covers from transistor-level schematics to the layout and chip implementation.

3.2 Op-amp Design Considerations

The op-amp in SC circuits, enables the active transport of signal charge from one capacitor to another without the charge leaking to parasitic capacitors. For the basic integrator of Fig. 3.2, the single-ended implementation is used here for simplicity, on clock cycle ϕ_2, the signal charge on C_s is transferred to C_f via the virtual ground node of the op-amp. Furthermore, the op-amp is configured as buffer so that the voltage across the capacitor can be measured without affecting the charge on that capacitor. Limitations in practical amplifier performance affect the accuracy of charge transfer from C_s to C_f on each clock period [24].

Considering the DT nature of a SC circuit, the signal at the output of the op-amp is only valid at each clock transition from integration to sampling phase and the following stage reads this input signal voltage. In this respect, the step response of the op-amp is of prime importance. The step response may exhibit a non-linear behaviour, the op-amp may slew or even have overshoot as long as the final value is approached within a specified error bound within one clock period. This feature alone makes SC circuits very attractive for inclusion with digital Very Large Scale Integration (VLSI) compared to their continuous-time counterparts [24].

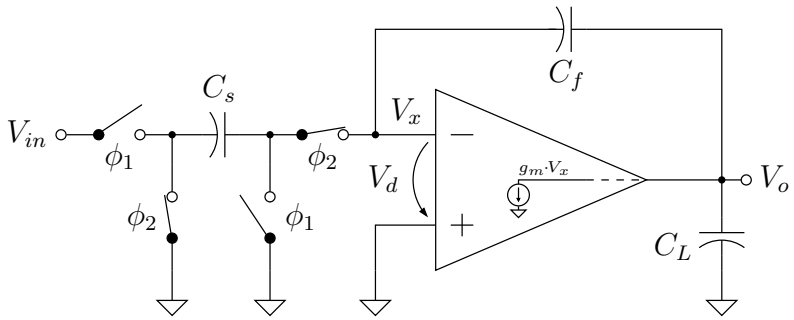


Figure 3.2: Basic integrator architecture. Single-ended version.

Applying Kirchhoff's Current Law (KCL), during the integration phase ϕ_2, at the inverting input and at the output of the op-amp in Fig. 3.2, two equations in the

Laplace domain are obtained:

$$\begin{cases} sC_s \cdot (v_x - v_{in}) + sC_f \cdot (v_x - v_o) = 0 \\ sC_L v_o + sC_f \cdot (v_o - v_x) + v_x g_m = 0 \end{cases}$$

The transfer function of the integrator can thus be obtained:

$$\frac{v_o}{v_{in}} = -\frac{C_s}{C_f} \cdot \frac{g_m\beta - s\beta C_f}{g_m\beta + s\left[C_L + C_f(1-\beta)\right]} \tag{3.1}$$

where $\beta = \dfrac{C_f}{C_s + C_f}$ is the feedback factor and g_m is the transconductance of the op-amp. Transfer function in (3.1) exhibits a Left Half Plane (LHP) pole:

$$p = -\frac{g_m \cdot \beta}{C_L + C_f \cdot (1-\beta)} = -\frac{g_m}{C_s + C_L \cdot \left(1 + \dfrac{C_s}{C_f}\right)} = -\frac{1}{\tau} \tag{3.2}$$

C_L models the capacitive load of the integrator and is the sum of parasitics capacitance and the input (sampling) capacitor of next stage of integration. It should be noted that the higher C_L the higher τ (i.e, the time constant involved in the transient response). In addition, a zero Right Half Plane (RHP) is present in the transfer function:

$$z = -\frac{g_m}{C_f} \tag{3.3}$$

3.3 Transient Behaviour in SC Integrator

Considering the general single-ended integrator in Fig. 3.3, V_R implements the function of the feedback signal provided by the DAC. In this proposed $\Sigma\Delta$ V_R input is used for implementing the subtraction function: in presence of feedback in the SC integrator, the value of V_R can be either V_{REF_N} or V_{REF_P} (0-V or 1-V, in the present design). The sampling mode occurs with $\phi_1 = 1$ and $\phi_2 = 0$ and the integration mode with $\phi_1 = 1$ and $\phi_2 = 0$. Assuming 50% duty-cycle for the clock signal and taking Fig. 3.4 as reference, the sampling instant in the $(n-1)$-th period is $t_0 = (n-1/2)T_{CK}$. Some charge transfer takes place just after the switching from sampling to integration, occurring at $t = t_0$, and before the op-amp starts the SR limiting phase [25]. Such voltage step has a relevant impact on the time length of the SR limiting regime. Due to

this effect the voltage, at nodes V_x and V_o, is discontinuous and jumps at $t = t_0^+$ to the opposite direction with respect to the settling values, as shown in Fig. 3.4. The magnitude of this step depends on the capacitor values (C_s, C_f and C_L) and on the sampled input voltage, $V_{in}(n-1)$. Computing exactly $V_o(t_0^+)$ and $V_x(t_0^+)$ is mandatory for accurately estimating the length of the slew-limited region and thus the final settling error.

In the sampling phase, where the sampling capacitor C_s store the input signal, the op-amp is not involved and the error is related to the two sampling switches due to the settling of the RC circuit. This error can be easily evaluated and embedded in the behavioural model. The result of the integration of the input voltage at the n-th clock period is the op-amp output voltage at the end of the integration phase. i.e at $t = nT_{CK}$. In this latter phase both op-amp and charge injection from switches add error to the output voltage. Charge injection is not considered in the behavioural modelling since it is usually minimized by means of circuit techniques involving dummy switches and bottom-plate sampling combined with a differential implementation of the integrator in Fig. 3.3. Regarding the errors caused by the op-amp it is useful to consider the output voltage signal, V_o, in integration phase, Fig. 3.4a. Three different sub-phases are evident: discontinuous variation ($t = t_0$), slew-limiting region ($t_0 < t < t_1$) and linear response region ($t_1 \leq t < nT_{CK}$).

It is worth to be noticed that the slew-limiting sub-phase is skipped if the differ-

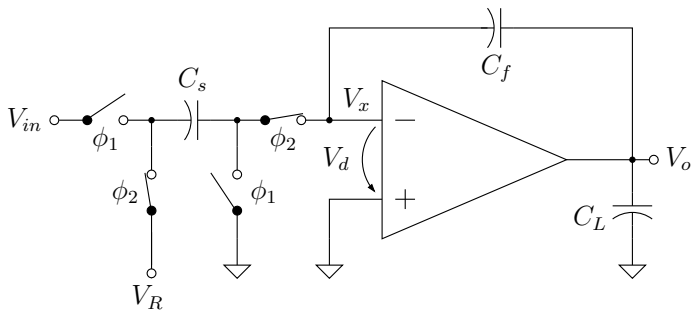
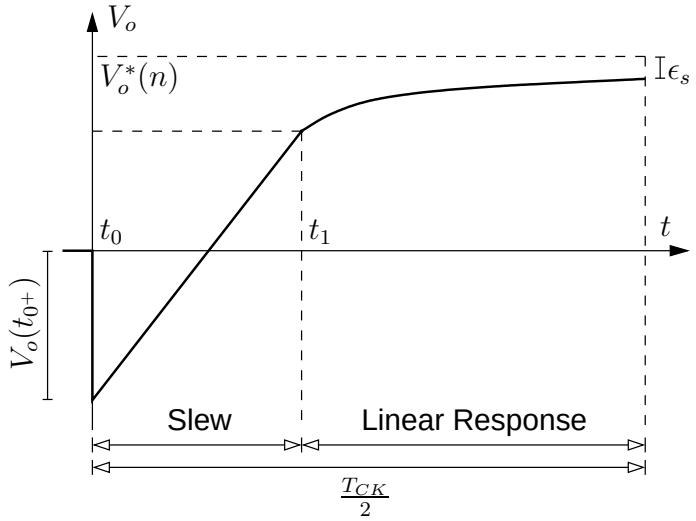
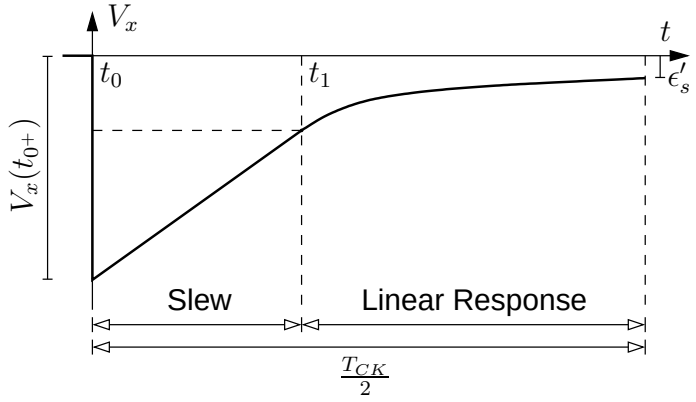


Figure 3.3: SC integrator (single-ended version). V_R stands for the feedback reference voltage.



(a)



(b)

Figure 3.4: Example of V_o and V_x transient in ϕ_2 (integration) phase. ε_s and ε_s' are the settling errors with respect to asymptotic values (i.e. $V_o^*(n)$ and 0 for V_o and V_x respectively).

ential input voltage at the beginning of the integration phase is within the linear range of the op-amp. The error accumulated during the slew-limiting phase has a primary impact on the overall integration error and increases the harmonic distortion of the

output spectrum with a sine-wave at the modulator input. In a design without a stringent power consumption limitation, a good margin can be achieved on the minimum SR value, the effect of the slew-limiting phase in the overall error is less important because the op-amp's SR can be sized to a reasonable high value. On the contrary, in a power constrained design, where the battery life time is of primary importance, both the maximum SR and the open-loop bandwidth of the op-amp must be minimized. Therefore the settling error (due to both sub-phases) is not negligible and must be accurately estimated by means of a behavioural model. This is mandatory to achieve the minimum specifications for the op-amp (in terms of SR and bandwidth) compatible with the resolution of the converter, but without resorting to time expensive transistor level simulations.

It is worth to be noticed that an accurate high-level behavioural model allows the designer to identify the best time partitioning between slew-limiting phase and linear response on the basis of the op-amp architecture that has to be evaluated for this design. Indeed if an op-amp with adaptive biasing or with a class-AB output stage is used, a lowest power consumption may be obtained by shrinking both the slew-limited phase and the op-amp bandwidth. An accurate estimation of the final settling error requires: an accurate estimation of t_1 and an accurate op-amp linear model.

3.3.1 Integration Phase: Initial Conditions

At the beginning of the integration phase for the circuit of Fig. 3.3, $t = t_{0^+}$ in Fig. 3.4, the charge conservation must be considered for both the negative input and output terminals of the op-amp. Since the op-amp output impedance at $t = t_{0^+}$ is high and thus no charge is transferred to the capacitors:

$$\Delta q_L = -\Delta q_f \tag{3.4}$$

$$\Delta q_s = -\Delta q_f \tag{3.5}$$

Solving (3.4) and (3.5), $V_o(t_{0^+})$ and $V_x(t_{0^+})$ are obtained:

$$V_o(t_{0^+}) = V_o(n-1) + \frac{C_f}{C_f + C_L} V_x(t_{0^+}) \tag{3.6}$$

$$V_x(t_{0^+}) = \beta \cdot [V_o(t_{0^+}) - V_o(n-1)] - \frac{C_s}{C_f + C_s} \cdot [V_{in}(n-1/2) - V_R] \tag{3.7}$$

where $V(n-1) = V[T_{CK}]$ notation, correspond to $z^{-1}V[z]$ in DT domain. Solving the charge conservation equations, (3.6) and (3.7), the values of V_o and V_x at $t = t_{0^+}$ are found:

$$V_o(t_{0^+}) = V_o(n-1) - \widetilde{V}_{in}(n-1/2) \cdot \frac{C_s}{C_s + C_L/\beta} \tag{3.8}$$

$$V_x(t_{0^+}) = -\frac{C_s}{C_s + C_L/\beta} \cdot \left(1 + \frac{C_L}{C_f}\right) \cdot \widetilde{V}_{in}(n-1/2) \tag{3.9}$$

where $\widetilde{V}_{in}(n-1/2) \equiv [V_{in}(n-1/2) - V_R]$. The contribution of the output capacitive load, C_L, due to sampling capacitance of the next stage and the op-amp parasitic output capacitance, in (3.8) and in (3.9) is relevant. It is worth to be noticed that in a power constrained design, the sampling capacitor of the second integrator is often set to the minimum value, since its impact on the converter noise floor is negligible. The problem is exacerbated in deep sub-μm designs since the parasitic capacitance at the op-amp output node scales down with the technology.

3.3.2 Op-amp Linear Range

Depending on the initial differential voltage $V_x(t_0^+)$, calculated in Sec. 3.3.1, and on the op-amp input linear range, during the integration phase the integrator exhibit either a full-linear or a combined slew-limited and linear step response. For the calculation of the length of the slew-limited phase, $t_1 - t_0$ in Fig. 3.4, the estimation of the op-amp linear range is mandatory. Indeed, the switching instant between the slew-limited and the linear regime, t_1, occurs when the differential input voltage, V_d for the op-amp in Fig. 3.3, enters in the linear range.

$$|V_d| \leq V_{LR} \tag{3.10}$$

The value of V_{LR}, i.e. the bound of the linear range, is determined by the input stage of the op-amp which is usually based on a differential pair (either NMOS or PMOS). Taking the basic fully-differential op-amp of Fig. 3.5 as reference, the output current of the differential pair, MP1 and MP2, is defined as the difference of the drain current

of the devices in the pair, $I_{diff} = I_{d_1} - I_{d_2}$. This current exhibits an almost parabolic dependence on the differential input voltage, V_d, provided that the MOS devices operate in strong-inversion region. The upper bound of the input linear range can be expressed in terms of the g_m/I_d value of the input devices, at $V_d = 0$:

$$V_{LR} = \sqrt{2} \cdot \left(\frac{g_{m0}}{I_{d0}} \right)^{-1} \tag{3.11}$$

where I_{d0} and g_{m0} are, respectively the drain current and the small-signal transconductance of the input transistor at $V_d = 0$. It should be remarked that g_m/I_d depends on the inversion-factor of the device, IF, and on the thermal voltage, v_{th}, while it is almost insensitive to the technological parameters:

$$\frac{g_m}{I_d} = \frac{1}{n \cdot v_{th}} \cdot \frac{1}{0.5 + \sqrt{0.25 + IF}} \tag{3.12}$$

where n is the slope factor.

In a power constrained design, the input devices are usually biased in weak-inversion region, leading to a hyperbolic tangent dependence on V_d:

$$I_{diff} = I_H \cdot \tanh \left(\frac{V_d}{2} \cdot \frac{g_{m0}}{I_{d0}} \right) \tag{3.13}$$

where I_H is the bias current of the differential pair, Fig. 3.5. It has to be noticed that in weak-inversion region the output current of the differential pair does not saturate at a finite V_d value. However a good approximation of the input linear range is obtained at $I_{diff} \approx 0.99 \cdot I_H$, thus:

$$V_{LR} \approx 5 \cdot \left(\frac{g_{m0}}{I_{d0}} \right)^{-1} \tag{3.14}$$

3.3.3 Op-amp Slew-Limiting Range

The op-amp of Fig. 3.3 enters in the slew-limited regime at $t = t_0^+$ if:

$$|V_x(t_0^+)| > V_{LR} \tag{3.15}$$

In this case the integrator output and input voltages approximately exhibit a linear step response behaviour:

$$V_o(t) = V_o(t_0^+) + sgn(V_o^*)\,SR \cdot t \tag{3.16}$$

$$V_x(t) = V_x(t_0^+) + sgn(V_o^*)\,\beta \cdot SR \cdot t \tag{3.17}$$

where SR is the op-amp maximum slew-rate and V_o^* is the (ideal) asymptotic value of the output voltage occurring with an unlimited op-amp voltage gain:

$$V_o^* = V_o(n-1) + \frac{C_s}{C_f} \cdot V_{in}(n-1/2) \tag{3.18}$$

The former and the latter terms in (3.18) are due to the charge stored on the feedback capacitor, C_f, at $t = t_{0^-}$ and to the charge transfer from C_s to C_f, respectively. The value of t_1, i.e. the instant when the op-amp toggles from slew-limited to linear settling behaviour, is estimated from the upper bound of the linear range and SR from (3.17):

$$t_1 = t_0 + \frac{|V_{LR} - V_x(t_{0^+})|}{\beta \cdot SR} \tag{3.19}$$

If $(t_1 - t_0) \geq T_{CK}/2$ the integration phase ends with the op-amp still operating in the slew-limited mode. This is not the case in medium-to-high resolution modulators where the constraints on the residual error requires that the op-amp enters in the linear-settling mode within the integration phase. Therefore, an accurate equation for $V_o(t)$ is required for $t \in [t_1, n \cdot T_{CK}]$.

3.3.4 Op-amp Two Poles Approximation: Second Order Model

In a low-power op-amp, the contribution of the second pole cannot be neglected since it is usually close to the op-amp unity gain angular transition frequency, and its effect must be taken into account [26]. In a low-power design a simple model based on a first-order op-amp transfer function, as in [25], cannot be used for accuracy reasons. Indeed, the contribution of higher-frequency poles and zeros cannot be neglected since they are usually close to the unity gain frequency due to low-power design constraints. Their effect can be taken into account by introducing an equivalent second

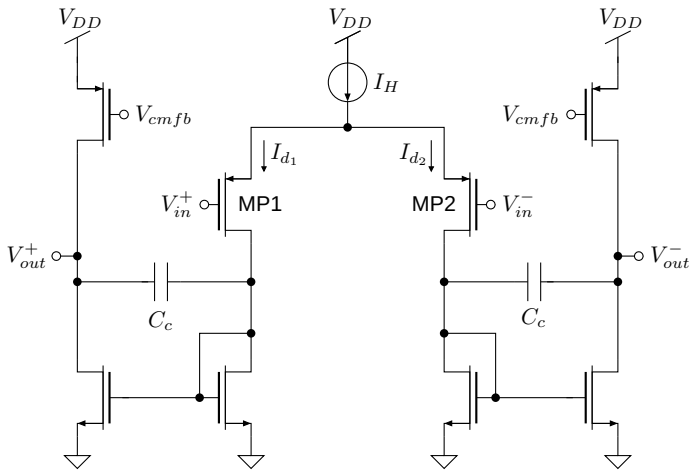


Figure 3.5: Simplified fully-differential op-amp. Miller compensated schematic.

pole, ω_{p2}, [26]. Considering an input frequency well above the first pole (i.e. ω_{p1}), the open loop, $A(s)$, and closed loop, $A_{CL}(s)$, transfer functions can be approximated as:

$$A(s) \simeq \frac{A_0 \cdot \omega_{p1}}{s \cdot \left(1 + \dfrac{s}{\omega_{p2}}\right)} \tag{3.20}$$

$$\begin{aligned} A_{CL}(s) = \frac{A(s)}{1+\beta \cdot A(s)} = \frac{1}{\beta} \cdot \frac{\overbrace{\beta\,\omega_{ta}\,\omega_{p2}}^{\omega_o^2}}{s^2 + \underbrace{\omega_{p2}}_{2\xi\,\omega_o} \cdot s + \underbrace{\beta\,\omega_{ta}\,\omega_{p2}}_{\omega_o^2}} = \\ = \frac{1}{\beta} \cdot \frac{\omega_o^2}{\left(s + \xi\,\omega_o - j\omega_o\sqrt{1-\xi^2}\right) \cdot \left(s + \xi\,\omega_o + j\omega_o\sqrt{1-\xi^2}\right)} \end{aligned} \tag{3.21}$$

where A_0 is the op-amp's DC-gain and ω_{ta} is the open loop angular transition frequency for $A(\omega)$. The transfer function from the input to the negative op-amp input, V_{in} and V_x for the circuit of Fig. 3.3, in the integration phase is thus obtained from

(3.21) and the feedback factor:

$$A_x(s) = \frac{v_x}{v_{in}} = \beta \cdot A_{CL}(s) \tag{3.22}$$

The natural angular frequency, ω_o, and the damping ratio, ξ, of $A_x(s)$ are therefore:

$$\omega_o \equiv \sqrt{\beta\, \omega_{ta}\, \omega_{p2}} \tag{3.23}$$

$$\xi \equiv \frac{\omega_{p2}}{2\omega_o} \tag{3.24}$$

The frequency of the equivalent second pole can be expressed as a function of the Phase Margin (PM) of the integrator in integration configuration [26]:

$$\omega_{p2} = \omega_t \cdot \tan(PM) \tag{3.25}$$

where ω_t is the unity-gain transition angular frequency of the loop gain, i.e. $\beta \cdot A(j\omega)$.

The voltage at the negative op-amp input, $V_x(t)$, in the linear settling sub-phase is thus obtained as the step response of a system with the transfer function in (3.22) from $t = t_1$:

$$\begin{aligned} V_x(t) &= V_x^{\infty} + [V_x(t_1) - V_x^{\infty}] \\ &\cdot e^{-\xi\omega_o(t-t_1)} \cdot \frac{\sin\left[\omega_o(t-t_1)\sqrt{1-\xi^2} + \phi\right]}{\sqrt{1-\xi^2}} \end{aligned} \tag{3.26}$$

where:

$$V_x^{\infty} \equiv lim_{t\to\infty} V_x(t) \tag{3.27}$$

$$\phi \equiv \arcsin\left(\sqrt{1-\xi^2}/\xi\right) \tag{3.28}$$

If the sinusoidal term is neglected in the previous equation and only the exponential envelope is considered, the following approximate expression is found for $V_x(t)$:

$$V_x(t) \approx V_x^{\infty} + [V_x(t_1) - V_x^{\infty}] \cdot e^{(t/\tau_{int})} \tag{3.29}$$

where, from (3.25):

$$\tau_{int} \equiv \xi\,\omega_o = \frac{2}{\omega_t \cdot \tan(PM)} \tag{3.30}$$

The output voltage is obtained from (3.29) and considering the feedback factor:

$$V_o(t) = \frac{V_x(t)}{\beta} + V_o^* \tag{3.31}$$

where the former term is the residual feedback error due to the limited op-amp voltage gain. Furthermore, the value of V_o in (3.31) must be upper and lower bounded by the maximum, $V_{o_{MAX}}$, and minimum, $V_{o_{MIN}}$, op-amp output voltage.
The asymptotic value of $V_x(t)$, V_x^∞, can be estimated at two different accuracy levels:

$$V_x^\infty \approx -\frac{V_o^*}{A_0} \tag{3.32}$$

$$V_x^\infty = -F_{oa}^{-1}(V_o^*) \tag{3.33}$$

where:

$$V_o = F_{oa}(V_d) \tag{3.34}$$

is the non-linear static I/O characteristic of the op-amp. With the approximation in (3.32) a constant voltage gain, A_0, is assumed over all the op-amp linear range and the small-signal DC-gain is required as the only op-amp parameter. In (3.33) a higher level of accuracy is obtained, but the I/O characteristic is required. This issue is discussed in Sec. 3.5.

It is worth to be noticed that (3.31), requires only five op-amp parameters if V_x^∞ is estimated with the lower accuracy level: A_0, ω_t, PM, V_{LR} and SR. Such parameters are easily obtained by short transistor-level simulations performed on the stand-alone op-amp and on the integrator in the integration configuration. In spite of the approximation of neglecting the sinusoidal term, (3.29) exhibits a higher accuracy with respect to simple single-pole approximation for $A(s)$. Indeed the time constant in the exponential term in (3.29) takes into account the effect of further poles and zeros in the open-loop op-amp transfer function through its PM. Furthermore, it is worth to be noticed that the equivalent integrator time constant, τ_{int}, can be used also in the noise model of the same circuit, as discussed in Sec. 3.6, thus improving the accuracy of the behavioural simulation of the modulator noise floor.

We can thus conclude that the proposed model exhibits the following improvements with respect to the analysis reported in [25]:

- a higher accuracy is obtained with the second-order transfer function, where the effect of further poles and zeros is modelled with an equivalent second-pole. The angular frequency of this pole is easily obtained from the PM of the circuit in the integration phase.

- the model is independent from the op-amp architecture and only five op-amp parameters are required (three of them obtained with a small-signal AC simulation, one with a DC-sweep simulation and one with a short transient simulation).

3.4 Transconductance Variation

The input differential pair, MP1 and MP2, of the basic fully differential op-amp in Fig. 3.2, exhibits a transconductance which depends on the input differential voltage, $V_d(t)$. The impact of transconductance, g_m, variation on the charge transfer error in SC amplifiers and filters has been already reported [27], [25]. The variation of g_m during the linear settling sub-phase is reflected on the ω_t parameter, obtained from the linearization of the op-amp circuit at a specific time instant t_k, with $t_k \in [t_1, nT_{CK}]$. Since the time constant in (3.29) depends on ω_t as shown in (3.30), it should be evaluated at each time point, t_k. In order to achieve an accurate estimation of the harmonic distortion introduced by the ΣΔM, such variation of $\tau_{int}(t_k)$ in the linear-settling sub-phase must be taken into account in the behavioural model. To this aim, the time interval where the op-amp works in linear settling mode must be divided in several time steps $(t_{k+1} - t_k)$ and an iterative algorithm has to update the value of $\tau_{int}(t_k)$ according to:

$$\tau_{int}(t_k) = \frac{\tau_{int_0}}{\eta(t_k)} \tag{3.35}$$

where τ_{int_0} is the time constant calculated with (3.30) in $V_d = 0$ bias point. An equation for η based on hypothesis of strong-inversion bias for the input pair transistor is reported in [27].

$$\eta(t_k) = \sqrt{1 - \alpha V_x^2(t_k)} - \frac{\alpha V_x^2(t_k)}{\sqrt{1 - \alpha V_x^2(t_k)}} \tag{3.36}$$

where:

$$\alpha = \frac{\mu c_{ox} \cdot (W/L)}{4 I_H} \tag{3.37}$$

I_H is the bias current of op-amp's source-coupled input pair, Fig. 3.5, μ is the carrier electrical mobility, c_{ox} is the gate oxide capacitance per unit area, and W/L is the aspect ratio of MP1 and MP2. α parameter can only be indirectly estimated by means of a DC circuit simulation of the op-amp since the knowledge of technology parameter is necessary and the hypothesis of strong-inversion biasing of the input pair transistor is no more valid in a power limited design. For this reason, in a design perspective, it is worth rewriting (3.36) in terms of a small-signal quantity ready to simulate: the g_m/I_d ratio. Making this choice, (3.36) can be rewritten:

$$\eta = \sqrt{1 - \left(\frac{V_x(t_k)}{4} \cdot \frac{g_{m_0}}{I_{d_0}} \right)^2} - \frac{\left(\frac{V_x(t_k)}{4} \cdot \frac{g_{m_0}}{I_{d_0}} \right)^2}{\sqrt{1 - \left(\frac{V_x(t_k)}{4} \cdot \frac{g_{m_0}}{I_{d_0}} \right)^2}} \tag{3.38}$$

In a low-power design, sub-threshold or weak-inversion biasing conditions for the source-coupled input pair must be considered. In this case the transconductance, g_m, becomes:

$$g_m(t_k) = g_{m_0} \cdot \left[1 - \tanh^2 \left(\frac{V_x(t_k)}{2} \cdot \frac{g_{m_0}}{I_{d_0}} \right) \right] \tag{3.39}$$

The equation of $\eta(t_k)$ in weak-inversion region is therefore:

$$\eta(t_k) = 1 - \tanh^2 \left(\frac{V_x(t_k)}{2} \cdot \frac{g_{m_0}}{I_{d_0}} \right) \tag{3.40}$$

Whatever is the bias of the input pair, only one parameter (g_{m_0}/I_{d_0}) must be obtained by a fast transistor-level simulation to find both V_{LR} and $\eta(t_k)$. In strong-inversion condition (3.11) and (3.38) must be used, while with a weak-inversion bias (3.14) and (3.40) are selected. The accuracy of the behavioural simulation of $V_o(t)$ depends on the width of the time step, $t_k - t_{k-1}$, where the value of τ_{int} is updated. A convenient trade-off between accuracy and the time consumed for the behavioural simulation is found by repeating a first trial simulation with a progressively shirked time step. This iteration is stopped when the change of the simulated total harmonic distortion of the ΣΔM is below the target resolution.

3.5 Static op-amp Characteristic

A hyperbolic tangent function can approximate the I/O static characteristic of the op-amp with reasonable accuracy, hence allowing variation of gain and consequent non-linearity in behavioural simulations. Any op-amp has its own DC characteristic, this is the reason why other authors use polynomial interpolation with more complicated optimization algorithms such as least squares regression [28]. Unfortunately, those methods are not very useful for preliminary design steps due to the lack of data. As discussed in Sec. 3.3.4 the knowledge of the op-amp static characteristic, i.e. $V_o = F_{oa}(V_d)$, allows to improve the accuracy of the equation modelling the integrator output voltage in the linear settling phase. If the input devices of the op-amp are biased in weak-inversion mode, the I/O characteristic is accurately modelled with a hyperbolic tangent function. However, as suggested in [29], this approach can be extended, with a reasonable accuracy, to the case of input devices biased in strong-inversion mode. Since the target is a design-oriented model, the hyperbolic approximation is implemented, which requires the values of only two op-amp parameters: the small-signal gain at $V_d = 0$, A_0, and the output voltage swing, $V_{o_{MAX}} - V_{o_{MIN}}$:

$$V_o(t_k) = a \cdot \tanh\left(b \cdot V_d(t_k)\right) \tag{3.41}$$

where:

$$a = \frac{V_{o_{MAX}} - V_{o_{MIN}}}{2} \tag{3.42}$$

$$b = \frac{A_0}{a} \tag{3.43}$$

and:

$$A_0 = \left.\frac{dV_o(t_k)}{dV_d(t_k)}\right|_{V_d=0} = a \cdot b \cdot (1 - \tanh^2(0)) = a \cdot b \tag{3.44}$$

Using this approximation for the static characteristic and recalling (3.33), the asymptotic value of $V_x(t)$ is rewritten as:

$$V_x^{\infty} = -\frac{1}{b} \cdot atanh\left(\frac{V_o^*}{a}\right) \tag{3.45}$$

The plot of the real op-amp I/O characteristic and the hyperbolic approximation is reported in Fig. 3.6.

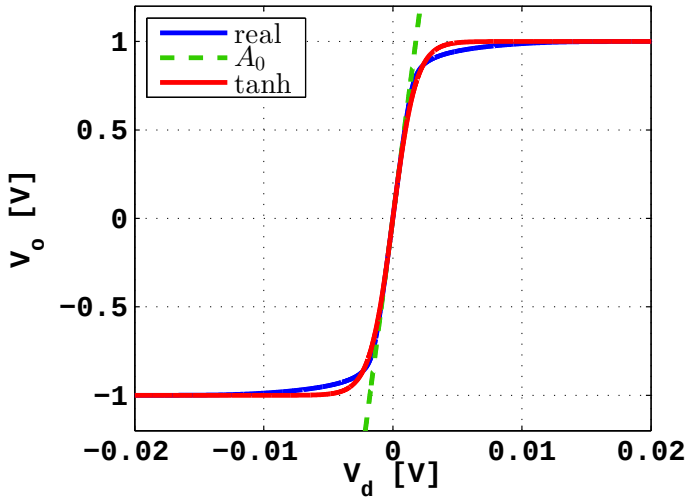


Figure 3.6: Real op-amp I/O static characteristic (blue line) and hyperbolic tangent approximation (red line).

3.6 Thermal Noise Modelling

Electronic noise generated in transistors is present in any circuit implementation and imposes an ultimate limit to the resolution of ADCs, especially in SC ΣΔM. This is because white spectrum of the main circuit noise sources components (broadband noise), are sampled together with the input signal at the clock frequency, so that they fold-over the modulator band and cause an increase of the modulator in-band noise due to aliasing [12], as discussed in Sec. 2.4. The noise floor of a SC ΣΔM is due to the quantization noise and to the noise generated by the integrator. While the former contribution does not require a significant modelling effort, the latter noise contribution must be carefully estimated since in a low-power design may have a relevant impact on the converter SNR.

A CDS based-integrator is used as first integrator into the ΣΔ loop, as described in Sec. 2.5.2, the noise switches are highlight in Fig. 3.7a. The noise contributions in the SC integrator circuit, as discussed in Sec. 2.5, are: the switches thermal noise

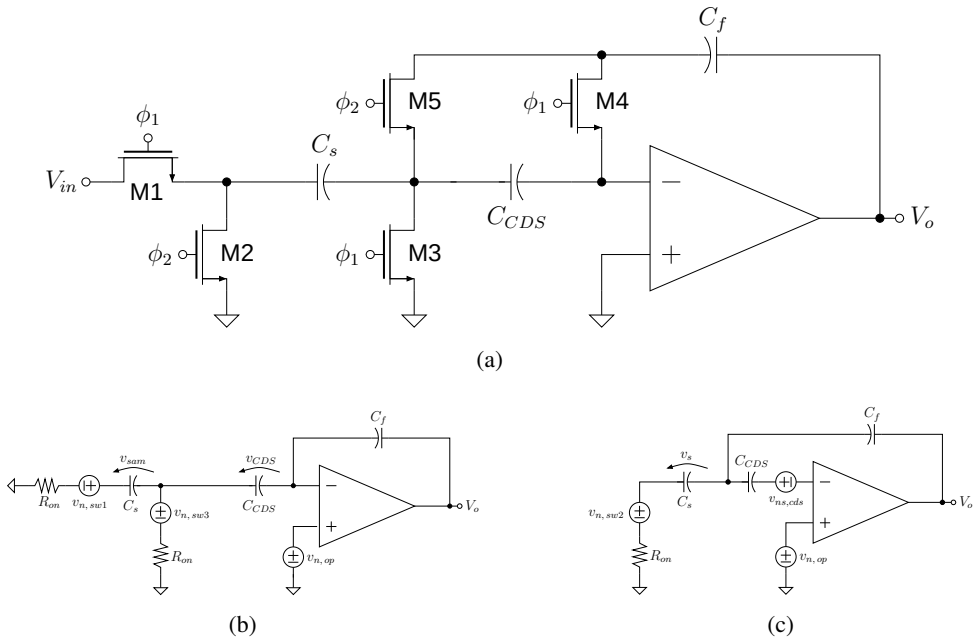


Figure 3.7: (a) Switched-capacitor CDS based integrator, CMOS switches are highlighted. (b) Noise sources in sampling phase (ϕ_2). (c) Noise sources in integration phase (ϕ_1).

and the op-amp voltage noise. The noise performance are determined mainly by the transition frequency of the loop gain set by the switches on state resistance and C_s in sampling phase and op-amp noise of the input stage. The total voltage noise power due to the sampling switches in the sampling phase is equal to kT/C [3]. In a first design phase, the value of the sampling capacitor is thus sized by equating the kT/C contribution to a fraction of the maximum allowed modulator noise referred to the input.

After this first sizing, the project of the integrator must be finalized by taking into account the noise from the switches in the integration phase and the op-amp noise. Accurate noise models have been proposed in literature in the past [30]. The common problem of many noise models is the requirement of the values of several circuit-dependent and technology parameters. In the proposed model only three parameters

are required for the op-amp in Fig.3.7a, as discussed in Sec. 3.6.1: ω_t, PM and the input-referred white noise power spectral density, N_{op}.

3.6.1 Integrator Noise Model

The equivalent input and output noise of the SC integrator of Fig. 3.7a can be split in two contributions: sampled noise and broadband noise. The former type of noise adds to the sampled voltage on capacitor C_s, while the latter one generates an equivalent output voltage noise. Due to the transfer function of the integrator in the Z-domain the broadband noise has a negligible contribution and it is usually neglected in the noise analysis. Fig. 3.7b and Fig. 3.7c show respectively the thermal noise sources in sampling and in integration phase. All the switches are assumed to exhibit the same on-state resistance, R_{on}. Considering the circuit in sampling configuration, Fig. 3.7b, switches M1 and M3 affect the sampled voltage due to their thermal noise contribution. As known, the MS value of sampled thermal noise on C_s as due to switches in on-state are:

$$v^2_{ns,sw1,s} = \frac{8kTR_{on}}{4\,\tau_{sam}} = \frac{kT}{2C_s} \tag{3.46}$$

$$v^2_{ns,sw3,s} = \frac{8kTR_{on}}{4\,\tau_{sam}} = \frac{kT}{2C_s} \tag{3.47}$$

where $\tau_{sam} = 2R_{on}C_s$ is the time constant of the RC circuit made by M1, M3 in on-state and C_s, provided that the impedance of C_{CDS} is much higher that R_{on}.

In the integration phase the noise is contributed by the on-state resistance of M2, causing $v_{n,sw2}$ noise voltage, and by the op-amp equivalent input voltage noise $v_{n,op}$. The sampled noise contribution of those sources is obtained as the equivalent noise voltage across capacitor C_s, i.e. v_s. The contribution of M2 in integration phase is therefore:

$$\overline{v^2_{ni,sw2,s}} = \int_{\omega=0}^{\omega=\infty} 4kTR_{on} \cdot |H_{n,sw2}(\omega)|^2 d\omega \tag{3.48}$$

where $H_{n,sw2}(\omega)$ is the noise transfer function from $v_{n,sw2}$ to the voltage across C_s, i.e. $H_{n,sw2} \equiv v_s / v_{n,sw2}$.

This transfer function is obtained from the circuit in Fig. 3.7c and the open-loop voltage gain of the op-amp. As discussed in Sec. 3.3.4, an equivalent first-order transfer

function can be used to model the integrator in closed loop. The result is still accurate provided that the effect of further poles and additional zeros in the op-amp transfer function is taken into account using a closed-loop time constant defined in (3.30). The 3-dB bandwidth of the integrator (in closed loop) is thus modelled as:

$$A_{int}(\omega) \approx \frac{1/\beta}{1 + j\omega/\omega_{int}} \tag{3.49}$$

$$\omega_{int} = \frac{1}{\tau_{int}} = \frac{\omega_t}{2} \cdot tan(PM) \tag{3.50}$$

The approach used in Sec. 3.3.4 can thus be used for obtaining an equivalent first-order transfer function for the op-amp in open-loop configuration, leading to a closed loop 3-dB angular frequency equal to ω_{int} for the integrator:

$$A_{1st}(\omega) \approx \frac{A_0}{1 + j\omega/\omega_{p1,eq}} \tag{3.51}$$

where:

$$\omega_{p1,eq} = \frac{\omega_{int}}{\beta A_0} \tag{3.52}$$

$H_{n,sw}(s)$ is derived by analysis of circuit in Fig. 3.7c without noise sources $v_{n,op}$ and $v_{ns,cds}$:

$$H_{n,sw2}(s) = \frac{1 + \dfrac{s}{\omega_{ta,eq}}}{s^2 \cdot \dfrac{\tau_{sam}}{2\omega_{ta,eq}} + \dfrac{s}{\beta\,\omega_{ta,eq}} + 1} \tag{3.53}$$

It is worth to be noticed that $\tau_{sam} \ll \omega_{ta,eq}$ since the bandwidth of the RC sampling circuit, left part of Fig. 3.7c, is usually much larger than the unity-gain bandwidth of the op-amp. Therefore $H_{n,sw}(s)$ exhibits two well separated real poles and can be approximated as:

$$H_{n,sw2}(s) \approx \frac{1 + \dfrac{s}{\omega_{ta,eq}}}{\left(1 + \dfrac{s}{\beta\,\omega_{ta,eq}}\right) \cdot \left(1 + s \cdot \dfrac{\beta\,\tau_{sam}}{2}\right)} \tag{3.54}$$

Using the approximate expression of $H_{n,sw2}(\omega)$ from (3.54) in (3.48) the MS value of the sampled noise contribution from M2 is found:

$$v_{ni,sw,s}^2 = 4kTR_{on} \cdot \left[\frac{\beta\,\omega_{ta,eq}}{4} \cdot \left(1 - \beta^2\right) + \frac{\beta}{2\tau_{sam}}\right] \tag{3.55}$$

From (3.50) and using the definition of τ_{sam} the previous equation can be rewritten as:

$$v_{ni,sw2,s}^2 = \frac{kT}{C_s} \cdot \left[\frac{\omega_{int}}{\omega_{sam}} \left(1-\beta^2\right) + \beta \right] \tag{3.56}$$

where $\omega_{sam} \equiv 1/\tau_{sam}$ is the 3-dB bandwidth of the circuit in sampling-mode. It is interesting to calculate the contribution of the thermal noise of M2 in the case with a feedback factor either low or close to unity:

$$v_{ni,sw2,s}^2 (\beta \to 0) = \frac{kT}{C_s} \cdot \frac{\omega_{int}}{\omega_{sam}} \tag{3.57}$$

$$v_{ni,sw2,s}^2 (\beta = 1) = \beta \cdot \frac{kT}{C_s} \tag{3.58}$$

The contribution of the op-amp noise, $v_{ni,op,s}^2$, in the integration phase is:

$$v_{ni,op,s}^2 = \int_{\omega=0}^{\omega=\infty} v_{n,op}^2 \cdot |H_{n,op}(\omega)|^2 d\omega \tag{3.59}$$

where $H_{n,op}(\omega) \equiv v_s/v_{n,op} = \beta A_{int}(\omega)$ is the noise transfer function from the input op-amp noise to the sampling capacitor in integration mode. Therefore, from (3.59):

$$v_{ni,op,s}^2 = N_{op} \cdot \left(\frac{\omega_{int}}{4} \right) \tag{3.60}$$

where N_{op} is the power spectral density of the op-amp input noise voltage. In the present analysis the $1/f$ op-amp noise is not considered since it is completely rejected by the CDS, provided that the corner frequency of the $1/f$ noise is lower than the Nyquist frequency of the SC integrator.

In the sampling phase the op-amp noise and the thermal noise of M3 are stored and sampled on C_{CDS} capacitor. This sampled noise, v_{CDS}, can be obtained with the same approach used for the noise caused by M2 and by the op-amp in the integration phase. Nevertheless a different time constant then in (3.30) must be used here:

$$\tau_{s-cds} \equiv \frac{2}{\beta_{cds}\, \omega_t \cdot \tan(PM)} \tag{3.61}$$

where the feedback factor of the circuit involving the op-amp in sampling mode is:

$$\beta_{cds} \equiv \frac{C_f}{C_f + C_{CDS}} \tag{3.62}$$

It is worth to be noticed that, in the linear model used to obtain the equivalent time constants τ_{int} and τ_{s-cds}, the effect of switch resistance was not taken into account. Other authors consider the effect of such resistance in the noise estimation at the cost of a higher complexity of the model [31]. If the analysis is focused on a low-power design context, the major bandwidth limitation is due to the op-amp, while switches in on-state have a negligible impact.
From (3.61) an equivalent 3-dB bandwidth for the feedback circuit in sampling mode is thus defined:

$$\omega_{s-cds} = \frac{1}{\tau_{s-cds}} \tag{3.63}$$

The equation of the voltage noise sampled on C_{CDS} in sampling mode due to the thermal noise of M3, $v^2_{ns,sw3,cds}$, and to the op-amp noise, $v^2_{ns,op,cds}$ are obtained with the same procedure used for (3.56) and (3.60), respectively.

$$v^2_{ns,sw3,cds} = \frac{kT}{C_s} \cdot \left[\frac{\omega_{s-cds}}{\omega_{sam}} \cdot \left(1 - \beta^2_{cds}\right) + \beta_{cds} \right] \tag{3.64}$$

$$v^2_{ns,op,cds} = N_{op} \cdot \left(\frac{\omega_{s-cds}}{4} \right) \tag{3.65}$$

In the integration phase, the noise transfer function from $v_{ns,CDS}$ to v_s, Fig. 3.7c is equal to unity. However, it has to be noticed that the noise voltage from M3 is sampled on C_s and C_{CDS} at the same time, therefore random noise processes causing $v_{ns,sw3,cds}$ and $v_{ns,sw3,s}$ are fully correlated.

The overall sampled voltage noise referred to the modulator input is obtained by summing the power of the uncorrelated contribution as in (3.66), where the noise power from M3 corresponds to the absolute value of the difference between $v^2_{ns,sw3,cds}$ and $v^2_{ns,sw3,s}$.

$$v^2_{n,in} = v^2_{ns,sw1,s} + |v^2_{ns,sw3,s} - v^2_{ns,sw3,cds}| + v^2_{ni,sw2,s} + v^2_{ni,op,s} + v^2_{ns,op,cds} \tag{3.66}$$

In the behavioural model of the modulator in Fig. 3.10 sampled noise due to switches and op-amp are implemented as separate Gaussian random number generators with variance equal to $v^2_{n,sw}$ and $v^2_{n,op}$ in (3.67) and (3.68). Modulator loop coefficients for

a single-loop third-order CIFF architecture are reported in Tab. 2.1.

$$v_{n,sw}^2 = \frac{kT}{2C_s} + \left| \frac{kT}{2C_s} - \frac{kT}{C_s}\left[\frac{\omega_{s-cds}}{\omega_{sam}}\left(1-\beta_{cds}^2\right)+\beta_{cds}\right]\right| + \cdots \\ \cdots + \frac{kT}{C_s}\left[\frac{\omega_{int}}{\omega_{sam}}\left(1-\beta^2\right)+\beta\right] \tag{3.67}$$

$$v_{n,op}^2 = \frac{N_{op}}{4}\cdot\left(\omega_{int}+\omega_{s-cds}\right) \tag{3.68}$$

It is worth to be noticed that this noise model requires only three op-amp parameters: ω_t, PM, N_{op}, with the value of the sampling capacitor C_s and the feedback factor β. Dynamic op-amp parameters are found in the first optimization phase, using the accurate non-linear model proposed in Sec. 3.3.4 and starting with a conservative estimation for C_s. With the noise model the value of C_s and N_{op} are optimized for minimum power consumption.
The value of the on-state switch resistance is required in (3.56). In a first design step the designer can set $\omega_{sam} = \omega_{int}$. The minimum acceptable value for ω_{sam} is found from fast noise simulation with the proposed behavioural model and from the maximum acceptable settling error in the sampling phase.

3.7 Design Example

The proposed model was validated in the design of a low-pass ΣΔM in 65-nm STM CMOS technology based on a single-loop third-order fully-differential CIFF architecture, Fig. 3.8. The target resolution is 16-bit and a summary of the other metrics is reported in Tab. 2.2. The design is carried out using the proposed behavioural model, implemented in Matlab or similar framework, and a transistor level simulator (Eldo or Spectre). The design steps are shown in the flow-chart in Fig. 3.9. In the first step, (**A**), the designer selects the modulator architecture and order (i.e. the number of integrators in the loop) on the basis of the specifications of the ΣΔ converter. The capacitance ratio, i.e. C_f/C_s, for each integrators are calculated by means of a mathematical modulator model [9] and reported in Tab. 2.1. It has to be noticed that the

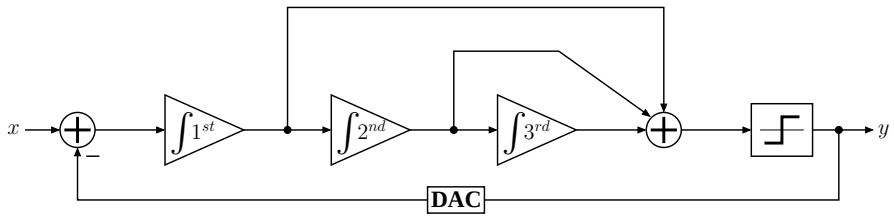


Figure 3.8: Third-order ΣΔM structure.

feedback capacitance adds to the load capacitance, C_L, and thus directly affects the integrator PM or unity-gain angular transition frequency, ω_t.

In the next design step, (**B**), a preliminary estimation of the first integrator parameter is carried out. The sampling capacitor, C_s, of the first integrator is estimated to satisfy the kT/C noise requirement [32]:

$$C_s^* = \frac{8kT \cdot DR}{V_{DD}^2 \cdot OSR} \tag{3.69}$$

where T is the absolute temperature, DR is the dynamic range, OSR is the oversampling ratio, and V_{DD} is used as the amplitude of a full-scale sinusoidal input. The DR is set to 106-dB for a design margin, 5÷10-dB is usually assumed as margin as adopted in [33]. For a power supply of 1.2-V, the required sampling capacitor, C_s, is set to 2-pF, with an extra noise margin. The other capacitors are selected to satisfy the modulator coefficients. The sampling capacitors value are reported in Tab. 3.1. The sampling capacitors of the second and third stage are close to the minimum value allowed by the technology and are sized without any noise consideration, since their impact on the modulator SNR is negligible but affects the total load capacitor C_L of each integrators.

The differential input pair of the op-amp, due to a low power constraint, is biased in moderate inversion region, e.g. $V_{GS} - V_T$ =80-mV, resulting in an inversion-factor, I_F, of 2. Typical values of $V_{GS} - V_T$ are between 0.08÷0.2-V [34]. This is a good trade-off among speed, power, noise and area. Recalling (3.12) an approximate value of $n \cdot v_{th} \approx$35-mV is taken [34], from which results g_m/I_d =14.3-V^{-1}.

To estimate the SR requirements, it is worth to be noticed that the worst transient

in the integration phase occurs when the negative differential feedback voltage, V_R in Fig. 3.3, is equal to −1-V and is subtracted from the maximum input voltage, e.g. 0.9-V, giving a total $\widetilde{V}_{in_{max}} \simeq 1.9$-V. Allocating 25% of a half-clock period for slewing (an equal time interval, $T_{CK}/4$, for both slewing and linear response) a first evaluation can be calculated:

$$SR^* \approx \frac{\widetilde{V}_{in_{max}}}{T_{CK}/4} = 1.9\,\frac{\mathrm{V}}{\mu\mathrm{s}} \tag{3.70}$$

In order to reach the target ENOB, integration settling error must be smaller than $1/2\ LSB = 2^{-N}/2$.

$$\mathrm{e}^{-\frac{T_{CK}}{4\,\tau_{int}}} = \mathrm{e}^{-\frac{\omega_{int}}{4\,f_{CK}}} < 2^{-(N+1)} \tag{3.71}$$

Therefore also the ω^*_{int} can be estimated:

$$\omega^*_{int} > f_{CK} \cdot 4(N+1)\ln 2 \simeq 11.75\,\frac{\mathrm{Mrad}}{\mathrm{s}} \tag{3.72}$$

Recalling (3.30) and assuming PM equal to 60°, which means that the step response of the feedback system exhibits little ringing providing a fast settling, results $\omega^*_{int} \simeq \omega^*_t$.

Although it is not possible to obtain an accurate estimation for the required DC-gain without knowledge of the non-linear nature of the op-amp's static characteristic, a common source output stage can be assumed. The DC-gain can be estimated using the intrinsic gain of a transistor:

$$A^*_0 \approx g_m \cdot r_{ds} \approx 30\text{-dB} \tag{3.73}$$

where r_{ds} is the drain-source resistance. An approximate value of 30-dB is usually assumed for short channel devices.

Starting from these values of first approximation, parametric simulations can be performed using Simulink model, step (**C**). The purpose is to refine op-amp's dynamic requirements (SR and ω_t) to waste less power as possible. Moreover, op-amp's design space can be explored including other additional variables: DC-gain (A_0), output range ($V_{o_{MAX}} - V_{o_{MIN}}$), capacitive load ($C_L$) and PM. Prior to run parametric simulations the six variables must be paired off so that while one pair is swept, the others

two are maintained constant. Actually, C_L^*'s value represents a project's degree of freedom, on condition that its realization is feasible, of course, and from (3.9) results $|V_x|_{max} < V_{DD}$. Starting from dynamic requirements (SR and ω_t), while static non-idealities can be deactivated (A_0 and PM). Behavioural simulation with two value of C_L^* are performed. As a first approximation C_L^* is set equal to the sampling capacitance of the second integrator, i.e C_{s_2} in Tab. 3.1, while in the second case is set equal to C_s^*, which is close to the transistor-level simulated load. Results obtained from behavioural simulations are shown in Fig. 3.11. The set of all feasible design alternatives for the system forms the red zone. Once determined a value for SR and ω_t, is possible to sweep PM and C_L, Fig. 3.11c. At least it is the turn of op-amp's static requirements, DC-gain (A_0) and output range ($V_{o_{MAX}} - V_{o_{MIN}}$) enabling I/O characteristic effects through a simple linear approximation or the one based on hyperbolic tangent, Fig. 3.11d.

On the basis of the specification obtained in step (**C**), the transistor level design of the first integrator takes place, step (**D**). Now the others parameters can be accurately estimated by means of transistor level simulations: g_m/I_d, τ_{int} and τ_{sam}, the op-amp output range ($V_{o_{MAX}} - V_{o_{MIN}}$), N_{op} and finally C_L. Then a full behavioural simulation with the Simulink model in Fig. 3.10 is performed, step (**E**). After that, if the SNR is below the target, the value of C_s^* and N_{op} must be adjusted. Else if the THD is below the target, transistor-level simulation could be performed, step (**F**). Otherwise a new optimization process, step (**C**), takes place.

The above discussion dealt only with the op-amp requirements in the first integrator. Distortion, settling and noise requirements of the others op-amps are greatly relaxed. In this example the others op-amps are a copy of the first, scaled down in current biasing by a factor 2, and 3 for respectively second, third and adder stage. The values of the sampling capacitors of this design are reported in Tab. 3.1.

3.7.1 Simulation Results

Two different op-amp's architecture are exploited in this design, depicted in Fig. 3.14. Both exploit current cancellation through local positive feedback [32] through MN6 and MN7. The op-amp in Fig. 3.14a, *OA-1*, is a Miller compensated op-amp with

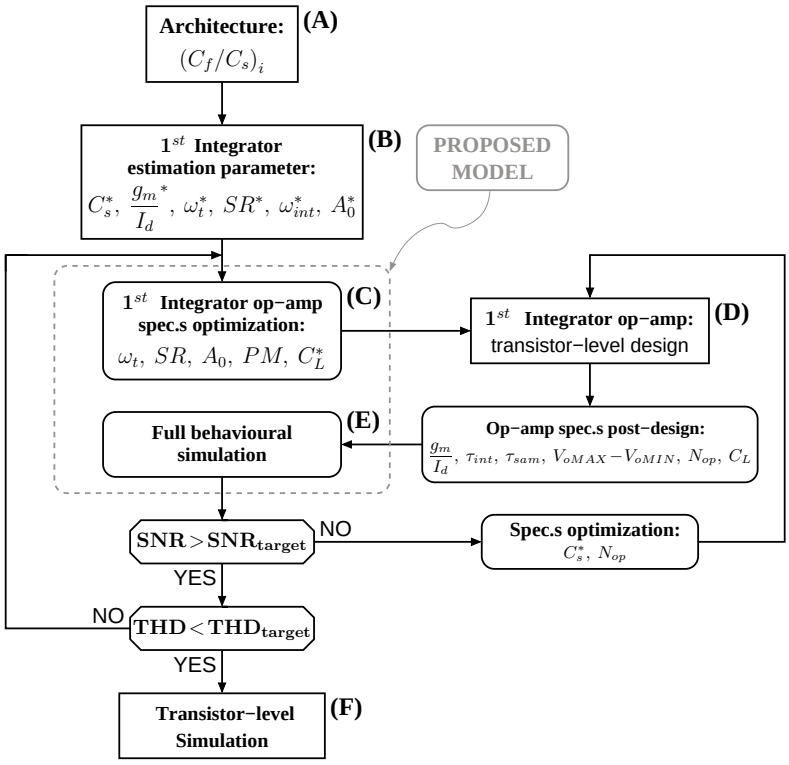


Figure 3.9: Flow-chart: design and verification steps.

class-A output stage. While the op-amp in Fig. 3.14b, *OA-2*, with a class-AB output stage, has the benefit, compared to a conventional Miller compensated op-amp, to achieve the same ω_t with a smaller C_c, due to the multiplication effect obtained by means of $g_{m_{18-19}}$. Tab. 3.3 reports op-amps' performances (in typical case) together with the target values returned by parametric simulations. The second part of Tab. 3.3 contains noise related quantities calculated applying (3.50) and (3.76).

Simulations are performed with a pure sine-wave input signal, 0.9-V amplitude and 36-Hz frequency. Results about harmonic distortion, obtained with *OA-1*, are reported in Tab. 3.2 and in Fig. 3.12 and show the high degree of accuracy achieved by the proposed model. FFT spectra are calculated over 2^{17} samples with Hann window-

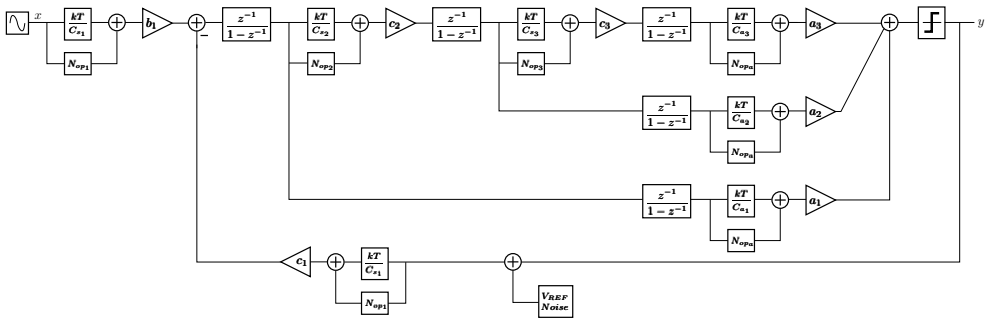
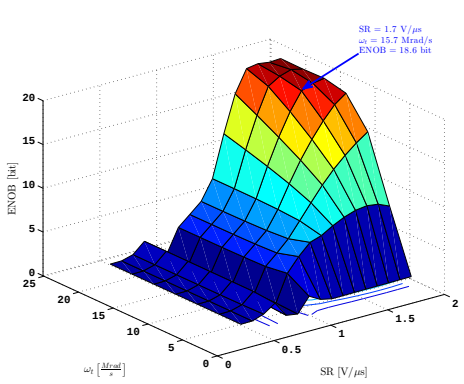


Figure 3.10: Behavioural model in Simulink.

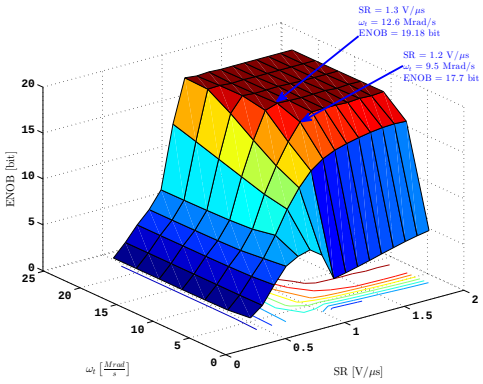
Table 3.1: Modulator sampling capacitors.

Capacitor	Value	Unit
C_{s_1}	2	pF
C_{s_2}	0.25	pF
C_{s_3}	0.25	pF
C_{a_1}	0.25	pF
C_{a_2}	0.25	pF
C_{a_3}	0.38	pF

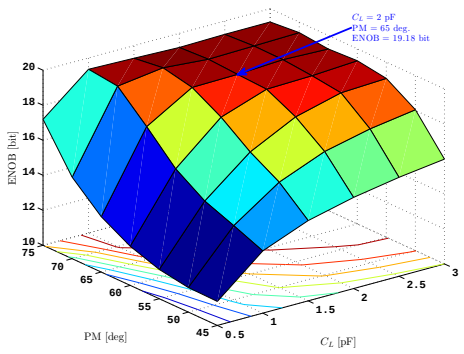
ing. The amplitude of the main in-band harmonics are in good agreement with the transistor-level simulation performed with commercial simulators (i.e. Spectre and Eldo). It is worth noticing that harmonics' amplitude depends mainly on dynamic op-amp's performances whereas at lower frequencies the impact of static op-amp's characteristic is relevant. Green dashed line in Fig. 3.12, indeed, display Simulink results with static characteristic's effects disabled (i.e. $A_0 = \infty$). It is clearly too low compared to the Spectre simulation's FFT. Enabling the linear approximation ($A_0 \neq \infty$) of static effects (orange dashed line) slightly improves the low frequency agreement with Spectre, but it is the red line (hyperbolic tangent approximation) the one which



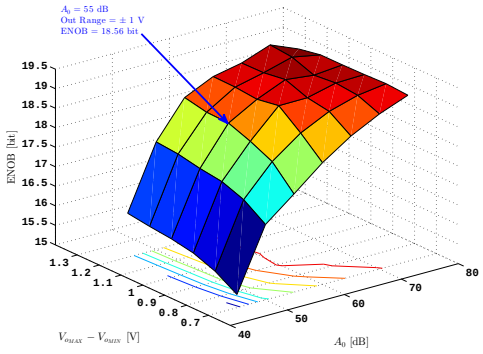
(a) ENOB Vs. ω_t and SR (@C_L=0.125-pF)



(b) ENOB Vs. ω_t and SR (@C_L=2-pF)



(c) ENOB Vs. PM and C_L



(d) ENOB Vs. $V_{o_{MAX}} - V_{o_{MIN}}$ and A_0 (@C_L=2-pF)

Figure 3.11: Parametric simulations.

fits most closely the blue line.

FFTs of Fig. 3.13 show the high effectiveness achieved by the model in evaluation of modulator's SNR. Green line, related to quantization noise only, is included for reference. Neglecting contributions from stages with order greater than one, the in-band SNR results:

$$SNR_{[dB]} = 10\log_{10}\frac{\overline{v_s^2}}{\overline{v_{n,q[b]}^2}+\overline{v_{n,sw[b]}^2}+\overline{v_{n,op[b]}^2}} \tag{3.74}$$

where $\overline{v_s^2}$ represents the average power of the 0.9-V sine-wave input signal. $\overline{v_{n,q[b]}^2}$ represents the in-band quantization noise, 0.98-μV^2. While $\overline{v_{n,sw[b]}^2}$ represents the in-band switches' thermal noise, recalling (3.67):

$$\overline{v_{n,sw[b]}^2} = \frac{v_{n,sw}^2}{OSR} \tag{3.75}$$

and $\overline{v_{n,op[b]}^2}$ is the average power of *in-band* op-amp's thermal noise, recalling (3.68):

$$\overline{v_{n,op[b]}^2} = \frac{v_{n,op}^2}{OSR} \tag{3.76}$$

Using the values reported in Tab. 3.3, (3.74) gives SNR(*OA-1*)=103.7-dB and SNR(*OA-2*)=99-dB. These results therefore confirm the validity of the proposed model for the accurate SNR estimation of the modulator.

Table 3.2: Summary of harmonics' amplitudes.

Harmonic	**Spectre**	**Simulink**	**Unit**
3^{rd} harmonic	-124.67	-125.85	dB
5^{th} harmonic	-119.41	-122.06	dB

3.8 Conclusion

An improved Simulink model focused on the accurate estimation of harmonic distortion and SNR in ΣΔMs is proposed. The model allows to optimize the op-amp

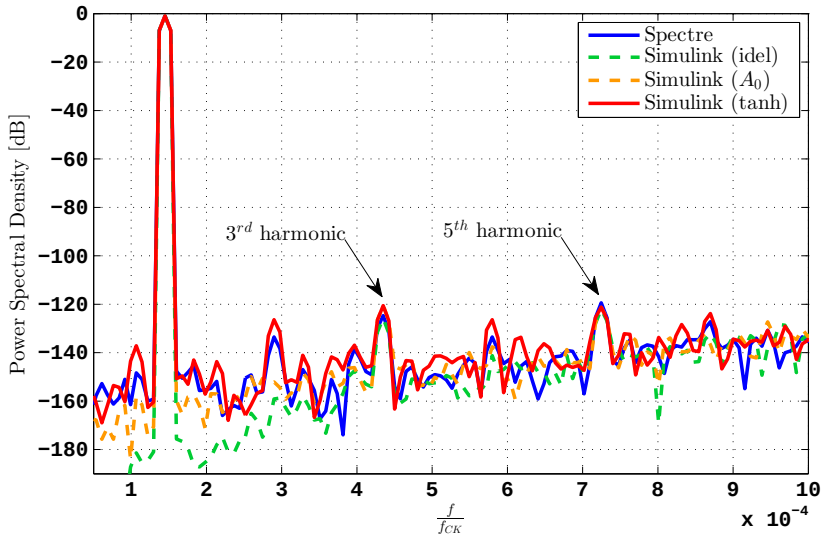
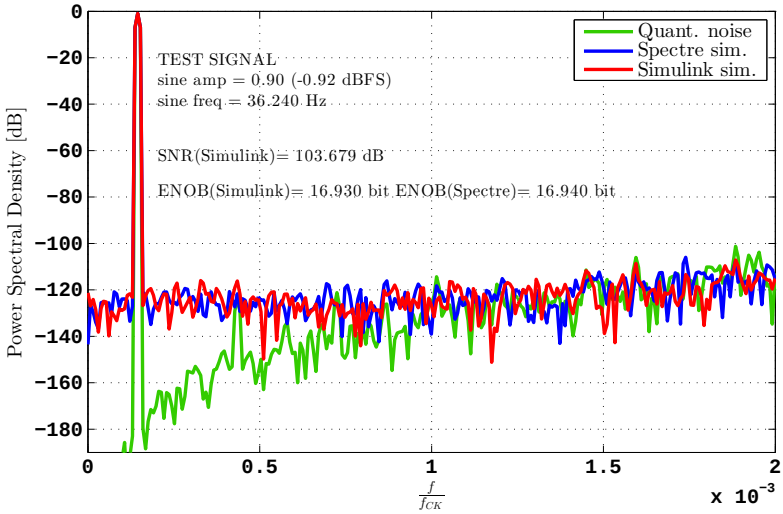
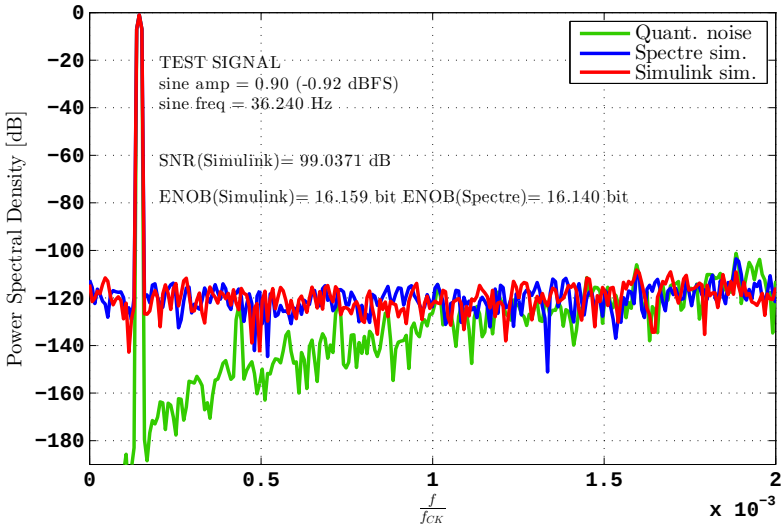


Figure 3.12: Simulation comparison between Simulink model (red line) and Spectre simulator (blue line) about harmonic distortion.

specifications in a power-limited modulator design. The simulated output spectra are in strict agreement with the results obtained with time consuming transistor-level simulations, thus proving the importance of the improvements carried out on state-of-the-art models in case of a low power modulator implementation. Effectiveness of the model was proved in two design cases, thus showing that this model is not strictly op-amp's circuit dependent.

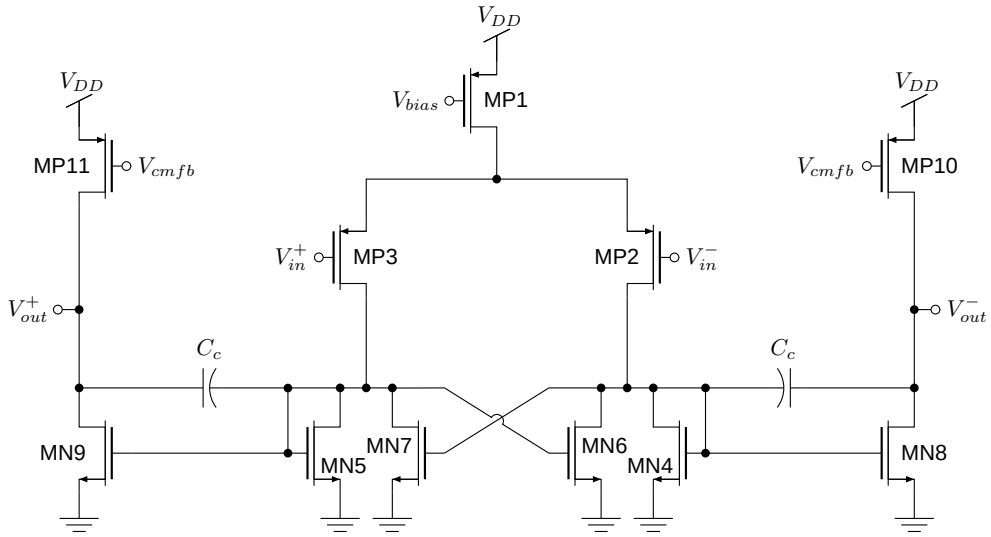


(a) *OA-1* spectrum

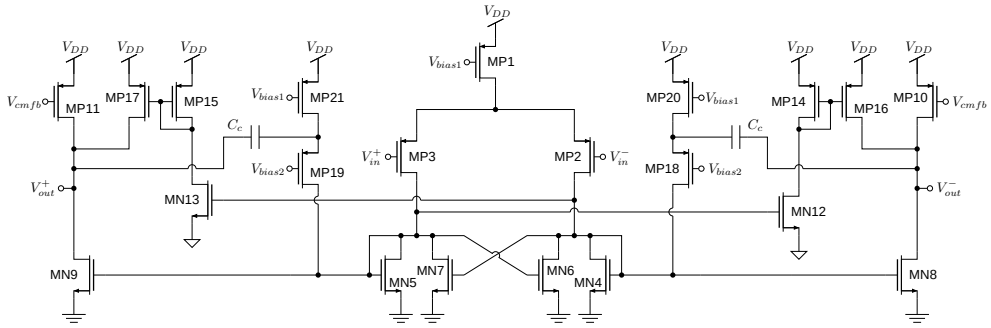


(b) *OA-2* spectrum

Figure 3.13: Simulation comparison between Simulink model (red line) and Spectre simulator (blue line) with thermal noise sources enabled.



(a) Schematic of the class-A op-amp, *OA-1*.



(b) Schematic of the class-AB op-amp, *OA-2*.

Figure 3.14: Simplified fully differential op-amps schematics. V_{cmfb} is the CMFB voltage.

Table 3.3: Summary of op-amp's metrics.

Metric	**Minimum**	*OA-1*	*OA-2*	**Unit**
A_0	50	58	55	dB
$V_{oMAX} - V_{oMIN}$	± 0.8	± 1	± 1	V
ω_t	9.4	9.4	13.8	Mrad/s
PM	65	66	71	deg.
SR	1.3	1.47	1.85	V/μs
$\sqrt{N_{op}}$	-	43	60	nV/$\sqrt{\text{Hz}}$
ω_{int}	10.1	10.7	20.1	Mrad/s
ω_{s-cds}	-	8.2	18.9	Mrad/s
$\overline{v^2_{n,op[b]}}$	-	8.6	35.6	μV^2

Chapter 4

A 1.2-V, 50-μW, 98-dB DR $\Sigma\Delta$ Modulator in 90-nm CMOS

A good scientist is a person with original ideas. A good engineer is a person who makes a design that works with as few original ideas as possible. There are no prima donnas in engineering.

– John Dyson

This Chapter presents, at the circuit level, the low-voltage building blocks suitable for the design of a ΣΔM in nanometer CMOS technology. At the same time, low-power is a constraint in the design of the building blocks. The device, implemented in a 90-nm CMOS technology, is designed for portable applications, where silicon area is critical. The designed ΣΔ exhibits a differential input and uses two-stage op-amps with class-A output stage. Two-stage op-amps fulfil moderate gain and output swing requirements, but the most challenging issues are imposed by the power consumption and by the SR limiting due to the compensation capacitor. One of the possible solutions is to increase the biasing current of the op-amp, but this leads to a power consumption penalty. A gain-enhanced class-A op-amp is presented firstly. By using this op-amp topology, and scaling down proportionally the power consumption of the op-amps from the first to the third integrator in the loop, a low-

power single-loop third-order SC $\Sigma\Delta$ implemented in a standard digital 90-nm CMOS STM technology is presented, exploring the possibilities of implementing high performance modulators in a standard digital process in nanometer technologies. Finally extensive measurements on noise, distortion, Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR) are discussed.

4.1 Low-Power Op-amp with Class-A Output Stage

The most critical part of the $\Sigma\Delta$M is the op-amp. The first op-amp has a dominant impact on the modulator performance, hence exhibits more than 50% of the overall power consumption. The class-AB circuit is known to be more power efficient, therefore, and is widely used [35]. However, a drawback of the class-AB architecture is that it requires extra circuit to control the quiescent current of the P-MOS and N-MOS output transistors. This design choice is exploited in Chapter 5.

In this design a single-stage class-A architecture, Fig. 4.1a, with local positive feedback [32] to increase amplifier DC-gain and Gain Bandwidth (GBW) is used. The technique is best applied to fully differential op-amp due to the nominally exact impedance balancing of the positive and negative outputs [36]. Direct creation of a negative output resistance is not feasible though, since whenever two transistors outputs are connected in parallel, their (positive) output resistances always add in parallel. Instead, partial positive feedback is created by employing a negative transconductance, $-g_m$, steered by the negative output voltage in order to cancel the op-amp output conductance. The modified conventional approach [37] to output resistance cancellation through positive feedback, is implemented by the addition of MN6 and MN7 causing a reduction of the effective output conductance and hence an increase of DC-gain, A_0:

$$A_0 = g_{m_3} R_{out} \cdot \frac{\varsigma}{1-\kappa} \tag{4.1}$$

$$GBW = \frac{g_{m_3}}{C_c} \cdot \frac{\varsigma}{1-\kappa} \tag{4.2}$$

where $\varsigma = (W/L)_9/(W/L)_5$, $\kappa = (W/L)_7/(W/L)_5$ and R_{out} is the output resistance of the op-amp. The effect of the drain-source resistances of the input pair and the

current steering transistors are neglected since the resistances are large because of the small amount of current and relatively large transistor lengths. If the amount of positive feedback is larger than 1, the circuit becomes a latch leading to instability in the integrator. In this design, the parameters are $\kappa = 0.8$ and $\varsigma = 15$. A practical maximum value for κ is 0.9, because beyond that any mismatches may cause the value to approach unity [38].

Tab. 4.1 shows the simulation results of the designed op-amp. In order to evaluate the performance of the op-amp in the capacitive feedback configuration, the effective load capacitances, C_L, is estimated with a transistor-level simulation. During the sampling phase the op-amp has lower C_L, which means a lower PM compared to the integrating phase. With the measured value of the load capacitance, C_L, of 2-pF the first op-amp exhibits: 58-dB DC-gain, 1.5-MHz GBW and an input referred thermal noise, N_{op}, of 43-nV/$\sqrt{\text{Hz}}$.

The op-amp was sized (transistors' aspect ratio and bias current) over process, mismatch and temperature range (−40°C÷80°C). The unity-gain-transition frequency, f_t, and the PM are obtained in feedback configuration (integrator's loop gain). The required compensation capacitor C_c is about 1.8-pF.

Table 4.1: Summary of the op-amp spec.s.

Metric	**Typ. Value**	**Unit**
A_0	58	dB
SR	1.47	V/μs
N_{op}	43	nV/$\sqrt{\text{Hz}}$
f_t	1.5	MHz
PM	66	deg.

4.1.1 CMFB circuit

A Common Mode Feedback (CMFB) circuit is necessary for a fully differential op-amp to ensure the required output Common Mode (CM) voltage. An improved version of the SC CMFB circuit, shown in Fig. 4.1b, is used [39]. V_{cm} is the desired

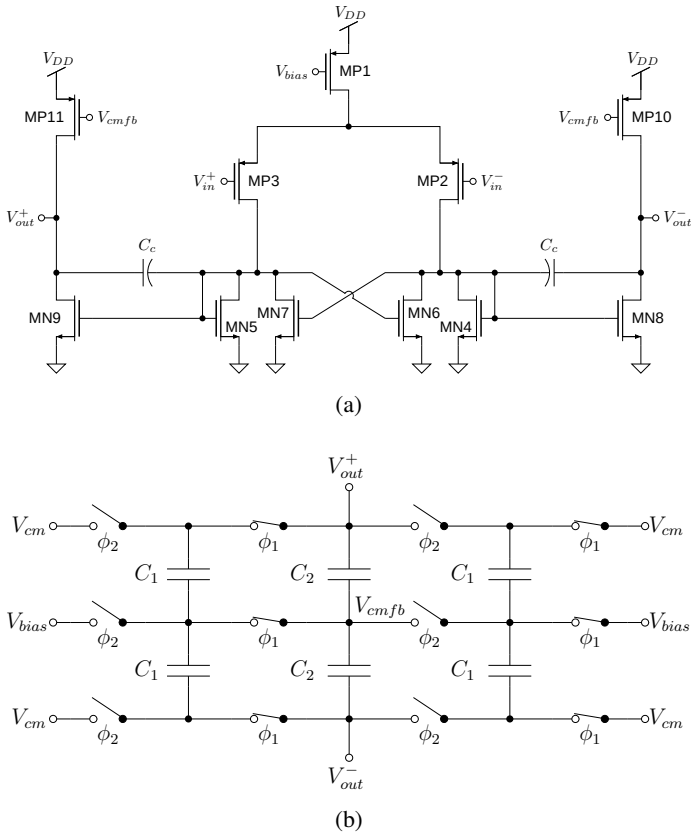


Figure 4.1: (a) Schematic of the class-A gain-enhanced fully differential op-amp. (b) SC CMFB configuration with symmetric loading.

output CM voltage, V_{bias} is the expected bias voltage, and V_{cmfb} is the CM feedback voltage. In the circuit, an extra set of capacitors, C_1 and an extra set of switches are used. Switches on the left side of axis of symmetry through V_{out}^+ and V_{out}^- node, operate with opposite clock phase as compared to those on the right side. Thus, during every clock phase, the total load of the outputs, V_{out}^+ and V_{out}^-, is $C_1 + C_2$ without asymmetry that can destabilize the op-amp. Care should be taken that the GBW of the CM loop should be greater than that of differential loop. The value of C_2 can be determined by making the CM loop bandwidth grater than that of the differential loop. Then C_1 can

be designed 5÷10 times that of C_2 for faster DC settling, lower steady-state errors, charge injection and leakage errors [39].

4.2 Basic Building Blocks

The complete modulator circuit is shown in Fig. 4.2. It exhibits three integrators with a latch comparator. The values of the sampling capacitors are reported in Tab. 3.1, while the modulator coefficients are reported in Tab. 2.1. The input CM voltage, V_{cm}, of the modulator is set to 0.5-V. The reference voltages, V_{ref_P} and V_{ref_N}, are set respectively to 1-V and 0-V (ground). The op-amps used are described in Sec. 4.1. The op-amp in the first integrator exhibits a power consumption of 21-μW. Thanks to the noise suppression inside the loop, the second and third integrator can be sized with a lower consumption, 10.5-μW, while the active op-amp in the adder stage consumes 7.2-μW. Furthermore, the other building blocks are the front-end input sampler described in Sec. 4.2.1, the one-bit quantizer described in Sec. 4.2.2 and the non-overlapping clock phase generator described in Sec. 4.2.3.

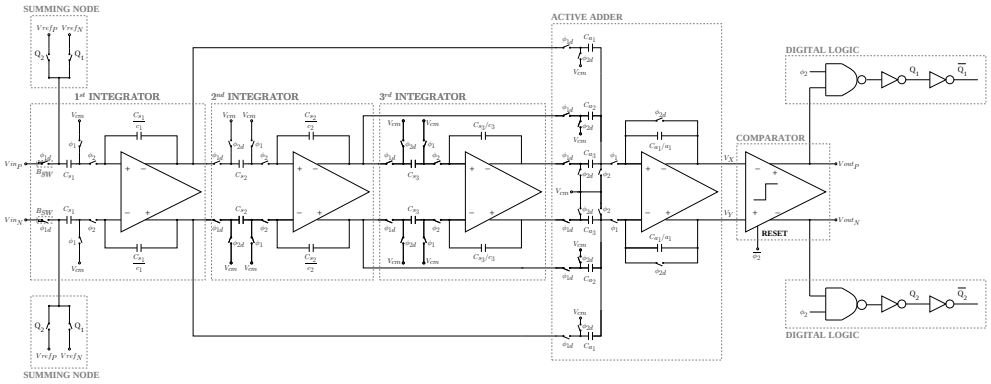


Figure 4.2: Schematic of the proposed third-order ΣΔM.

4.2.1 Bootstrapped Switch

Sampling of the time-varying input signal is the first step in any type of ADC. For high-resolution and low-distortion ΣΔM, a high-linearity input switch circuit is needed as front-end. Sampling switch non-linearity, due to non-linear on resistance and associated parasitic capacitance, produces harmonic distortion when sampling signals. This limits SFDR and THD that are fundamental metrics to evaluate the converter linearity. The linearity of the input sampler switch is very important in ΣΔM, because it is outside the feedback loop. Therefore, the ΣΔM noise shaping cannot attenuate the harmonic distortion added by the sampler. For this reason a bootstrap switch is used instead of a transmission gate switch, to reduce the harmonic distortion of the input sampler. The bootstrap switch used in this design is reported in Fig. 4.3 [40]. Through capacitor C the V_{GS} of the switch MN1, between V_{in_P} and V_{out_P}, is V_{DD} for every value of the input V_{in_P} in order to minimize its on-state resistance. During ϕ_2 the capacitor C is charged to V_{DD} with MN5 and MP2. In ϕ_1, C is connected between the source and the gate of MN1 through MN2 and MP1.

In order to ensure the desired modulator resolution, it is necessary to reduce the parasitic gate resistance of MN1, which has a detrimental effect on the THD of the switch. For this reason a multi-gate design strategy is mandatory. Indeed, if the device consists of multiple fingers, then the overall gate resistance is decreased by χ, where χ is the number of fingers.

4.2.2 One-Bit ADC Quantizer

The one-bit quantizer converts signal at the output of the adder to a digital signal. This is implemented with a dynamic latch comparator, shown in Fig. 4.4. In reset mode, RST is low (0-V), the latch comparator is off and the outputs, V_{out_N} and $V_{out\,p_N}$, are high (V_{DD}). When RST is high with a 0-V differential input, the latch goes in a metastability condition. When a voltage unbalance between the two branches of the circuit occurs, due to the variation of non-zero differential input signal ($V_X - V_Y$), the latch toggles in a stable quiescent point. The threshold voltage is set to V_{cm}.

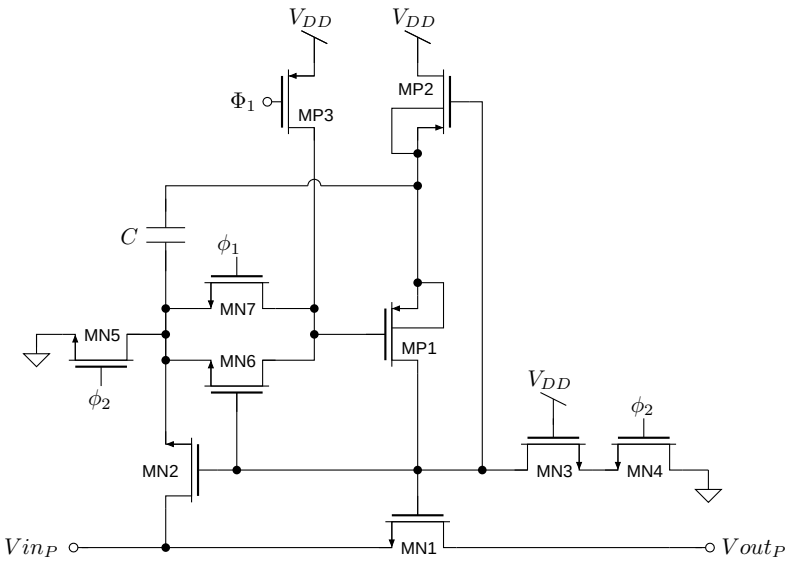


Figure 4.3: Schematic of the bootstrap switch.

4.2.3 Phase Generator

The on-chip clock phase generator is shown in Fig. 4.5. The external clock input signal, *CK*, is buffered and then two non-overlapping clock signals are generated. To avoid the signal dependent charge injection, two delayed clocks, i.e ϕ_{1d} and ϕ_{2d}, are also generated. As clock phases are used in every block of ΣΔM, these signals need to be routed through the entire chip. To this purpose, a U-shaped bus, conceptually depicted in Fig. 4.6, is used. Each clock phase, ϕ_x, is surrounded by ground, GND in Fig. 4.6, strips of the same metal as that used for the clock phases. The whole bus is covered by the same ground above and below the routed phases with plates implemented at the upper and lower metal layers, respectively.

4.2.4 Master Bias Current Generator

All current sources and sinks required to bias the ΣΔ op-amps, need to be generated internally (on-chip) from a master bias current generator. Fig. 4.7 shows the master

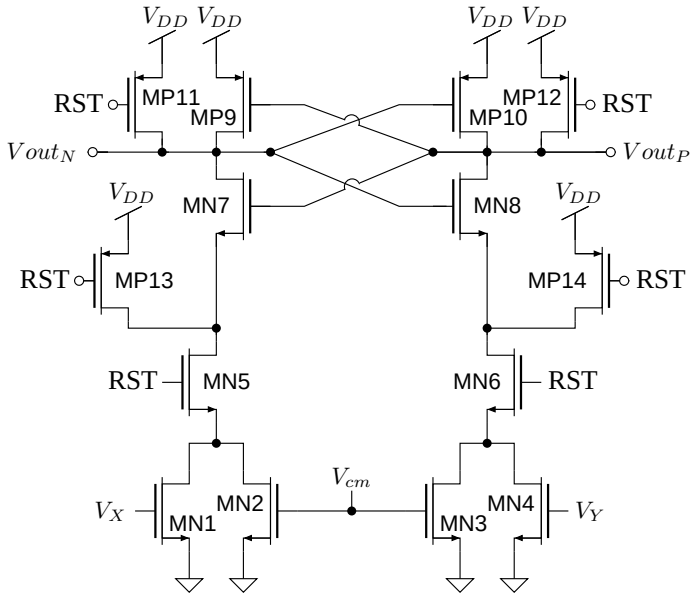


Figure 4.4: Schematic of the latch comparator.

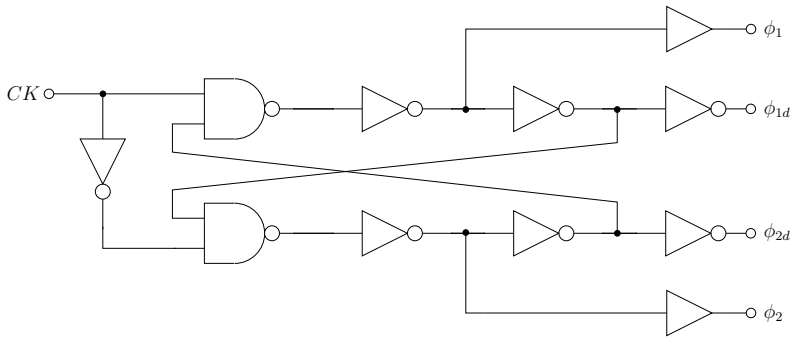


Figure 4.5: Schematic of the clock phase generator.

bias current generator. A master current is generated from the external reference voltage, $V_{ref_{ext}}$, and an external (off-chip) resistor and op-amp. The generated master bias current is mirrored and properly scaled to bias all op-amps used in the integrators and in the active adder. Adaptive bias currents are implemented by means of pro-

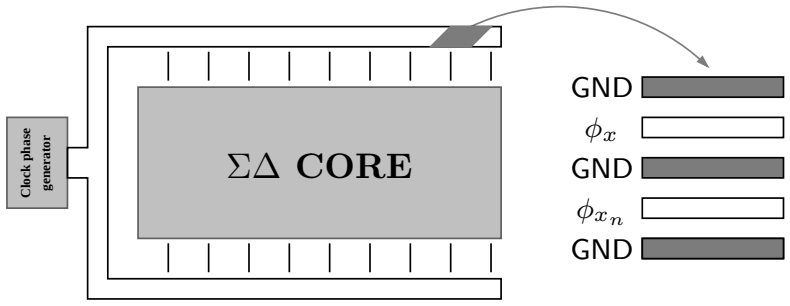


Figure 4.6: Clock-phase distribution and routing along a ΣΔM: conceptual U-shape bus distribution and clock-phase signal isolation using a ground shield.

grammable current mirrors based on the combination of switchable transistors. This way, the performance of the ΣΔ core, can be adapted to a different set of specifications with optimized power consumption.

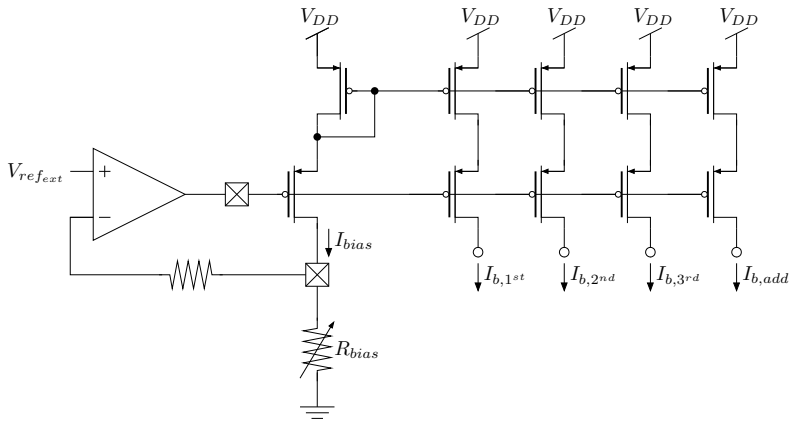


Figure 4.7: Schematic of the master bias current generator.

4.3 Implementation and Measurement Results

The proposed modulator is implemented with a standard 90-nm STM CMOS technology. The chip micrograph is shown in Fig. 4.8, B_{SW} stands for the bootstrap switch. The chip core size is 0.29-mm$\times$1.4-mm. Standard Metal Insulator Metal (MIM) capacitors are used. As the loop coefficients are defined by the capacitance ratios, no robust loop coefficients are required to be more tolerant to the mismatched capacitance. Besides, MOS capacitances are widely used as decoupling capacitors around the chip. The sensitive analog blocks and the noisy digital circuits are separated by a triple-well isolation. To reach the maximum CMRR, all the analog parts and paths are laid out symmetrically. The same capacitor unit element is used, leading to higher precision in the integrator gain and less capacitor mismatch. Furthermore, the surroundings of the unit capacitances are identical to ensure good matching.

The schematic of the measurement set-up is shown in Fig. 4.9. The die was packaged in a Quad Flat No-leads (QFN) package with exposed ground pad. A down-bond strategy is adopted to reduce the overall inductance in series with the ground pin, while decoupling capacitors are used to suppress noise interference. Local decoupling capacitors are used in power supplies and biasing sources. Different separate voltage supplies for the different parts of the modulator are adopted. Therefore, dedicated power supplies (V_{DD_A} and V_{SS_A} for the analog part and V_{DD_D} and V_{SS_D} for the digital part), each one with their bonding pad and chip package pin. The single-bit output stream, D_{out}, of the modulator is captured by a Field Programmable Gate Arrays (FPGA) board, connected to the characterization board by means of digital isolators, and transferred to a PC for off-line processing. Printed Circuit Board (PCB) design strategies for the characterization board are discussed in Appendix A. To shield the chip from external interferences, the PCB is encapsulated in a metal-alloy box.

Fig. 4.10 shows the measured output spectrum of a 35-Hz sinusoid signal, while Fig. 4.11 shows the output spectrum with the inputs shorted through a 50-Ω resistor. Fig. 4.12 shows the measured SNR and SNDR Vs. the input signal amplitudes normalized by reference voltage. The peak SNR reaches 94-dB while the peak SNDR reaches 92.5-dB. The DR is 98-dB over a 250-Hz signal bandwidth. Fig. 4.13 shows

the measured SNR Vs. the input signal amplitudes normalized by reference voltage at different temperature. The maximum peak is obtained at −40°C, 94.6-dB, while the minimum is obtained at 100°C, 91-dB. Fig. 4.14 shows the measured SNDR Vs. the input signal amplitudes normalized by reference voltage at different temperature. The maximum peak is obtained at −40°C, 93-dB, while the minimum is obtained at 100°C, 85-dB. Fig. 4.15 shows the measured DR at different temperature. The maximum, obtained at −40°C is 99.5-dB, while the minimum, obtained at 100°C, is 97.6-dB. Tab. 4.2 gives the summary of the performance. The power consumption of the master bias circuit, presented in Sec. 4.2.4, is not included.

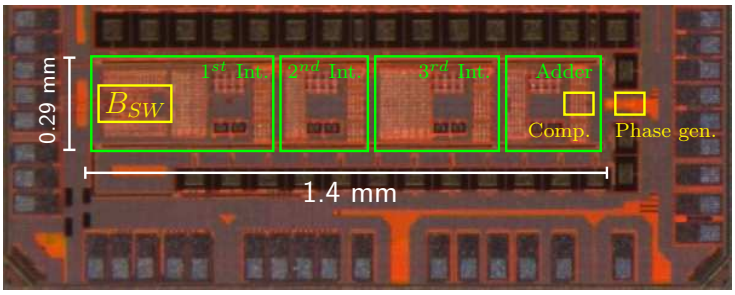


Figure 4.8: Chip micrograph.

4.3.1 Measurements on PSRR and CMRR

In the design of the third-order single-loop modulator, the PSRR of the modulator is of concern. The output stage of the op-amp in Fig. 4.1a, i.e. the transistor MP10, is directly connected to the power supply rail. Although the transistor MP10 is biased in strong inversion and the output impedance is high, thus the coupling from the analog supply to the output signal is minimized. There is a concern of coupling the disturbance on the supply rail to the gate of the transistor MP10, resulting into degradation of the PSRR. The measurement set-up is shown in Fig. 4.16a. The analog power supply is provided by a signal generator. A sinusoidal signal with a DC offset, V_{DD_A}, functions as the analog power supply of the modulator. In this way, a ripple on the analog supply is created. The frequency ripple of the power supply is fixed to 35-Hz

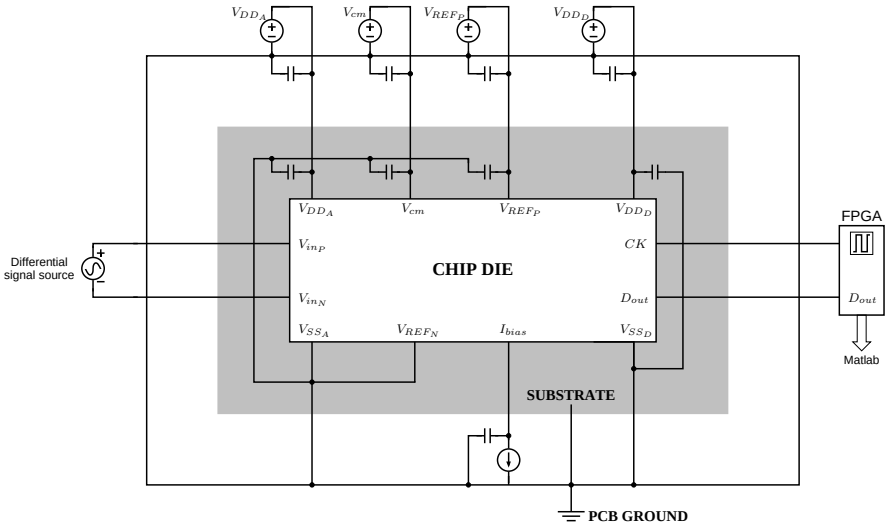


Figure 4.9: Schematic of the ΣΔM measurement set-up.

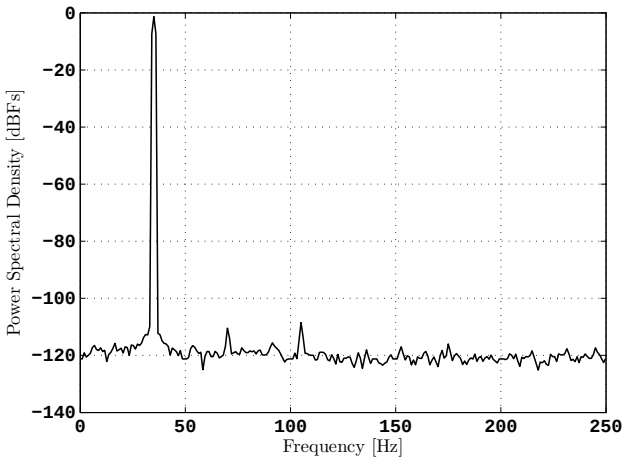


Figure 4.10: Measured output spectrum with a 35-Hz input signal (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

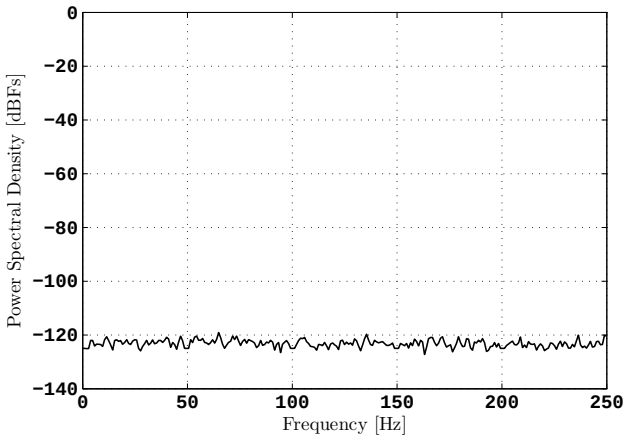


Figure 4.11: Modulator noise floor with the inputs closed on a 50-Ω resistor, no spurious tones are present. Obtained averaging 10 spectra. The DC component is removed.

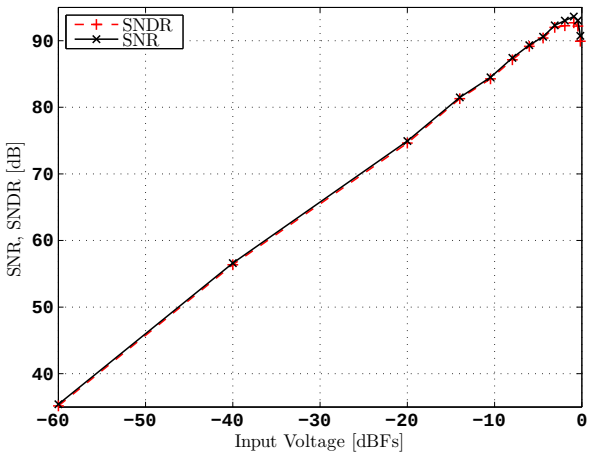


Figure 4.12: Measured SNR and SNDR Vs. input amplitude. Every point is obtained averaging 5 spectra.

with an amplitude of −20-dBFs. To measure the impact of the ripple on the analog supply to the performance of the modulator, a low frequency test signal is used to

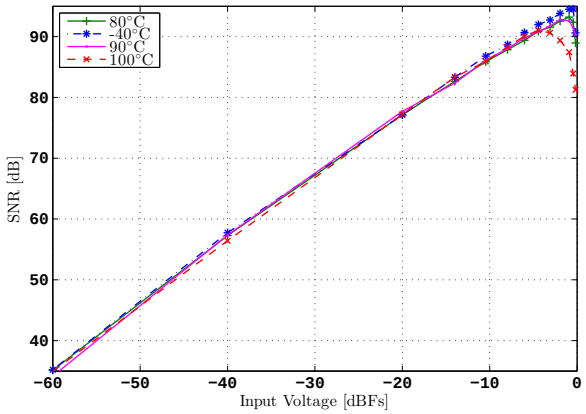


Figure 4.13: Measured SNR Vs. temperature. Every point is obtained averaging 5 spectra.

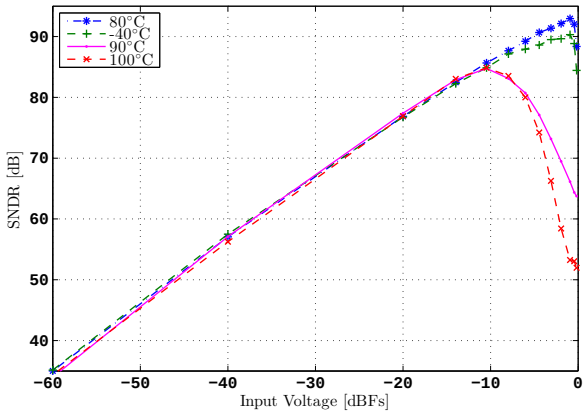


Figure 4.14: Measured SNDR Vs. temperature. Every point is obtained averaging 5 spectra.

reduce the attenuation from the off-chip decoupling capacitors [41]. Fig. 4.17 shows the measurement results, the measured PSRR is 76-dB at 35-Hz.

The test-bench set-up for the measurement of the CMRR is shown in Fig. 4.16b.

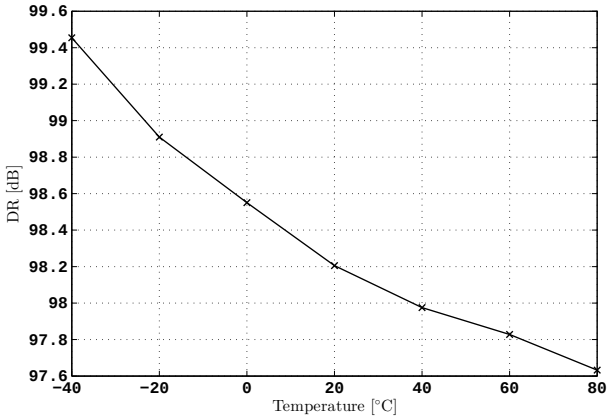
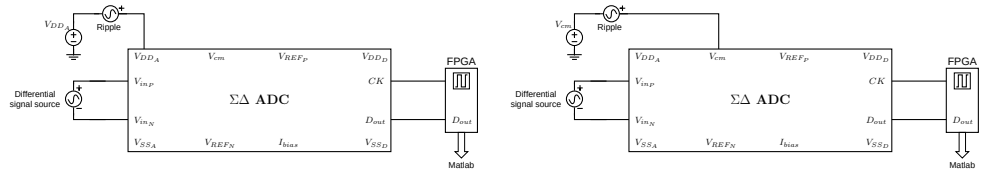


Figure 4.15: Measured DR Vs. temperature. Every point is obtained averaging 5 spectra.

Table 4.2: Measured performance summary.

Sampling frequency	250	kHz
Sampling bandwidth	250	Hz
Oversampling ratio	500	-
Supply voltage	1.2	V
Power consumption	50	μW
Peak SNR	94	dB
Peak SNDR	92.5	dB
Peak SFDR	107.2	dB
DR	98	dB
Active die area	0.4	mm^2
Technology	90-nm STM	-

As for the PSRR measurements, a sine-wave CM voltage is provided by a signal generator. A 35-Hz CM input sine-wave with an amplitude of −20-dBFs is used in the test. The CMRR can then be computed as the ratio between the power of the tone that appears at the output of the modulator in response to an input CM disturbance. Fig. 4.18 shows the measurement results, the measured CMRR is 83-dB at 35-Hz.



(a) (b)

Figure 4.16: Measurement circuit for: (a) PSRR, (b) CMRR.

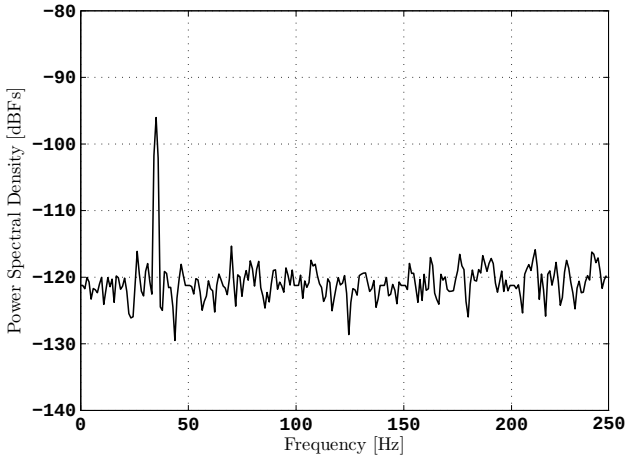


Figure 4.17: PSRR measured output spectrum with a 35-Hz sine-wave disturbance (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

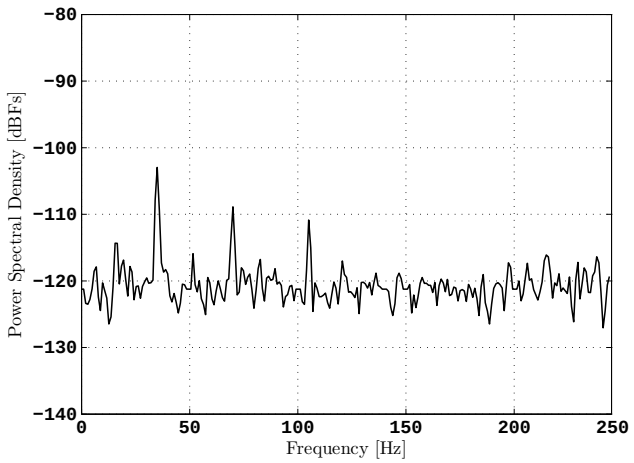


Figure 4.18: CMRR measured output spectrum with a 35-Hz sine-wave disturbance (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

4.3.2 Measurement on Low-Frequency Noise Floor

In the measurement results shown in Fig. 4.10, the low-frequency noise floor of the designed ΣΔM is not explicitly shown. On the other hand, the device noise, especially the $1/f$ noise, is mixed with the leakage (DC component removed in signal processing), making it difficult to measure the real circuit noise level. To reveal the low-frequency noise, more FFT points are taken to increase the FFT resolution. The result shown in Fig. 4.19 is derived. Using CDS technique, as discussed in Sec. 2.5.2, on the first integrator of the loop no $1/f$ noise is present in the output spectrum.

4.4 Decimation Filter

The digital signal produced by a ΣΔM, has a frequency equal to the Nyquist frequency multiplied by OSR, and must therefore needs to be downsampled. The modulator converter shapes the data in such a way as to allow high resolution by reducing low-frequency noise. Once the signal is converted in the digital domain, a LP digital filter

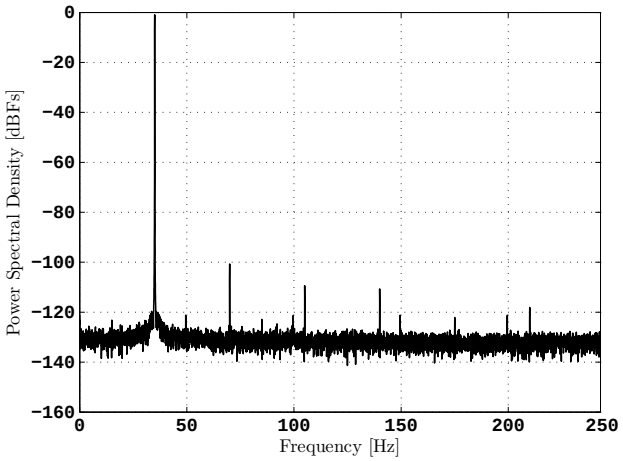


Figure 4.19: Measured output spectrum with a 35-Hz input signal (2^{24} FFT points). Obtained averaging 5 spectra. The DC component is removed.

is used to attenuate the high frequency noise, and a decimator filter function can be used to slow down the output-data rate. The designed decimation filter and results are discussed in Appendix B.

4.5 State-of-the-Art Comparison

In this Chapter a low-power low-voltage $\Sigma\Delta$ ADC design in nanometer CMOS is discussed. Then a low-power low-voltage SC $\Sigma\Delta$M implemented in a standard 90-nm CMOS technology is presented. By introducing low-power low-voltage building blocks at circuit level, high-performance $\Sigma\Delta$M in nanometer CMOS technologies is implemented. A gain enhancement technique is adopted in the op-amps to satisfy the distortion requirements of the modulator. The peak SNR reaches 94-dB and the DR is 98-dB over a 250-Hz signal bandwidth. The peak SFDR is 107.2-dB, limited by integrator gain non-linearity. The total power consumption is 50-μW with a 1.2-V power supply. The results have proven the feasibility of implementing high-performance $\Sigma\Delta$ ADCs in nanometer standard digital CMOS technologies. Measurements of the

PSRR, CMRR and low-frequency noise floor are also presented.

A comparison with other third-order ΣΔ at the state-of-the-art is reported in Tab. 4.3. The design have been selected according to their architecture characteristic: single-loop, single-bit quantizer and low-pass ΣΔMs. In all cases, the main features of each reported design are summarized in terms of the following performance metrics: f_B, OSR, supply voltage, CMOS technology process, power consumption (of the ΣΔM only), DR, peak SNDR and SNR. The efficiency of those proposed ΣΔMs are quantified by means of a ΣΔ FOM (1.13) [8].

Table 4.3: Performance Comparison.

Ref.	f_B [kHz]	OSR	Supply Voltage [V]	CMOS Tech.	Power [μW]	DR [dB]	Peak SNDR [dB]	Peak SNR [dB]	FOM [pJ/conv]
[40]	25	100	1	0.35-μm	950	88	85	87	0.88
[42]	20	100	1	90-nm	140	88	81	85	0.18
[43]	50	65	0.65	90-nm	27	65	59.5	61	0.19
This work, [15]	0.25	500	1.2	90-nm	50	98	92.5	94	1.5

Chapter 5

A 1.2-V, 30-μW, 96-dB DR $\Sigma\Delta$ Modulator in 90-nm CMOS

Any intelligent fool can make things bigger, more complex, and more violent. It takes a touch of genius - and a lot of courage - to move in the opposite direction.

– Ernst Friedrich Schumacher

To increase the number of effective bits by 1-bit, a 6-dB reduction of the noise is required, which means a factor four increase in capacitance. Since power scales linearly with the value of capacitance to charge, the power will also increase with a factor four. Thus, the $\Sigma\Delta$ FOM will become at least a factor 2 worse when the ENOB is increased by one. In this Chapter the design goal is to minimize power consumption without sacrificing resolution. Therefore, a class-AB op-amp is used. Moreover, architecture strategies are adopted in order to reduce the input referred thermal noise of the op-amp.

5.1 Op-amps

Sec. 5.1.1 considers a class-AB gain-enached op-amp with common gate cascode compensation. Sec. 5.1.2 proposes the same architecture, with the common gate embedded in the fist stage of the op-amp. This has a benefit in terms of input referred thermal noise, essential requirement in the front-end integrator.

5.1.1 Class-AB Op-amp with Common Gate Compensation

A two stage class-AB fully differential op-amp, shown in Fig. 5.1, with a pair of common gate stages, MP18 and MP19, to block the feedforward current through the compensation capacitors, C_c, is proposed [44], [45]. This architecture uses local positive feedback, to increase amplifier gain and GBW product. A class-AB operation implemented with the push-pull output stage, consisting of transistors MP11 and MP17, is preferred for power efficiency. A detailed small-signal analysis of this op-amp has been already reported [44]. This compensation scheme has the benefit, compared to a conventional Miller compensated op-amp, to achieve the same f_t with a smaller C_c, due to the multiplication effect obtained by $g_{m_{18-19}}$. The drawback of this op-amp is the presence of a mismatch between two current sources, MP20 and MP21, which increase the input referred noise of the op-amp due to the uncorrelated noise add at the output. The input referred noise of the op-amp can be approximated to:

$$\overline{v_{n,in}^2} \approx 4kT\gamma \left(\frac{g_{m_3}}{g_{m_5} - g_{m_7}} \right)^2 \cdot \left[g_{m_3} + g_{m_7} + g_{m_{21}} + g_{m_9} \left(g_{m_9} \cdot \frac{r_{ds_{11}} r_{ds_{17}}}{r_{ds_{11}} + r_{ds_{17}}} \right)^2 \right] \quad (5.1)$$

where T is the absolute temperature, k is the Boltzmann constant and γ is a unitless constant derived to be equal to $2/3$ for long channel transistors and may need to be replaced by a larger value for sub-μm CMOS technologies [46].

In a low-power design, is not recommended to use current sources in weak-inversion region, because the absolute values of the currents become so small that the noise becomes exceedingly large. In addition it is well know that the velocity saturation effect reduces the channel thermal noise. This imposes device polarization in

strong inversion leading to higher power consumption. Generally speaking, the transistor reaches the maximum g_m/I_d ratio and low saturation voltage when it operates in the weak inversion region, hence the maximum power efficiency is achieved. To improve the noise performance of the op-amp, the solution is to move the common-gate devices in the first stage of the op-amp. In this case, there is no need of an additional noisy current sources for polarization. The proposed circuit is shown in Sec. 5.1.2.

Tab. 5.1 reports op-amps' performances (in typical case). The op-amp achieves an f_t of 2.2-MHz while driving a 2-pF load, value estimated with a transistor-level simulation, and exhibits 11-μW power consumption at a 1.2-V supply voltage. The PM is 71 degrees. The power consumption of the CMFB circuit is also included. The op-amp was sized (transistors' aspect ratio and bias current) over process, mismatch and temperature range (–40°C÷80°C). DC-gain (A_0), SR and input referred thermal noise, N_{op}, are obtained with the load corresponding to the integration phase. The unity-gain-transition frequency, f_t, and PM are obtained in feedback configuration (i.e. integrator's loop gain was considered). The required compensation capacitor C_c is about 0.8-pF.

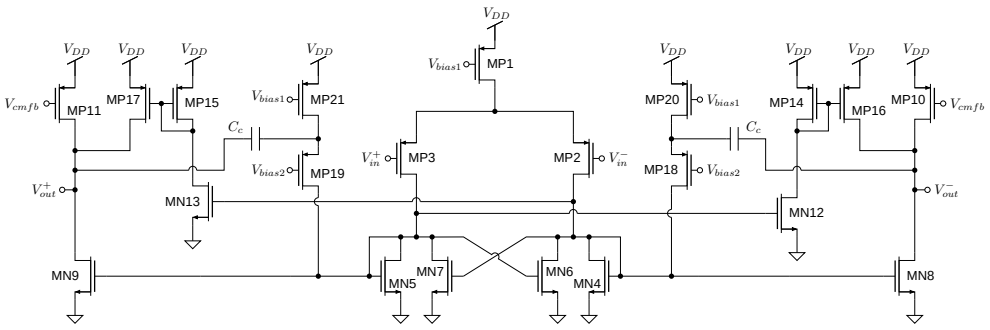


Figure 5.1: Schematic of the class-AB op-amp.

Table 5.1: Summary of the common gate op-amp compensated spec.s.

Metric	Value	Unit
A_0	55	dB
SR	1.85	V/μs
N_{op}	60	nV/$\sqrt{\text{Hz}}$
f_t	2.2	MHz
PM	71	deg.

5.1.2 Class-AB Op-amp with Embedded Common Gate Compensation in the First Stage

As mentioned in Sec. 5.1.1, the idea is to move the common-gate devices in the first stage of the op-amp [47]. The circuit is shown in Fig. 5.2. Since the gates of cascode devices, MP19 and MP20, are no longer at AC ground due to the presence of the active feedback loop, an extra pole and LHP zero are introduced by the feedback op-amp, *OA*, respect to the op-amp in Fig. 5.2. The idea is to boost the transconductance of cascode transistors, MP19 and MP20, by measuring their source voltages and regulating them at a constant value by controlling their gate voltages. The amplifier *OA*, with a DC-gain A_{OA}, increases the transconductance $g_{m_{19-20}}$ by a factor $(1+A_{OA})$. The input referred noise of the op-amp can be approximated to:

$$\overline{v_{n,in}^2} \approx 4kT\gamma \left(\frac{g_{m_3}}{g_{m_5} - g_{m_7}} \right)^2 \cdot \left[g_{m_3} + g_{m_7} + g_{m_9} \left(g_{m_9} \cdot \frac{r_{ds_{11}} r_{ds_{17}}}{r_{ds_{11}} + r_{ds_{17}}} \right)^2 \right] \tag{5.2}$$

The noise of the auxiliary op-amp *OA* negligibly contributes to the input noise of the op-amp, especially at low frequency. Indeed the impedance at node **C** is large, $1/(g_{m_{4,5}} - g_{m_{6,7}})$, due to the gain enhanced architecture. Model the output-referred noise of *OA*, at node **B** in Fig. 5.2, with a voltage source, the gain from the gate of MP19 and its drain **C** is low making negligible this noise source.

There are four transistors vertically stacked in the first stage of the op-amp. The

transistors biased in strong inversion region are: the current source MP1, the diode-connected MN4-5 and the cross diode-connected devices MN6-7. The polarization of MN4-5 and MN6-7 in strong inversion is strongly recommended to reduce the mismatch variation of their transconductance g_m, which can lead to latch condition for the op-amp with gain enhanced architecture. Furthermore, the increase of the gain of the first stage, due the presence of the cascode MP19, relaxes the equivalent resistance requirements of the gain enhanced architecture. The differential input pair MP2-3, are biased in moderate inversion region, e.g. $V_{GS} - V_T =$ 30-mV. This is a good trade-offs among speed, power and area. The common gate devices MP19-20 are biased in weak inversion region were transistor reaches the maximum g_m/I_d ratio.

The architecture used for *OA*, reported in Fig. 5.3a is differential. Moreover as will be demonstrated it is not necessary an high DC-gain, A_{OA}, for this amplifier. For this reason, in the output stage a pair of diodes MN23-24 are used as load for MP21-22, no CMFB circuit is need. A pair of source-followers MN25-26 are used as a level shifter at the input of the auxiliary op-amp. In this way the V_{ds} of the current source

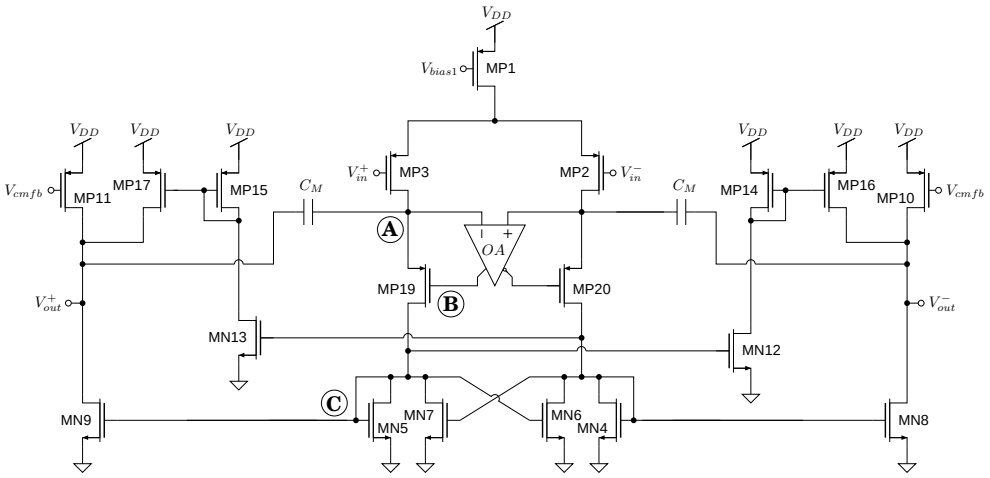
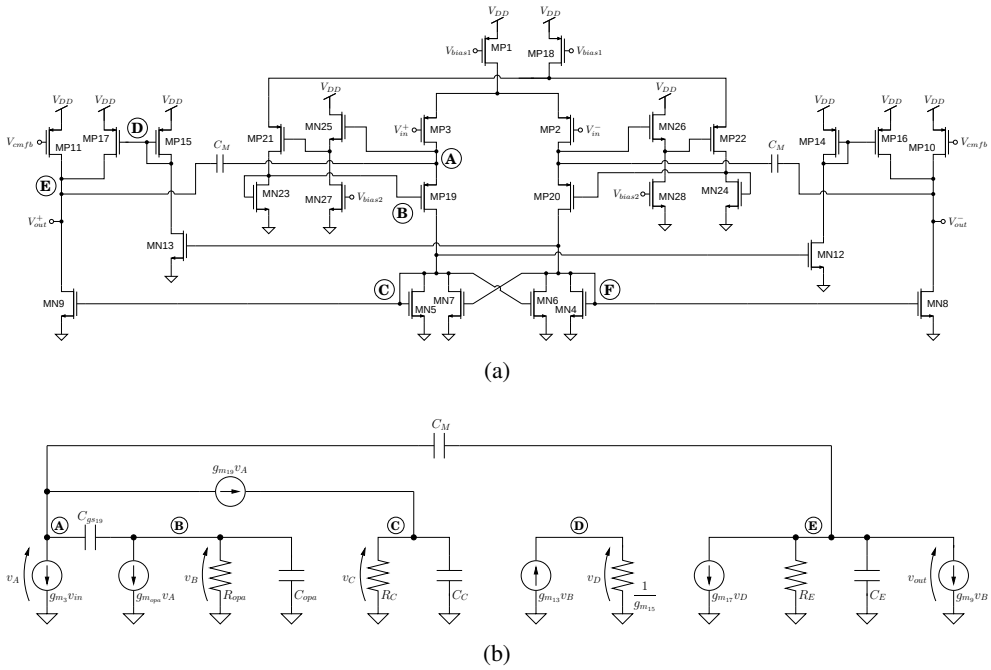


Figure 5.2: Schematic concept of a two-stage gain enhanced op-amp with MP19-20 as common gate transistor.



(a)

(b)

Figure 5.3: (a) Two-stage gain enhanced op-amp with each C_M connected to a common-gate transistor MP19-20. (b) Small-signal, half circuit.

of the auxiliary op-amp, MP18, is equal to:

$$V_{ds_{18}} = V_{DD} - \left(V_{gs_{23,24}} + V_{gs_{19,20}} - V_{gs_{25,26}} + V_{gs_{21,22}}\right) \tag{5.3}$$

with the benefit that the terms in the brackets are reduced by $V_{gs_{25,26}}$, this margin is important for keeping MP18 in saturation region over the temperature range.

A small-signal analysis of a half of the fully differential op-amp, Fig. 5.3b, is proposed. R_{opa} and C_{opa} model the impedance at node **B** for the circuit in Fig. 5.3a. R_C and C_C model the impedance at node **C**, finally R_E and C_E model the impedance

at node **E**. The approximate formulas are reported:

$$R_{opa} \approx \frac{1}{g_{m_{23}}} /\!/ r_{ds_{21}}, \tag{5.4a}$$

$$C_{opa} \approx C_{gs_{23}}, \tag{5.4b}$$

$$R_C \approx \frac{1}{g_{m_5} - g_{m_7}}, \tag{5.4c}$$

$$C_C \approx C_{gs_5} + C_{gs_6} + C_{gs_9} + C_{gs_{12}}, \tag{5.4d}$$

$$R_E \approx r_{ds_9} /\!/ \left(r_{ds_{11}} /\!/ r_{ds_{17}}\right), \tag{5.4e}$$

$$C_E \approx C_{db_9} + C_{LOAD}, \tag{5.4f}$$

C_{LOAD} in (5.4)f represents the external load of the circuit (i.e. the feedback capacitor of the first integrator) and dominates compared to C_{db_9}. The op-amp DC-gain, A_{DC}, is equal to:

$$A_{DC} = R_C R_E g_{m_3} g_{m_{19}} \cdot \left(1 + \frac{g_{m_{13}} g_{m_{17}}}{g_{m_{15}} g_{m_{19}}}\right) \tag{5.5}$$

The op-amp voltage gain exhibits three zeroes and four poles. The zero doublet, $z_{1,2}$, can be approximated as:

$$z_{1,2} \approx \sqrt{\frac{g_{m_{19}} \cdot (g_{m_9} g_{m_{15}} + g_{m_{13}} g_{m_{17}})}{C_M C_C g_{m_{15}}}} \tag{5.6}$$

The third zero, z_3, is at high frequency and is equal to:

$$z_3 \approx -\frac{1}{R_{opa} \cdot (C_{opa} + C_{gs_{19}})} \tag{5.7}$$

The op-amp gain has also four poles. The first, p_1 is:

$$p_1 \approx -\frac{g_{m_{15}}}{C_M R_C R_E \cdot (g_{m_9} g_{m_{15}} + g_{m_{13}} g_{m_{17}})} \tag{5.8}$$

In general poles p_2 and p_3 could be real or complex conjugate, depending on the bias conditions. In this case if the parasitic capacitor C_C is sufficiently high, as in this case due to the C_{gs} of MN5-6-9-12, the approximation $|p_1| \ll |p_2|$ and $|p_2| < |p_3|$ is

still longer valid and the poles p_2 and p_3 must be assumed as real. The approximated formulas are found:

$$p_2 \approx -\frac{R_E\, g_{m_{19}} \cdot (g_{m_9}\, g_{m_{15}} + g_{m_{13}}\, g_{m_{17}})}{C_C \cdot (g_{m_{15}} + R_Y\, g_{m_{15}}\, g_{m_{19}})} \tag{5.9}$$

$$p_3 \approx -\frac{g_{m_{19}}}{C_{gs_{19}} + C_E + g_{m_{19}}\, R_{opa} \cdot (C_{opa} + C_{gs_{19}})} \tag{5.10}$$

The forth pole is located at higher frequency, $|p_3| \ll |p_4|$, and is equal to:

$$p_4 \approx -\frac{C_{gs_{19}} + C_E + R_{opa}\, g_{m_{19}} \cdot (C_{opa} + C_{gs_{19}})}{C_E\, R_{opa} \cdot (C_{opa} + C_{gs_{19}})} \tag{5.11}$$

The doublet $z_{1,2}$, influences the poles of the voltage gain in feedback circuit configuration, while the zeroes doesn't change. Including the effect of the zeroes in the closed loop transfer function of the op-amp, with a feedback factor H_R, is mandatory for an accurate analysis. Considering $|p_4|$ and $|z_3|$ high compared to others poles and zeroes, the closed loop transfer function $A_{CL}(s)$ can be apporximated as in (5.12). The denominator exhibits three poles, two of them are complex conjugate and one is real. The approximate expression for the dominant complex conjugate poles is obtained, (5.13):

$$A_{CL}(s) = \frac{A_{DC} \cdot \left(1 - \dfrac{s^2}{z_{1,2}^2}\right)}{\left(1 - \dfrac{s}{p_1}\right) \cdot \left(1 - \dfrac{s}{p_2}\right) \cdot \left(1 - \dfrac{s}{p_3}\right) + H_R A_{DC} \cdot \left(1 - \dfrac{s^2}{z_{1,2}^2}\right)} \tag{5.12}$$

$$p^*_{1,2_{CL}} \approx -\frac{\alpha \cdot g_{m_{19}} + g_{m_9}\, g_{m_{15}}\, g_{m_{19}} \cdot \left(\sqrt{1 - \dfrac{\alpha \cdot 4\, C_C\, H_R\, g_{m_3} \cdot (g_{m_{19}} - H_R\, g_{m_3})}{C_M\, g_{m_{15}}\, g_{m_{19}}\, g_{m_9}^2}}\right)}{2\, C_C\, g_{m_{15}} \cdot (g_{m_{19}} - H_R\, g_{m_3})} \tag{5.13}$$

where α is equal to:

$$\alpha = (g_{m_9} g_{m_{15}} + g_{m_{13}} g_{m_{17}}) \tag{5.14}$$

The poles are complex conjugate if the terms under the square root satisfied, as in this case, the following condition:

$$\frac{C_M\, g_{m9}^2\, g_{m15}\, g_{m19}}{g_{m19} - H_R\, g_{m3}} < 4\, C_C\, H_R\, g_{m3} \cdot \alpha \tag{5.15}$$

Taking into account the effect of p_3 in (5.12), is necessary because p_2 and p_3 are not sufficiently spaced. But in closed loop, $|p^*_{1,2_{CL}}| \ll |p_{3_{CL}}|$ and the study of the stability can be reported to a second order system. Finally the damping factor, δ, and the natural frequency, ω_n, of the dominant pole, $p^*_{1,2_{CL}}$, are obtained:

$$\omega_n = |p^*_{1,2_{CL}}| \tag{5.16}$$

$$\delta = -\frac{\Re(p^*_{1,2_{CL}})}{|p^*_{1,2_{CL}}|} \tag{5.17}$$

The key point is to find the best amplification factor for $g_{m_{19}}$ and thus the voltage amplifier gain A_{OA}. Fig. 5.4 shows the time response to a unit step input, for the amplifier in feedback configuration, for three values of the parameter A_{OA}. $H_R = 0.5$ for the first integrator, c_1 in Tab. 2.1. The overshoot is maximum for $A_{OA} = 0.5$, in this case the settling time is not acceptable and the system is at bound of stability. While for $A_{OA} = 1$ and $A_{OA} = 5$ the overshoot is well controlled and the system response is good. The pole location for this three cases are reported in Fig. 5.5, the dotted lines represents the constant damping ratio and natural frequency in the S-plane. The damping factor, δ, as function of A_{OA} is reported in Fig. 5.6. For $A_{OA} < 0.75$ the approximations used to obtain (5.13) are no more valid, because poles p_2 and p_3 in open loop are close, while the (5.9) and (5.10) are obtained with the hypothesis $|p_2| < |p_3|$, in addition $p_{3_{CL}}$ is close to $p^*_{1,2_{CL}}$ and cannot be neglected. For $A_{OA} > 0.75$ the simulations of the approximated two pole system compared to the full system, without approximations, are in strictly good agreement and confirms the validity of the proposed approach. In this design A_{OA} is set equal to 1 for a faster settling.

Tab. 5.2 reports op-amps' performances (in typical case). The op-amp achieves an f_t of 1.8-MHz while driving a 2-pF load, C_L estimated with a transistor-level simulation, and consumes 15-μW power at a 1.2-V supply voltage. The PM is 73 degrees.

The power consumption of the biasing and the CMFB circuits are also included in the result. The op-amp was sized (transistors' aspect ratio and bias current) over process, mismatch and temperature range (–40°C÷80°C). DC-gain (A_0), SR and input referred thermal noise, N_{op}, are obtained with the load corresponding to the integration phase. The unity-gain-transition frequency, f_t, and the PM are obtained in feedback configuration (integrator's loop gain). The required compensation capacitor C_M, in Fig. 5.3a, is about 2.3-pF.

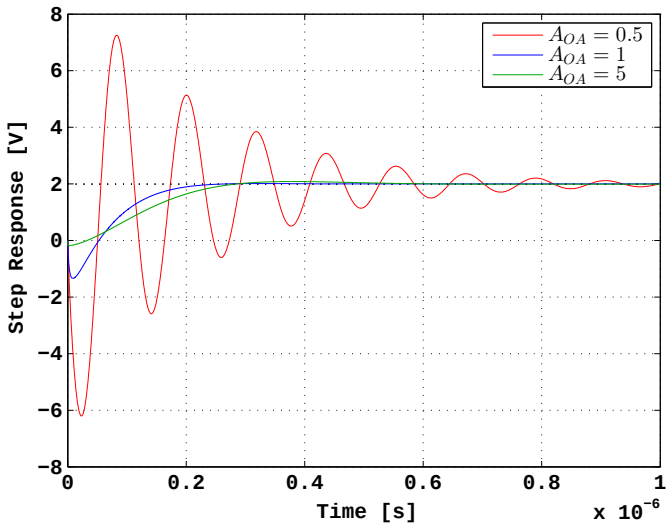


Figure 5.4: Step response.

5.2 Basic Building Blocks

The complete modulator circuit is shown in Fig. 5.7. It has three integrators with a latch comparator. The input CM voltage, V_{cm}, of the modulator is set to 0.5-V. The reference voltages, V_{ref_P} and V_{ref_N}, are set respectively to 1-V and 0-V (ground). The op-amp used in the first integrator is described in Sec. 5.1.1, while the op-amps used

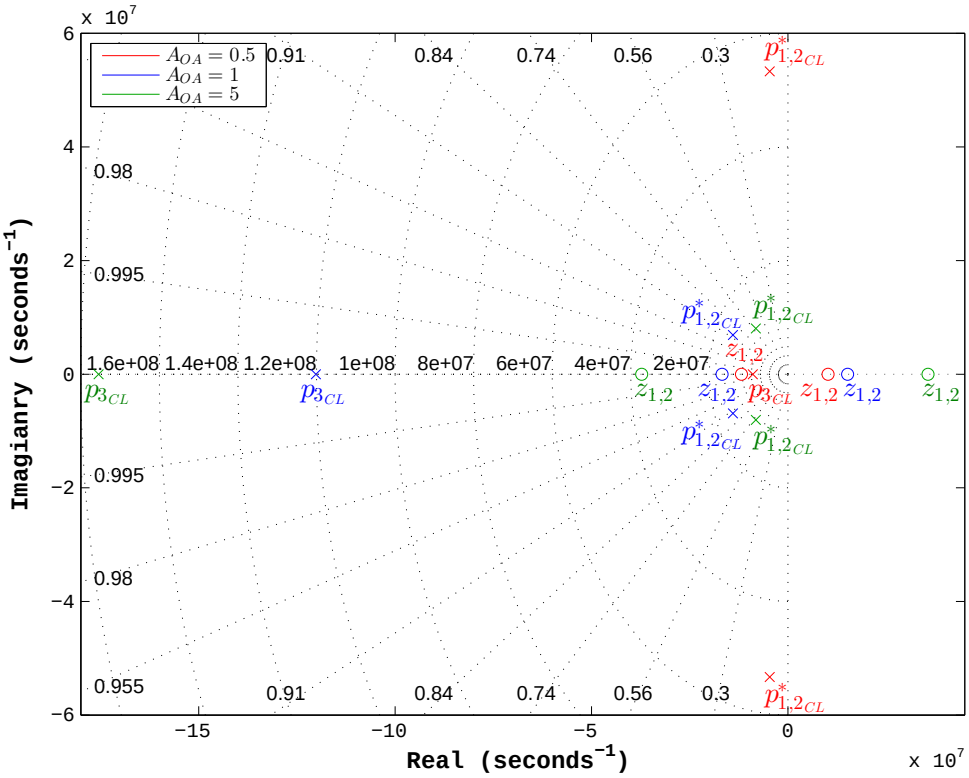


Figure 5.5: Poles and zeroes location for three different values of the auxiliary amplifier gain A_{OA}. $p^*_{1,2_{CL}}$ is the dominant complex conjugate pole, (5.13) for approximate formula. $p_{3_{CL}}$ is the third pole in closed loop configuration, for $A_{OA} = 0.5$ its effect is not negligible. $z_{1,2}$ is the zero doublet in open loop, it is not modified in closed loop.

in the second and third integrator are described in Sec. 5.1.2. The op-amp in the first integrator exhibits a power consumption of 15-μW. Thanks to the noise suppression inside the loop, the second and third integrator consume each one 7.5-μW, while the adder stage is passive. Furthermore, the other building blocks are the front-end input sampler described in Sec. 4.2.1, the one-bit quantizer described in Sec. 4.2.2 and the non-overlapping clock phase generator described in Sec. 4.2.3.

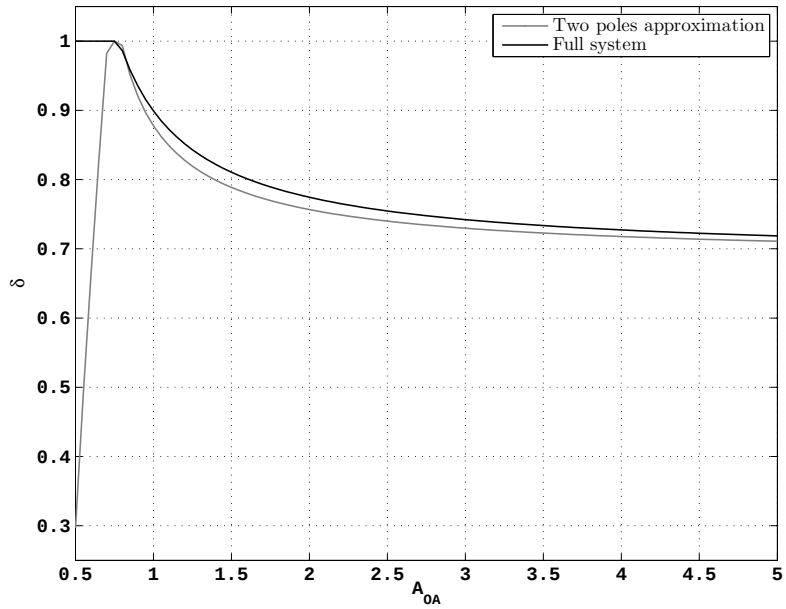


Figure 5.6: The damping factor, δ, as function of A_{OA}.

Table 5.2: Summary of the embedded common gate op-amp compensated spec.s.

Metric	**Value**	**Unit**
A_0	56	dB
SR	1.6	V/μs
N_{op}	31	nV/$\sqrt{\text{Hz}}$
f_t	1.8	MHz
PM	73	deg

5.3 Implementation and Measurement Results

The proposed modulator is implemented with a standard 90-nm STM CMOS technology. Standard MIM capacitors are used. The chip micrograph is shown in Fig. 5.8,

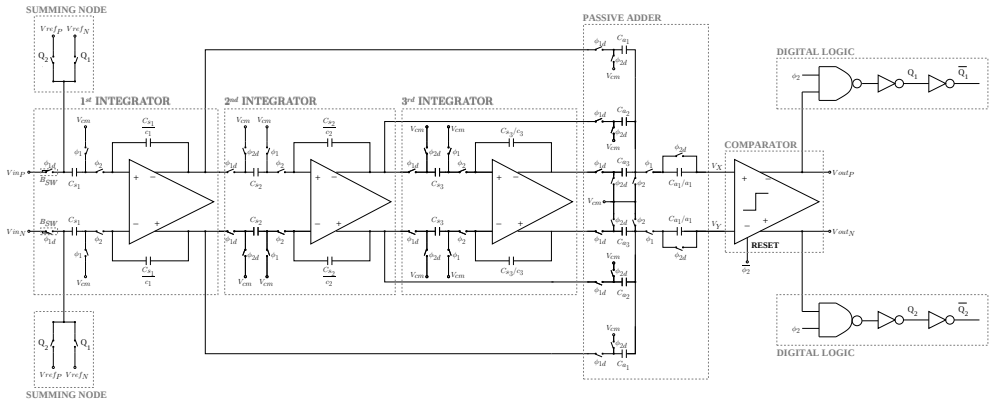


Figure 5.7: Schematic of the proposed third-order ΣΔM.

B_{SW} stands for the bootstrap switch. The chip core size is 0.29-mm×1.3-mm. The schematic of the measurement set-up is the same adopted for the modulator presented in Chapter 4, Fig. 4.9. The die was packaged in a QFN package with exposed ground pad. A down-bond strategy is adopted to reduce series inductance at ground pin, while decoupling capacitors are used to suppress supply bouncing. Local decoupling capacitors are used in power supplies and biasing sources. Separate supply voltages for the different parts of the modulator are adopted. The single-bit output stream of the modulator is captured by an FPGA board, connected to the characterization board by means of digital isolators, and transferred to a PC for off-line processing. PCB design strategies for the characterization board are discussed in Appendix A. To shield the chip from external interferences, the PCB is encapsulated in a metal-alloy box.

Fig. 5.9 shows the measured output spectrum of a 35-Hz sinusoid signal, while Fig. 5.10 shows the output spectrum with the inputs short-circuited to a 50-Ω resistor. Fig. 5.11 shows the measured SNR and SNDR Vs. the input signal amplitudes normalized by reference voltage. The peak SNR reaches 92-dB while the peak SNDR reaches 91-dB. The DR is 95.5-dB over a 250-Hz signal bandwidth. Fig. 5.12 shows the measured SNR Vs. the input signal amplitudes normalized by reference voltage at different temperature. The maximum peak is obtained at −40°C, 94.4-dB, while the minimum is obtained at 100°C, 90.8 -dB. Fig. 5.13 shows the measured SNDR Vs.

the input signal amplitudes normalized by reference voltage at different temperature. The maximum peak is obtained at −40°C, 93.4-dB, while the minimum is obtained at 100°C, 81.6-dB. Fig. 5.14 shows the measured DR at different temperature. The maximum, obtained at −40°C is 96.1-dB, while the minimum, obtained at 100°C, is 94.6-dB. Tab. 5.3 gives the summary of the performance. The power consumption of the master bias circuit, presented in Sec. 4.2.4, is not included.

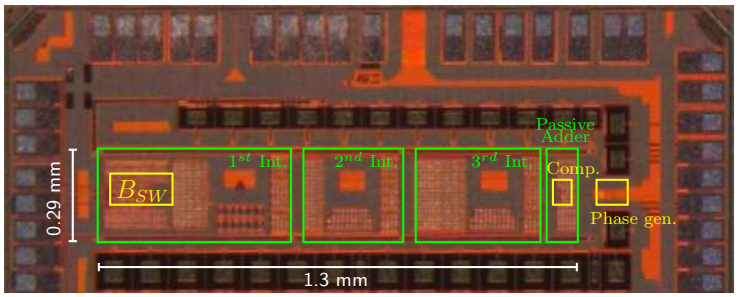


Figure 5.8: Chip micrograph.

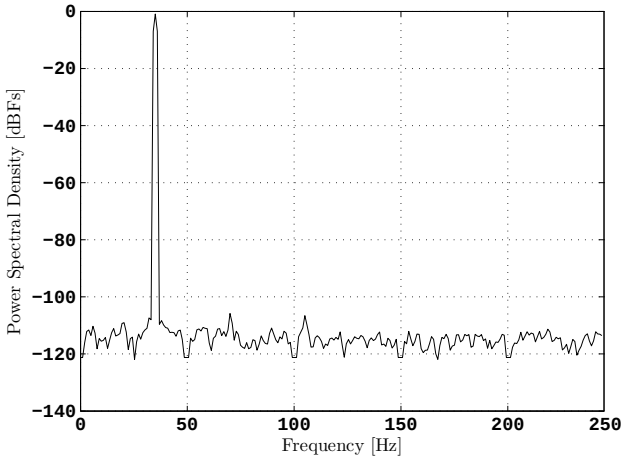


Figure 5.9: Measured output spectrum with a 35-Hz input signal (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

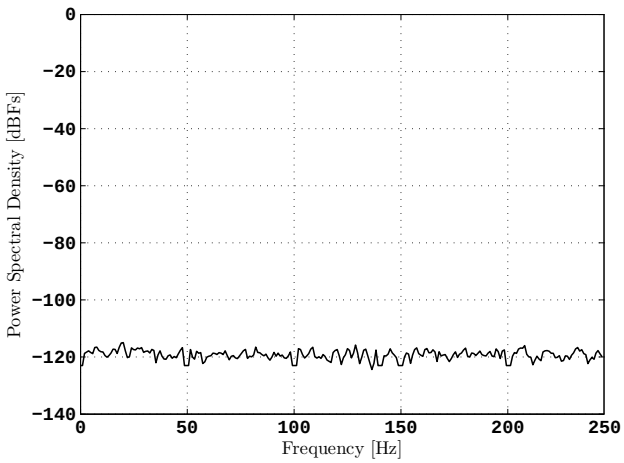


Figure 5.10: Modulator noise floor with the inputs closed on a 50-Ω resistor, no spurious tones are present. Obtained averaging 10 spectra. The DC component is removed.

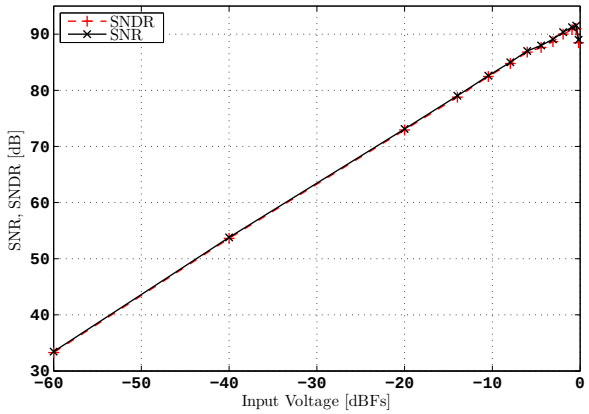


Figure 5.11: Measured SNR and SNDR Vs. input amplitude. Every point is obtained averaging 5 spectra.

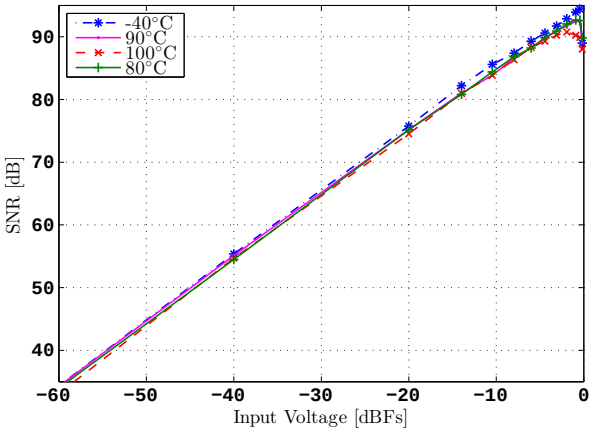


Figure 5.12: Measured SNR Vs. temperature. Every point is obtained averaging 5 spectra.

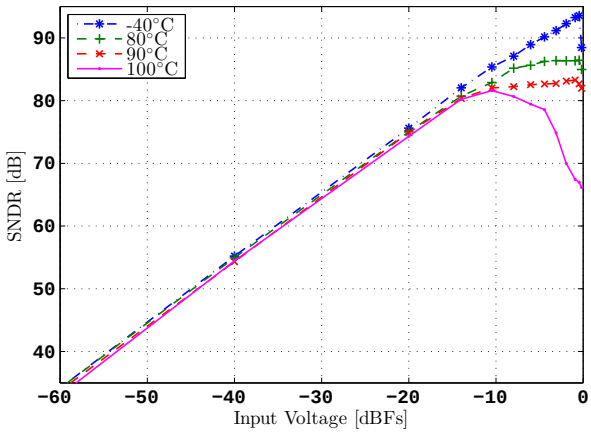


Figure 5.13: Measured SNDR Vs. temperature. Every point is obtained averaging 5 spectra.

5.3.1 Measurements on PSRR and CMRR

In the design of the third-order single-loop modulator, the PSRR of the modulator is of concern. Although the transistor MP10, Fig. 5.3, is biased in strong inversion and

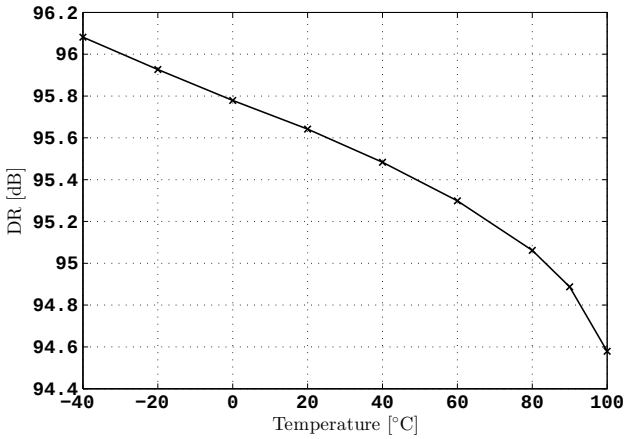


Figure 5.14: Measured DR Vs. temperature. Every point is obtained averaging 5 spectra. The DC component is removed.

the output impedance is high, thus a coupling from the analog supply to the output signal is present. Any disturbance on the supply rail my be transferred to the gate of the transistor MP10, resulting into degradation of the PSRR. The measurement set-up is shown in Fig. 4.16a. The analog power supply is provided by a signal generator. A sinusoidal signal with a DC offset, V_{DD_A}, functions as the analog power supply of the modulator. In this way, a ripple on the analog supply is intentionally introduced. The frequency ripple of the power supply is fixed to 35-Hz with an amplitude of −20-dBFs. To measure the impact of the ripple on the analog supply to the performance of the modulator, a low frequency test signal is used to reduce the attenuation from the off-chip decoupling capacitors [41]. Fig. 5.15 shows the measurement results, the measured PSRR is 76-dB at 35-Hz.

The test-bench set-up for measuring the CMRR is shown in Fig. 4.16b. As for the PSRR measurements, a sine-wave CM voltage is provided by a signal generator. A 35-Hz CM input sine-wave with an amplitude of −20-dBFs is used in the test. The CMRR can then be computed as the ratio between the power of the tone that appears at the output of the modulator in response to an input CM disturbance. Fig. 5.16

Table 5.3: Measured performance summary.

Sampling frequency	250	kHz
Sampling bandwidth	250	Hz
Oversampling ratio	500	-
Supply voltage	1.2	V
Power consumption	30	μW
Peak SNR	92	dB
Peak SNDR	91	dB
Peak SFDR	102.3	dB
DR	95.5	dB
Active die area	0.38	mm^2
Technology	90-nm STM	-

shows the measurement results, the measured CMRR is 58-dB at 35-Hz.

5.3.2 Measurement on Low-Frequency Noise Floor

In the measurement results shown in Fig. 5.9, the low-frequency noise floor of the designed $\Sigma\Delta$M is not explicitly shown. On the other hand, the device noise, especially the $1/f$ noise, is mixed with the leakage (DC component removed in signal processing), making it difficult to measure the real circuit noise level. To reveal the low-frequency noise, more FFT points are taken to increase the FFT resolution. The result shown in Fig. 5.17 is derived. Using CDS technique, as discussed in Sec. 2.5.2, on the first integrator of the loop no $1/f$ noise is present in the output spectrum.

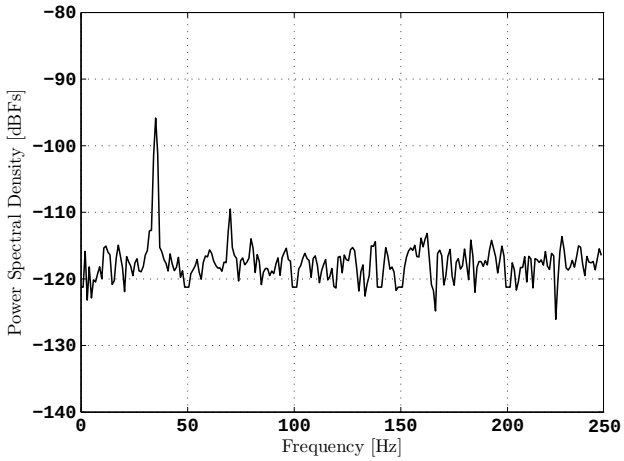


Figure 5.15: PSRR measured output spectrum with a 35-Hz sine-wave disturbance (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

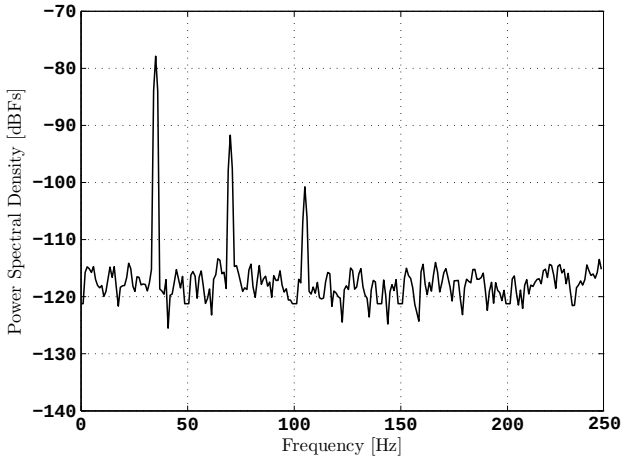


Figure 5.16: CMRR measured output spectrum with a 35-Hz sine-wave disturbance (2^{17} FFT points). Obtained averaging 5 spectra. The DC component is removed.

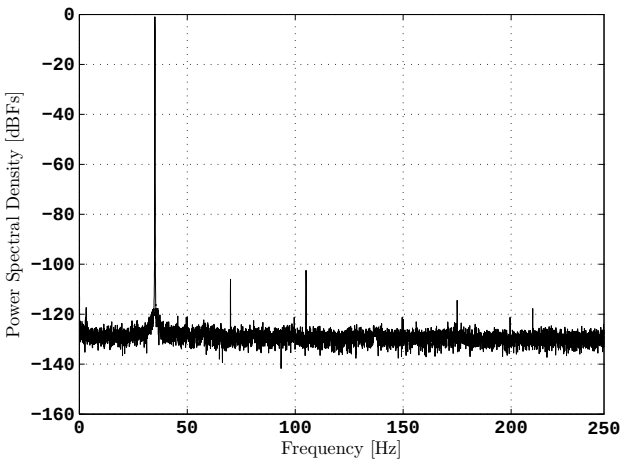


Figure 5.17: Measured output spectrum with a 35-Hz input signal (2^{24} FFT points). Obtained averaging 5 spectra. The DC component is removed.

5.4 State-of-the-Art Comparison

In this Chapter a low-power low-voltage $\Sigma\Delta$ ADC design in nanometer CMOS is discussed. Then a low-power low-voltage SC $\Sigma\Delta$M implemented in a standard 90-nm CMOS technology is presented. An op-amp with class-AB output stage and embedded common gate compensation is adopted to reduce the power consumption of the modulator. The peak SNR reaches 92-dB and the DR is 95.5-dB over a 250-Hz signal bandwidth. The peak SFDR is 102.3-dB, limited by integrator gain non-linearity. The total power consumption is 30-μW with a 1.2-V power supply. The results have proven the feasibility of implementing high-performance $\Sigma\Delta$ ADCs in nanometer standard digital CMOS technologies. Measurements of the PSRR, CMRR and low-frequency noise floor are also presented.

A comparison with other third-order $\Sigma\Delta$ at the state-of-the-art is reported in Tab. 5.4. The design have been selected according to their architecture characteristic: single-loop, single-bit quantizer and low-pass $\Sigma\Delta$Ms. In all cases, the main features of each reported design are summarized in terms of the following performance met-

rics: f_B, OSR, supply voltage, CMOS technology process, power consumption (of the ΣΔM only), DR, peak SNDR and SNR. The efficiency of those proposed ΣΔMs are quantified by means of a ΣΔ FOM (1.13) [8].

Table 5.4: Performance Comparison.

Ref.	f_B **[kHz]**	**OSR**	**Supply Voltage [V]**	**CMOS Tech.**	**Power [μW]**	**DR [dB]**	**Peak SNDR [dB]**	**Peak SNR [dB]**	**FOM [pJ/conv]**
[40]	25	100	1	0.35-μm	950	88	85	87	0.88
[42]	20	100	1	90-nm	140	88	81	85	0.18
[43]	50	65	0.65	90-nm	27	65	59.5	61	0.19
[15], Cap. 4	0.25	500	1.2	90-nm	50	98	92.5	94	1.5
This work	0.25	500	1.2	90-nm	30	95.5	91	92	1.2

Chapter 6

Conclusion

The important thing is not to stop questioning.

– Albert Einstein

This thesis has been focused on the design of ΣΔ architectures well suitable for low power applications. Two high-performance ΣΔMs have been proposed for sensor interface applications. The measurement results of the two prototypes have verified the effectiveness of the proposed behavioural model. Therefore, the main contributions of this thesis, presented in Chapter 3 and Chapter 5, are summarized.

6.1 Contribution of this Work

Oversampling ΣΔMs are used as key components in oversampled A/D and D/A converters. As the technology advances, current research on these circuits shows the potential of ΣΔ converters in high-speed and low-power interfaces for mixed-signal ICs. Although, transistor-level simulation is the most accurate approach known for these components this method becomes impractical for complex systems due to the long computational time. Consequently, device-level simulation in most cases is performed at the end of the design cycle as a final verification step. This situation has led

designers to consider behavioural modelling as an alternative technique being more time-efficient. The use of behavioural modelling provides to the designer the building blocks specifications for optimizing the power consumption at some converter SNR. Chapter 3 presents a comprehensive behavioural model for a ΣΔM implemented using Simulink. The model addresses proper representation of significant nonidealities such as the integrator dynamics, which are the main source of performance degradation in ΣΔM, due to the defective op-amp's settling, including:

- thermal noise of the integrator during sampling and integration phases;
- op-amp slew-rate limitations;
- op-amp input pair transconductance variation;
- op-amp static I/O characteristic;
- parasitic capacitive load of the integrator;

Moreover a two-pole op-amp model, that requires a higher level of knowledge and detail, provide a better approximation and description of the dynamics effects of the op-amp is proposed.

In Chapter 5, a new architecture of a class-AB op-amp with embedded common-gate compensation in the first stage has been presented. The small signal analysis takes into account the parasitic pole and zero of the auxiliary op-amp used to boost the transconductance of the common-gate cascode transistors. Moreover the impact of the auxiliary op-amp DC-gain over the settling of the op-amp in closed loop configuration is discussed. This op-amp architecture has been embedded in the low-power ΣΔM presented Chapter 5. The experimental results of the implemented ΣΔM support the analysis.

6.2 Future Work

Recently, there has been increasing demand of ADCs as sensor interfaces in portable systems. As a means of achieving high-resolution A/D conversion in a low-power

environment, ΣΔ modulation offers promise because of its limited analog circuit requirements. The proposed ΣΔM, designed in Chapter 5, provides a good starting point for a low-power design. The most substantial modifications will be needed in the op-amp design. Other circuit techniques, involved in the design of the op-amp could be exploited for further power saving. For example dynamic op-amp biasing [48], or instead of using an op-amp, an inverter-based SC circuit is applied to low-voltage, low-power ΣΔMs [49]. Finally, the pursuit of the proposed converter will eventually reach a point where the capabilities of the converter exceed those of the signal source by means of an increase power consumption.

Appendix A

PCB Design Considerations

PCB used for validating and testing data converters must be carefully designed to preserve the quality of the parameters being measured and to avoid false errors that hamper the results. The design of the interface board requires good design techniques such proper signal routing, decoupling, and grounding when measuring SNDR, SFDR and other dynamic features in data converters. The purpose of this Appendix, is to provide to the designer some practical layout recommendations to avoid errors in the PCB design that can totally mask the performance of the involved IC. The Appendix also discusses the layout of the evaluation board used in the experimental set-up of the two ΣΔ prototypes presented in Chapter 4 and Chapter 5.

A.1 Driving the Analog Inputs

Differential modes of operation provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion. A method for providing a differential signal to the converter input is to use a differential amplifier, such as the ADA4940-1. The ADA4940-1 can be used in applications where DC coupling is required and can be used as a single-ended-to-differential amplifier. The ADA4940-1 is as easy to use as an op-amp, and greatly simplifies differ-

ential signal amplification and driving. Fig. A.1 shows the typical application circuit of the ADA4940-1 [50], in a single-ended-to-differential amplifier configuration. The differential outputs of the ADA4940-1 helps balance the differential input signals of the ADC, maximizing its performance. The positive and negative outputs of the amplifier are connected to the respective inputs of the converter with a pair of LP filter with a cut-off frequency of 34-kHz. The ADA4940-1 has an output noise spectral density of 3.9-nV/$\sqrt{\text{Hz}}$ for the selected configuration. This noise is integrated over the filter bandwidth (2.12), this is 0.8-μV^2. This corresponds to an SNR due to the ADA4940-1 of 119-dB, which is more than 10-dB better than the SNR of the ADC presented in Chapter 4 and Chapter 5.

Another alternative method is to provide directly the differential signal at the inputs of the modulator by a low-noise and low-distortion Audio Precision signal generator [51]. The fundamental performance limits of an A/D converter will be reached only when the A/D conversion occurs directly at the signal source and the input signal is not processed through attenuation and gain stages. There are benefits at the PCB level. First, differential inputs have high CMRR to stray signals such as ground and power noise. Also, they provide good rejection to CM signals. This allow much improvement in performance of the tested IC performance. Measurement results reported in Chapter 4 and Chapter 5 are obtained with this method.

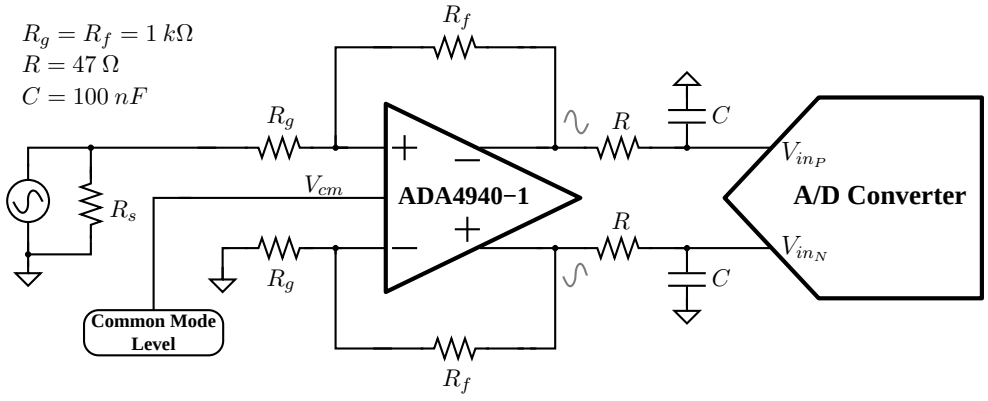


Figure A.1: Using the ADA4940-1 as a single-ended-to-differential amplifier.

A.2 Separating Analog and Digital Ground Planes

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. As shown in Fig. A.2, a simple 4-layer board would have internal ground and power plane layers with the outer two layers used for interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance with improved high frequency decoupling of the power supply [52]. In mixed-signal systems such data converters, it is highly desirable to physically separate sensitive analog components from noisy digital components. Separating power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. It may also be beneficial to use separate ground planes for the analog and the digital circuitry, Fig. A.3. With this approach, and using the digital isolator [53], all noisy digital currents are isolated from the sensitive analog section of the board.

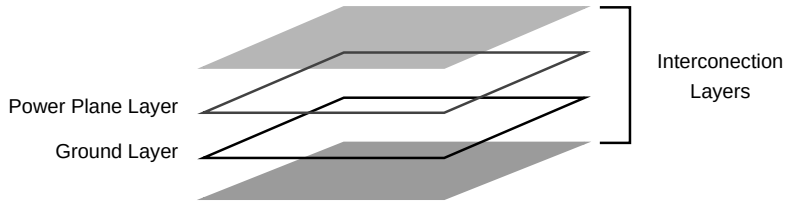


Figure A.2: Multilayer board. Conceptual 4-layer example.

A.3 Evaluation Board Layout

The main purpose of this Section is to show the layout of the multilayer evaluation board used for the experimental results of the two ΣΔ prototypes presented in Chapter 4 and Chapter 5. The PCB have been designed by following the practical recommendations described above. The top level of the evaluation board is shown in Fig. A.4a. The low-frequency clock signal is provided by the FPGA. The clock signal

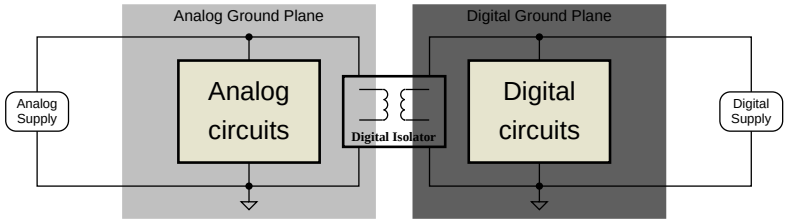
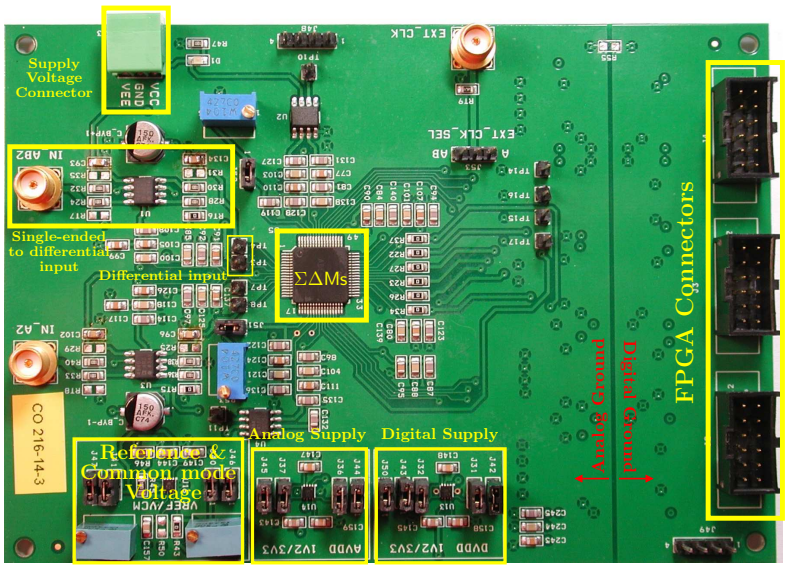
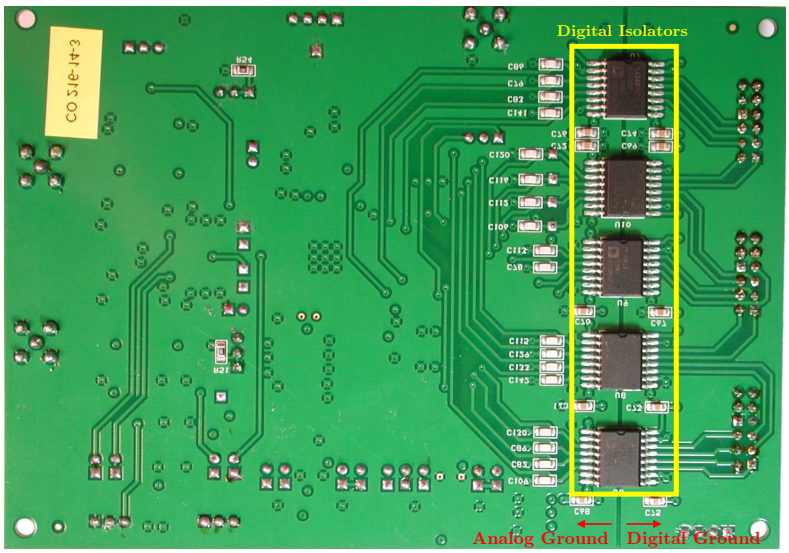


Figure A.3: Grounding mixed signal ICs at the PCB level: the analog ground and digital ground planes are separated by means of digital isolator.

as all controls signals from the FPGA to the analog part of the evaluation board are routed on the digital ground plane and well separated from the analog ground plane by means of digital isolators, Fig. A.4b. In the top layer, Fig. A.4a, there is the possibility of test the two ΣΔMs with differential or single-ended input signal, as explained in Section A.1.



(a)



(b)

Figure A.4: (a) PCB top signal level. (b) PCB bottom signal level.

Appendix B

Digital Filter

In ΣΔMs the digital decimation filter is essential part. This Appendix considers the design and implementation on FPGA of such a digital decimation filter [54]. The decimation filter attenuates the noise presented in the output spectrum of the ΣΔ and reduces the sample rate by OSR. A synthesizeable decimation filter for a given ΣΔ converter is presented. The decimation is done in two steps consisting of a filter followed by down-sampling. The filter is a LP filter that shall prevent aliasing. The down-sampling reduces the sampling rate by OSR[1]. The starting point in this work is the filter specifications. Then Matlab was used to design a model of the filter. The Matlab model and the hardware architecture was designed simultaneously, because some architectural decisions affects the Matlab model and vice-versa. The filter model created in Matlab is implemented in VHDL. Finally the VHDL model is synthesized on FPGA.

B.1 Filter Design

Due to the high decimation factor, the implementation of a monolithic filter increases the complexity. Then a three stage implementation, Fig. B.1, is adopted. The fre-

[1] In this design OSR=500. The reduction factor is set to the nearest power of two, 512. This implies a reduction of f_B from 250-Hz to 244-Hz.

quency of the single bit output stream of the ΣΔM is 250-kHz. Then down-sampled by 128 from the first stage and by 2 from the second and third stage respectively. The focus is on the design of the first stage, although the presence of a single-bit input reduces the complexity compared to a multi-bit input filter with the same order. Filters are usually classified between Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). IIR filters can only be realized by using recursive algorithms and FIR can be realized with a recursive or non recursive algorithm. The advantages of FIR over IIR filters are that they can have a linear phase response. They are always stable and easy to implement with poly-phase decomposition. On the other hand FIR filters require much higher filter order and introduce a large group delay. The pass/stop and transition band vary, Fig. B.2. The normalized signal band, represented in blue, extends from 0÷0.125, 0÷0.25 and 0÷0.5 respectively for the first, second and third stage. Due to the presence of the first spectral replica centred in 1, represented in red, the transition band of the third stage is no more relaxed. An in-band attenuation for the third filter must be accepted. For an SNR of about 100-dB, the attenuation value in stop-band, A_{att}, must be at least equal to −100-dB. The specifications of the filters are reported in Tab. B.1.

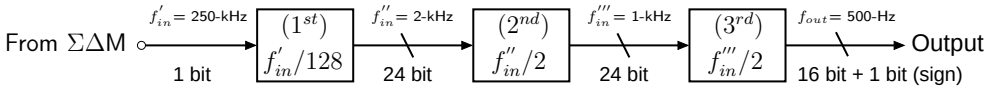


Figure B.1: Multi-stage decimation filter structure.

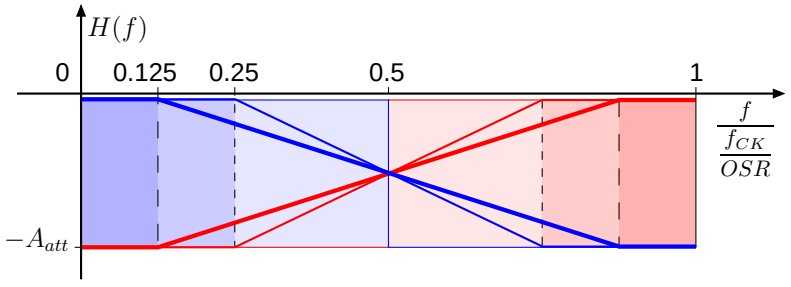


Figure B.2: Normalized filters bands. Signal band, blue, first spectral replica, red.

Filter	1^{st}	2^{nd}	3^{rd}
Type	FIR	FIR halfband	FIR halfband
Order	2048	30	90
Polyphase	direct	transposed	transposed
Rounding	Full precision	Nearest	Nearest

Table B.1: Decimation filters specifications.

B.1.1 First Stage

For the first stage the direct poly-phase architecture is considered, Fig. B.3. Due to the high order of the filter, reducing the complexity means reducing the number of the adders. Multipliers are not present because any coefficient multiplied by one bit is equal to itself or zero. Then a simple AND operation is sufficient. Distributed Arithmetic (DA) technique is adopted [55], [56]. The output, y, of a FIR filter is a linear combination between the N coefficients, $a_{1...N}$, and the last N samples at the input x.

$$y = \sum_{i=1}^{N} a_i \cdot x_i = \sum_{i=1}^{N} a_i \cdot \underbrace{\left[\sum_{k=1}^{W_d} x_{ik} \cdot 2^{-k} \right]}_{\text{binary encoding of } x_i} = \sum_{k=1}^{W_d} \underbrace{\left[\sum_{i=1}^{N} a_i \cdot x_{ik} \right]}_{F(x_{1k...Nk})} \cdot 2^{-k} \tag{B.1}$$

Where W_d is the bit-length of the samples x and x_i is a binary number. $F(x_{1k...Nk})$ can be implemented in a Look-Up Table (LUT) that stores for each address (the N bit $x_{1k...Nk}$) the result corresponding to the linear combination of N coefficients $a_{1...N}$. In this specific case, this technique has been applied to the sub-filter of each phase and the scheme just described is greatly simplified. In fact, $W_d = 1$ then $x_{ik} = x_i$ and $x_{1k...Nk} = x_{1...N}$:

$$y = \sum_{k=1}^{W_d} \left[\sum_{i=1}^{N} a_i \cdot x_{ik} \right] \cdot 2^{-k} = \sum_{i=1}^{N} a_i \cdot x_i = F(x_{1...N}) \tag{B.2}$$

$F(x_{1...N})$ of each phase already contains all its possible results. Therefore it is sufficient to direct the N bits stored in the flip-flops of that phase to the address decoder

of its LUT without further sums and/or translations. So 128 LUTs are used for replacing the adders. Since the symmetric impulse response (linear phase delay) of the filter, the first 64 LUTs are symmetrical with respect to the other 64 and then can be reused with the consequent halving of the complexity. This arrangement significantly reduces circuit complexity and allows the use of full-precision arithmetic without rounding.

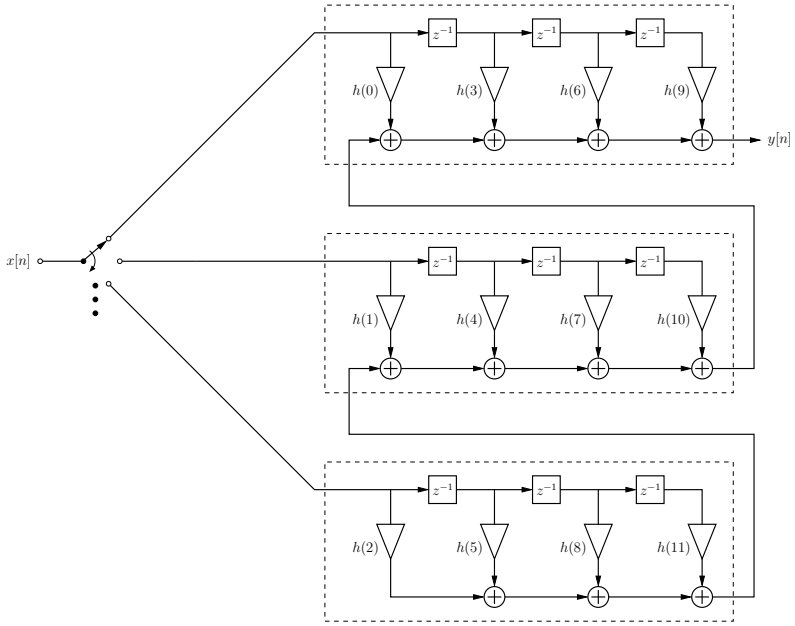


Figure B.3: Direct poly-phase architecture.

B.1.2 Second and Third Stage

To implement the second and third filter a transposed poly-phase architecture is used, Fig. B.4. The decimation factor for both filters is 2, this means that are half-band filters. A half-band filter with an impulse response $h(n)$ have the property that every odd filter tap in the impulse response will be zero:

$$h(2p+1) = 0 \tag{B.3}$$

In addition the impulse response is symmetrical then half of the required coefficients need to be implemented.

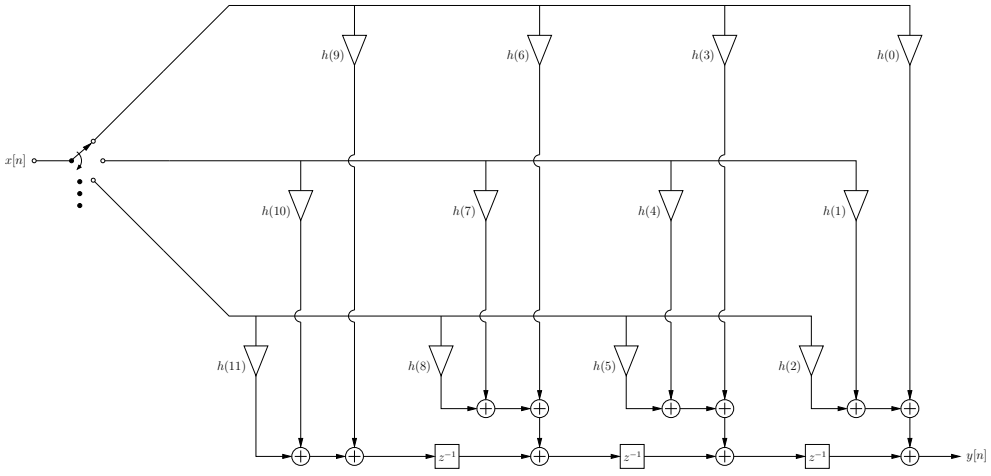


Figure B.4: Transposed poly-phase architecture.

B.2 Results

For Nyquist converters, Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) are used to measure the non-linearity of the I/O characteristic. These static parameters measure the accuracy of the conversion on a sample-by-sample basis. The output of an oversampling ΣΔ converter depends on its previous state, so the INL and DNL parameters are not meaningful. Instead, dynamic parameters such as the SNR and SNDR are used to characterize oversampling converters [57].

The histogram method to perform the code density test is frequently used [58]. A repetitive and dynamic signal with a bathtub distribution (e.g. sine-wave signal) is applied to the ADC, generating a corresponding distribution of digital codes at the output of the converter. For an ADC, given an analog input signal, the histogram shows how many times each different digital code word appears on the ADC output. Fig. B.5 shows the histogram of the ΣΔM described in Chapter 4. The black line

is the probability density function, of the sine-wave. The test is performed with a 7-Hz sinusoidal input signal with 0.95-V amplitude. This ΣΔM as that described in Chapter 5, achieve 16-bit resolution with no missing codes.

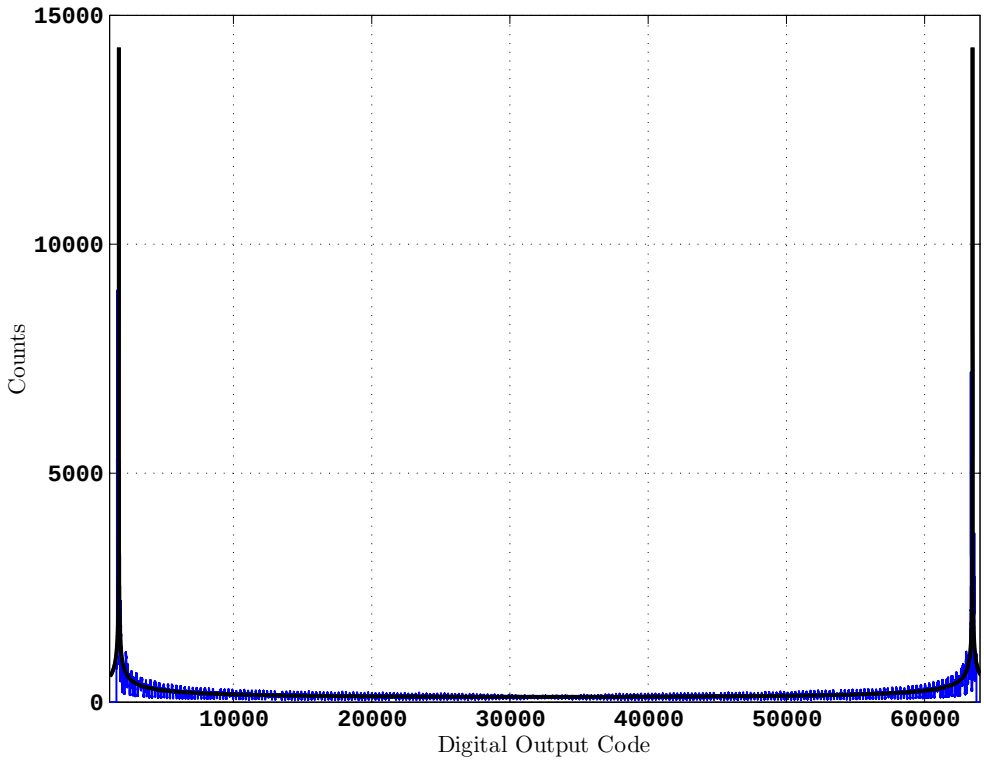


Figure B.5: Code histogram sine-wave.

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Patent pending

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Acknowledgements

The completion of this dissertation would not have been possible without the support and encouragement of many people, including colleagues, advisers and friends.

First and foremost, I wish to thank Professor Andrea Boni for his support and guidance. By allowing freedom in the course of my research while requiring significant and useful results. I also appreciate and have benefited greatly from his emphasis on producing quality publications.

This work was supported by STMicroelectronics for the fabrication of the experimental circuits described in this dissertation. I am grateful to Dr. Marco Ronchi of STMicroelectronics for the useful and fruitful discussions about the project and the technical support.

I wish to thank my Master Student Giorgio Pietrini for the contribution to my research, in particular in the behavioural modelling of the ΣΔ nonidealities.

Among my colleagues, Dr. Alessandro Magnanini deserves special recognition, his assistance was helpful in the initial phases of my research. I am also grateful to him and the other members of that research group, Dr. Matteo Tonelli and Dr. Marco Bigi, for my ”training” when I was a Master Student. Finally among my colleagues, the assistance of Dr. Andrea Ricci was essential in the FPGA set-up for the test of the two prototypes.

The author would like to thank Francisco Saia for the technical assistance in the debug of the evaluation PCB.

I wish Michele Caselli, new Ph.D. student in Microelectronics, a rewarding doctorate in the energy harvesting field.

I want to thank the people to whom I dedicated my thesis for their guidance, support, love and enthusiasm. Without these things this thesis could not have been possible.

Luca Giuffredi
Parma, 2016