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H8 CONVERTER: A THREE-PHASE TRANSFORMERLESS INVERTER WITH REDUCED COMMON-MODE VOLTAGE

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Summary

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Introduction

Power electronic converters constitute a large group of circuits used for the conversion of electrical energy.

Among all the existing power electronics converters, the category of Voltage-Source Inverters (VSIs) is the most widespread in the world of research as well as in industry. VSIs are used for transforming a continuous input voltage (DC) into an alternating output voltage (AC), possibly controllable in amplitude and frequency. They have become widely used in all those applications where an adjustable DC-AC conversion is needed, such as motor drives, utility interfaces and power supplies. For home appliances single-phase AC is generally standard, while in industry three-phase systems are; higher phase orders are given much less diffusion, primarily for their greater complexity and cost.

The aim of this work is to present the development of a novel three-phase voltage-source inverter, therefore the discourse focuses the attention onto the world of three-phase VSIs, whereas different families of power converters in this respect have a marginal pertinence and are disregarded in this thesis.

Most VSIs control the electrical parameters of the low-frequency output voltage using semiconductor-based switches and by means of high-frequency pulses modulated so that, after being low-pass filtered, they resolve into the desired waveform. Over the years, following the evolution of solid-state technology, power electronics has dramatically developed, giving birth to new and always better semiconductor devices, namely, in order of appearance: thyristors, gate turn-off thyristors (GTOs), bipolar power transistors (BJTs), power MOS field effect transistors (MOSFETs) and

insulated gate bipolar transistors (IGBTs). Thanks to a long series of technological leaps, since the precursors of the 1950s, silicon-based power converters have witnessed a strong improvement in terms of performance, efficiency, flexibility and reduction of size and cost. Further developments were made in the last ten years with the introduction of wide band-gap semiconductors, like silicon carbide (SiC) and gallium nitride (GaN), that opened the way to new opportunity for research in power electronics.

In addition to the evolution of semiconductor technology, several topologies of VSIs have been introduced over the last decades and a wide variety of modulation techniques have been developed too. Overall, each solution presents different pros and cons, making difficult to spot a single winner under every aspect of interest.

In former times, but still today in some applications, DC-AC converters adopted an isolation transformer, either a low-frequency transformer at the AC side, or a high-frequency transformer at the DC side. However, the transformer produces additional losses and its adoption is not free from drawbacks, since it is generally heavy and bulky and it increases the overall cost of the systems. The last trend is to take out the insulation transformer, designing what is addressed as a transformerless converter. Unfortunately this is not a perfect solution either, since the lack of galvanic insulation, together with the poor common-mode voltage (CMV) characteristics typical of these systems, allows for the flow of leakage common-mode currents through common-mode impedance paths that exist between the converter and the load. In photovoltaic applications this effects the efficiency and the power quality. In motor drives, bearing failures, electro-magnetic interferences that cause inverter drive trip, or interference with other electronic equipment in the vicinity can happen. Inconveniences related to the CMV in transformerless converters represent such a significant aspect that a lot of research has been conducted over the years trying to remedy them both in the industry and in academia.

Also the modulation of the switching devices plays a relevant role in the converter performance. Among the several existing possibilities, the traditional Sinusoidal Pulse-Width Modulation (SPWM) is popularly accepted as a good trade-off between simplicity and effectiveness, whereas the Space-Vector PWM (SVPWM)

technique is somewhat complex, but it has been proved to give superior performance and it is expected to be increasingly diffused in future.

This work fits in this context, presenting an original topology called “H8” for a three-phase VSI, along with a dedicated SV modulation. The main purpose of the project is the realization af a transformerless inverter with top-of-the-line performance in terms of CMV reduction. For this reason most of the attention is given to CMV-related aspects.

The thesis is organized as follows:

- Chapter 1: introduces the theme of transformerless inverters and presents a survey on solutions oriented to the CMV reduction.
- Chapter 2: explains the main aspects of transformerless inverters employment in PV applications and motor drives.
- Chapter 3: focuses on modulation, exposing the functioning principles of Sinusoidal and Space Vector PWM. It also provides a survey of the most relevant techniques that reduce CMV.
- Chapter 4: exposes architecture and modulation of the H8 inverter and offers comparisons to a classical VSI with the support of simulation results.
- Chapter 5: first explains the experimental setup with focus on the realized prototype, then it shows experimental results.
- Conclusions: delineate the contribution of this thesis resuming the main achievements of the work and propose future works to address still open issues.
- Appendix A: presents full schematics and PCB layout of the realized prototype.

Chapter 1

Overview on transformerless three-phase inverters

1.1 Introduction

In all practical applications, electrical systems are grounded for safety reasons. In the case of an inverter where a connection to ground is present on both the DC input and the AC output, a classical approach was to provide galvanic isolation along the conversion path by means of a transformer. It could be placed either in the DC-DC converter in the form of a high-frequency transformer (Fig. 1.2), or on the AC output side, in the form of a bulky low-frequency transformer (Fig. 1.3). Unfortunately these solutions are far from ideal, the former decreasing the efficiency and making the system more complex, the latter having a low-frequency transformer which considerably increases size and cost of the system [2].

A higher efficiency, smaller size and weight, and a lower price for the inverter are possible by omitting the isolation transformer. The classical transformerless architecture is depicted in Fig. 1.1. Of course the lack of any transformer brings to the lack of galvanic insulation between the DC source and the load and, as a consequence, to the lack of any sort of block for common-mode currents through common-mode impedance paths [3].

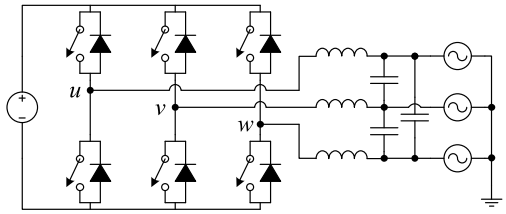


Figure 1.1: Transformerless inverter.

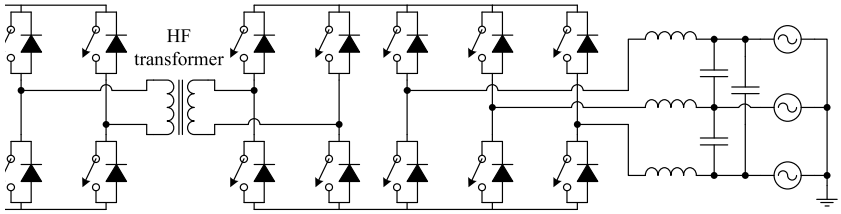


Figure 1.2: Inverter with high-frequency transformer.

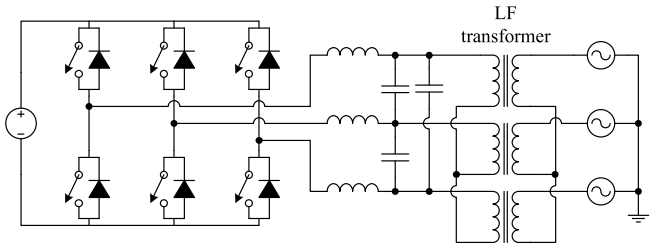


Figure 1.3: Inverter with line-frequency transformer.

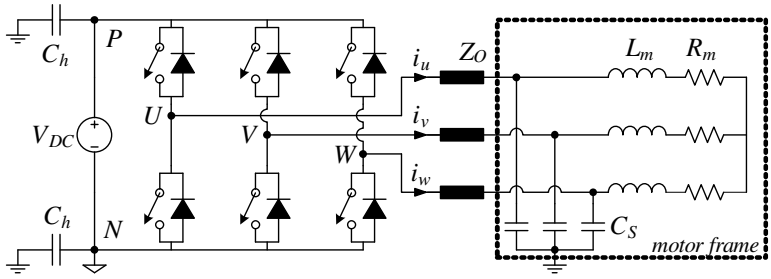


Figure 1.4: Transformerless drive with stray capacitances to ground.

1.2 Common-mode and differential-mode

This section describes a model for the common-mode and differential-mode of a standard inverter based on the three-phase bridge [4].

Fig. 1.4 shows a three-phase bridge drive powered by a DC source V_D. The stray capacitances C_h between the terminals of the DC link and ground, as well as those between the motor windings and the frame C_S, are shown to better clarify the existence of a common-mode path involving the inverter, those elements and the ground. For each output line, the impedance Z_O includes the inductive and resistive effects of the cable, while L_m and R_m represent those of the motor windings.

Assuming the negative side of the DC link N as the reference potential and naming the output ports of the inverter U, V and W, the output voltages of the three-phase bridge can be addressed as v_{UN}, v_{VN} and v_{WN}. The output common-mode voltage v_{cm} is defined as their arithmetic average:

$$v_{cm} = \frac{v_{UN} + v_{VN} + v_{WN}}{3} \tag{1.1}$$

Three-phase inverters can be modeled with differential- and common-mode equivalent circuits [4]. In this thesis the rectifier at the inverter input is not taken into account; instead, a DC voltage V_{DC} is here considered at the input port.

Switching states for each leg and for the whole bridge are expressed in (1.2) and

(1.3) respectively.

$$s_u, s_v, s_w = \begin{cases} 1 & \text{upper switch ON} \\ 0 & \text{lower switch ON} \end{cases} \tag{1.2}$$

$$S_{inv} = \begin{bmatrix} s_u & s_v & s_w \end{bmatrix} \tag{1.3}$$

The common-mode (CM) contribution X_C and the differential-mode (DM) components $X_{j,D}$, for each phase voltage or phase current X_j, can be expressed as in (1.4) and (1.5), where the subscript $j = u, v, w$ denotes each output phase.

$$X_C = \sum_{j=u,v,w} \frac{X_j}{3} \tag{1.4}$$

$$X_{j,D} = X_j - X_C \qquad \text{where} \sum_{j=u,v,w} X_{j,D} = 0 \tag{1.5}$$

From (1.4) and (1.5), the transformation matrix in (1.6) gives a comprehensive relationship between three-phase quantities and their CM and DM contributions.

$$\begin{bmatrix} X_{u,D} \\ X_{v,D} \\ X_{w,D} \\ X_C \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} X_u \\ X_v \\ X_w \end{bmatrix} \tag{1.6}$$

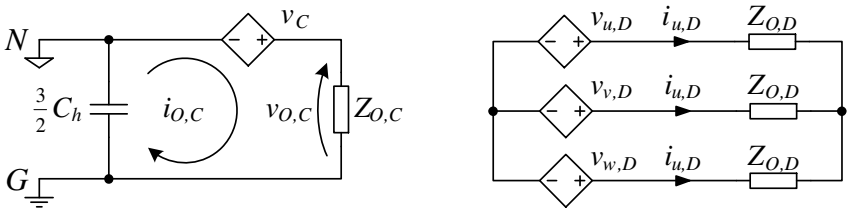
CM and DM equivalent circuits of the three-phase inverter are shown in 1.5, where voltage sources and impedances are given by (1.7-1.9).

$$v_C = \frac{s_u + s_v + s_w}{3} V_{DC} \tag{1.7}$$

$$v_{j,D} = \left(s_j - \frac{s_u + s_v + s_w}{3} \right) V_{DC} \qquad \text{for } j = u, v, w \tag{1.8}$$

$$Z_s = -\frac{j}{\omega C_S} \qquad Z_m = R_m + j\omega L_m \tag{1.9}$$

$$Z_{O,C} = Z_O + Z_S \qquad Z_{O,D} = Z_O + \frac{Z_S Z_m}{Z_S + Z_m} \tag{1.10}$$



(a) (b)

Figure 1.5: Common-mode (a) and differential-mode equivalent circuit (b).

1.3 Converter Architectures

This section reports a survey of the different solutions proposed by researchers over the last decades to address the problems of high-frequency common-mode voltage and common-mode leakage current. The majority of them are variations of the traditional three-phase bridge like that of Fig. 1.4, hereafter referred to as “H6” because of the six switches it is composed of.

1.3.1 Neutral-Point-Clamped inverter

The Neutral-Point-Clamped (NPC) inverter was proposed for the first time in 1981 by Nabae Takahashi and Akagi [5]; also, since the early 1980s, modulation techniques for NPC have been well developed. Since its introduction, several publications focused on this topology and a lot of variants with different number of voltage levels have been proposed. The most common version is that of Fig. 1.6.

The NPC converter offers benefits over the conventional two-level inverter especially in terms of efficiency, thanks to the series connections of the devices in each leg, which in turn reduce the voltage across each of them and therefore losses. Actually, in this regards the DC link voltage must be considered too: for smaller voltage levels, conduction losses are more relevant, whereas for higher voltages switching ones become predominant. NPCs are more efficient when high voltage systems are considered, because given the semiconductor technology, they exhibit less switching losses. Cross-even point depends on the technology. Furthermore, having more than

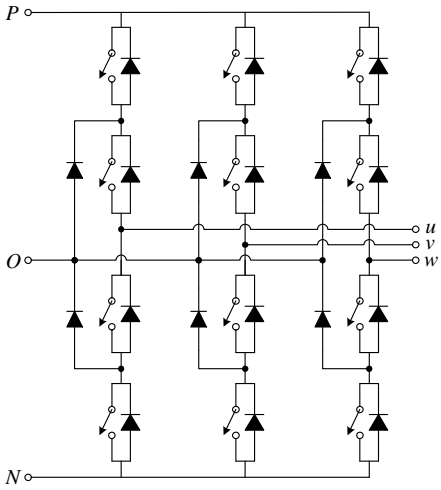


Figure 1.6: The Neutral Point Clamped inverter.

two voltage levels, this type of converter generates a lower harmonic distortion and lower current ripple, making it suitable for smaller output filters. In many works this architecture was adopted, both for single-phase and three-phase inverters [6].

The main drawback of NPC consists in the complexity: more devices and more driver circuitry are necessary compared to other architectures and the control turns out to be more complex as well. Also, unbalance voltage can arise in the DC link capacitors. If any current is injected into the neutral point O, a capacitor will be charged and the other will be discharged, with the consequence that the voltage applied to the output can become asymmetric. In order to cope with this problem, some countermeasures must be taken designing the modulation and the control system [6].

1.3.2 Impedance-source inverter

The impedance-source, or impedance-fed inverter, often abbreviated as Z-source inverter (ZSI), is derived from the full-bridge structure with the addition of an impedance network on the source side. This two-port network is made up of two inductive elements, which can either be a split inductor or two separate inductors, and a couple of capacitors connected in X shape, as shown in Fig. 1.7. The key feature of ZSI is

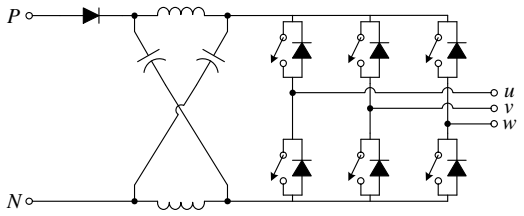


Figure 1.7: The Z-source inverter.

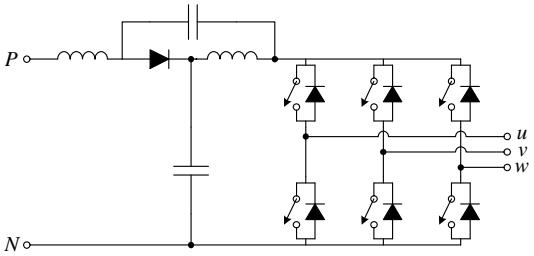


Figure 1.8: The Quasi-Z-source architecture.

that AC output can theoretically assume any value from zero to infinity regardless of the DC source voltage because the ZSI ultimately represent a buckboost inverter. It is also worth to be mentioned that this concept is suitable for all combinations of power conversions (DC/AC, AC/DC, AC/AC, and DC/DC), especially in applications where the input voltage changes widely. In addition, when compared to cascaded DC/DC plus DC/AC traditional converters, cost is reduced and efficiency increased since two conversion stages get incorporated into one same converter. In reality, it is suitable for boost ratio range up to 2, while for higher ratios the DC/DC boosted PWM inverter is the best configuration. Furthermore, the presence of a right-hand-plane zero limits the dynamic response and it cannot be eliminated by adjusting the Z-source parameters [7–10].

The Quasi-Z-source inverter, depicted in Fig. 1.8, represent a slightly modified topology of to the ZSI, exhibiting all the main advantages of the ZSI and even additional benefits such as a constant input current and less stress on components. Moreover, it is suitable for space vector modulation for minimizing the common-mode voltage [11].

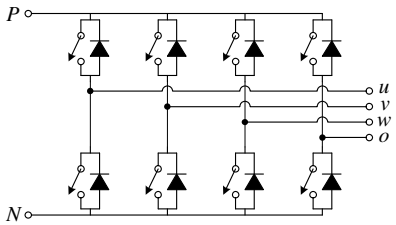


Figure 1.9: The four-legs inverter.

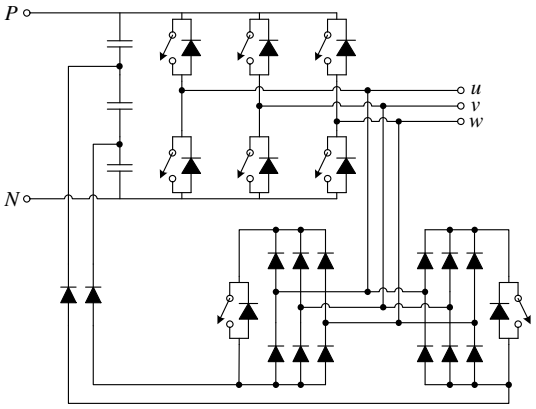


Figure 1.10: The two-levels three-phase PV inverter topology proposed in [1].

1.3.3 Other topologies

The CMV-related problems were addressed also with other approaches, here the most relevant alternative topologies are reported.

A four-legs inverter like that of Fig. 1.9, where a fourth leg is added to the H6 for controlling the CMV, adopting a specific modulation can reduce the average output voltage and the differential mode distortion [12].

The topology proposed in [1], represented in Fig. 1.10, reduces the CMV and the leakage current, but it has a great number of diodes and switches which increase switching and conduction losses with the immediate consequence that efficiency is lower than in conventional three-phase inverters.

In [13], the authors propose a solution where seven switches are present (shown

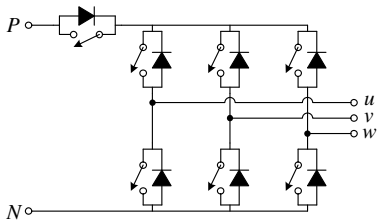


Figure 1.11: The H7 architecture.

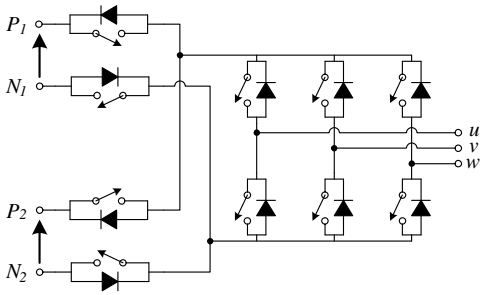


Figure 1.12: The DCM-232 inverter.

in Fig. 1.11), allowing to break the leakage current conduction path during the free-wheeling period. Moreover, this converter utilizes a reduced-common-mode-voltage modulation where the zero-voltage states are not used. However, it only focuses on leakage current elimination compromising issues such as voltage linearity, output current ripple, dc-link current ripple and harmonic distortion.

A topology called DCM-232 is depicted in Fig. 1.12. It makes use of ten switches, six for the H6 and four for a DC multiplexer with two DC sources (PV panels). Both of them are disconnected from the DC bus when the zero vectors are generated, so that the stray capacitance of the panels remains at a constant value and leakage current does not arise. The solution performs well in terms CMV and leakage current reduction, however it needs separate DC sources and it increases the complexity both of the hardware and of the control because of the presence of ten switches [14].

Chapter 2

Applications of transformerless inverters

Inverters find application in all those fields where a DC-AC conversion is needed. Three-phase architectures are generally preferred to single-phase for power ratings greater then about 5 kW. In this section a general-terms description is given for the two main inverter-based categories of electronics: photovoltaic (PV) systems, controllable motor drives.

Also, the main features typical converters (control of the current and filtering) are exposed in the followings.

2.1 Control of the current

In most of the applications, a controller is employed to track the current reference from either a MPPT block in PV system or the torque control in motor drives: it produces a value of duty cycle so to generate the desired current. The definition of an effective and reliable control scheme is of great importance. In this section, some of the most popular schemes for current controllers are presented.

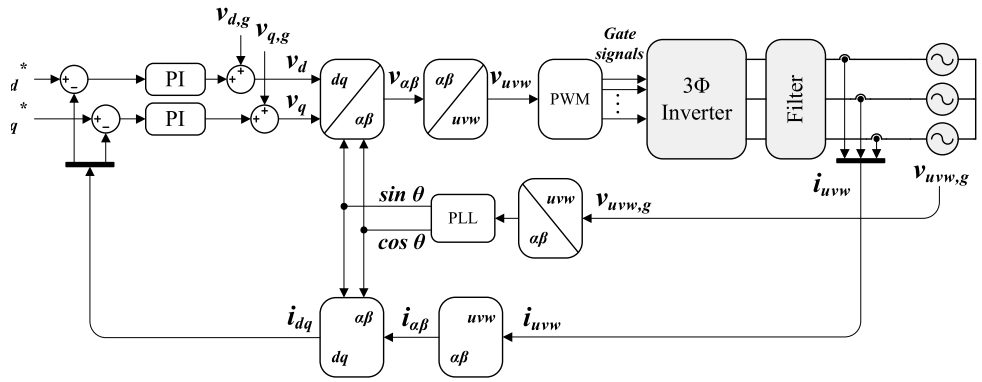


Figure 2.1: Block scheme of the current controller for a three-phase system adopting PI controllers in the synchronous reference frame.

Proportional Integral (PI) controllers

PI controllers are a simple solution and are often adopted. For a generic PI controller, with k_P and k_I as respectively proportional and integral coefficients, the transfer function is given in (2.1).

$$G_{PI}(s) = k_P + \frac{k_I}{s} \tag{2.1}$$

Because the PI controller is not able to track a sinusoidal reference without a steady-state error, the control scheme of Fig. 2.1 is adopted. It is based on the fact that balanced sinusoidal three-phase quantities turn in constant values when transformed in the dq synchronous frame. In normal working conditions reference values from the MPPT block can be considered constant, or varying with dynamics much slower then the converter output fundamental frequency. Therefore, with a PI for each of the two dq components, it is possible to perform the control of three-phase currents with zero steady-state error. In addition, dq feed-forward voltages are added in the control loops, counterbalancing the presence of the grid voltages at the inverter output.

Proportional Resonant (PR)

The Proportional Resonant (PR) controller is a second order controller with an infinite gain at a specific frequency. Its gain is given by (2.2), where ω_0 is the resonance frequency, while K_P and K_I are the proportional and integral coefficients.

$$G_{PR}(s) = K_P + K_I \frac{s}{s^2 + \omega_0^2} \tag{2.2}$$

However, because of the infinite gain at the resonance frequency, an ideal PR controller can suffer from instability. In an actual implementation, this must of course be avoided: some damping behavior must be introduced, making the PR controller non-ideal. The gain of a non-ideal PR controller is given by (2.3), where ω_c sets the bandwidth, thus the controller sensitivity towards variations of the grid frequency around the nominal ω_0, where the gain in now finite but still high enough for providing a relatively small steady-state error.

$$G_{PR}(s) = K_P + K_I \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{2.3}$$

Since the PR controller works in the stationary frame, without the need of any Park's transformation, it is also suitable for harmonic compensation by cascading several of them, each one tuned to the specific harmonic to be compensated, as shown in Fig. 2.2, where the ideal PR controller of equation (2.2) works in parallel with other resonant terms that compensate the 3rd, 5th and 7th harmonics.

Deadbeat controller

The deadbeat controller is a predictive controller, thus based on the model of the system where it is adopted. The model is used to foresee the behavior of the system, that is the evolution of the controlled quantities. In other terms, the equations that describe the relationships between the physical quantities and the switching states of the converter are used to determine the most effective switching events that will null the error in the shortest number of sampling periods. Provided a precise knowledge of the system parameters, theoretically the deadbeat controller has a very high

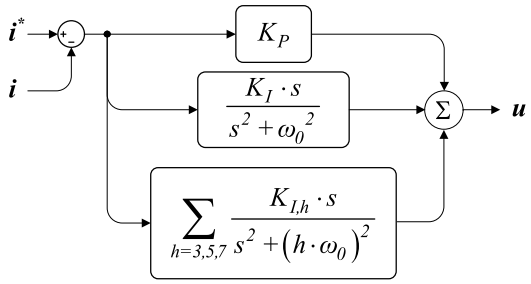
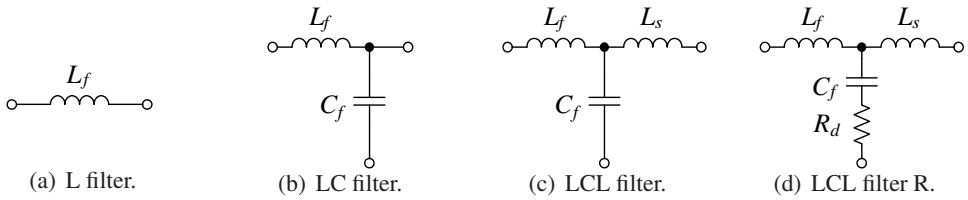


Figure 2.2: Block representation of the ideal PR controller. The bottom branch is for harmonic compensation of 3rd, 5th and 7th harmonics.

bandwidth, hence a sinusoidal signal can be tracked with a very little error. However, being a model-based controller, it is easily effected by parameters mismatches that may lead to considerable tracking errors or, in the worst cases, to stability problems.

2.2 Filtering

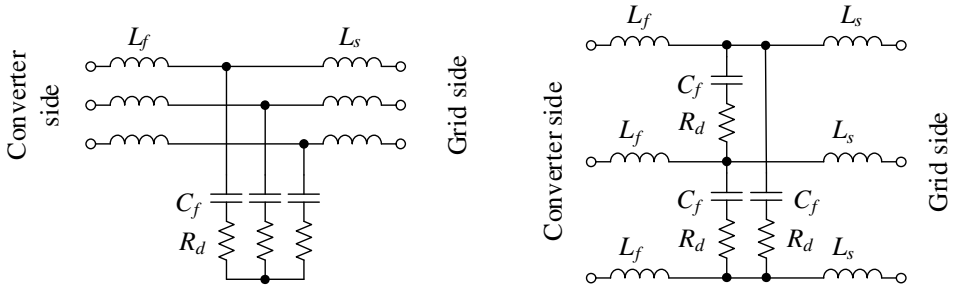
As already mentioned, voltage-source inverters synthesize the output voltage by some sort of modulation of high frequency pulses. In order to reduce the switching harmonics, an output low-pass filter must be employed. Output filters for grid-connected inverters and considerations related to their design have been deeply explored in literature [15]. In brief words, a grid filter made by a simple inductor is the simplest solution, but usually it does not give satisfying performance in term of harmonic reduction, even employing a large inductance value. For this reason, in most cases a LC or LCL filter are instead employed. Usually, a damping resistor R_d is also employed, keeping in mind the trade-off between damping and power losses, both increasing functions of R_d. In Fg. 2.3 the typical filter configurations (L, LC, LCL, $LCL + R_d$) are depicted. Filter parameters should be chosen so to limit the overall size of the reactive elements and the power losses connected to the passive damping elements (usually required to avoid resonance). First, inductors L_f must ensure a current ripple under the required one. Capacitors C_f are limited by the absorbed reactive power and they play a role in further limiting the current ripple. The LC resonance peak



(a) L filter. (b) LC filter. (c) LCL filter. (d) LCL filter R.

Figure 2.3: Typical filter configurations.

must be checked to end up in the range between ten times the grid frequency and half the switching frequency. More accurate design considerations can be found in many publications [16–18]. For the three-phase applications, the two mainly adopted topologies employ three $(C_f + R_d)$ series in a wye or delta connection, as those depicted in Fig. 2.4.



(a) $(C_f + R_d)$ in wye connection (b) $(C_f + R_d)$ in delta connection

Figure 2.4: Configurations of the three-phase LCL filter with damping resistors.

2.3 Photovoltaic systems

In the last decades, the demand for electrical power has increased, whilst the traditional non-renewable energy sources have diminished in stocks, thus causing a growing interest towards the generation from renewable power sources. Photovoltaic en-

ergy falls into this trend and PV systems have more and more integrated into the existing distribution grid [19].

The main classification of PV systems is between stand-alone or grid-connected. The former are suited for remote installations where the PV panels power a local load, while the latter work tied to the electrical grid. In a stand-alone system, the highly irregularity in the output of a PV field during a day requires some suitable electric energy storage, which however can only ensure limited accumulation and autonomy, in dependence with their size and operation conditions. This drawbacks do not arise in grid-connected systems, since the connection to the grid always allows to inject or consume power. The majority of PV systems are of this kind and research was mainly focused on this field. For these reasons, this chapter only considers grid-connected converters.

2.3.1 Control of a grid-connected photovoltaic converter

In Fig. 2.5 the general layout of a PV system is depicted. The PV panel represents a DC non linear supply feeding a DC-DC stage. This has two main functions: to step-up the DC voltage and to perform the Maximum Power Point Tracking (MPPT). The third and main stage consists of a three-phase voltage-source inverter (VSI), where the DC-AC conversion takes place. Because of the high-frequency contents of the voltages at the inverter output, they are then filtered, usually with a LCL filter, where ultimately takes place the connection to the grid. The control system performs the MPPT, the synchronization with the grid, the current control and the modulation of the inverter. The variables used to control the system are also shown. PV current i_{PV} and voltage v_{PV} and the DC-link voltage v_{DC} are necessary for MPPT. At the inverter output, current i_g and voltage v_g are used to perform the current control and the synchronization with the grid.

2.3.2 Synchronization to the grid

In the control of power converters connected to the electrical grid, the proper synchronization to the three-phase utility voltages is of fundamental importance. As usual, the

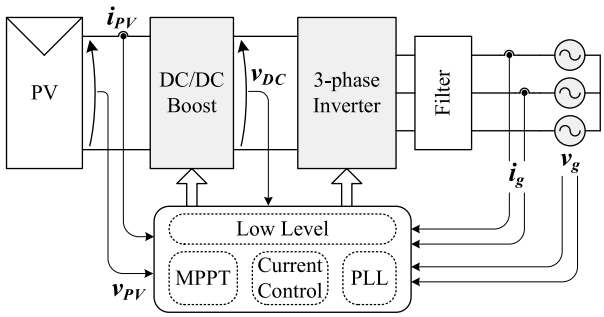


Figure 2.5: Block scheme of the control for a three-phase PV inverter.

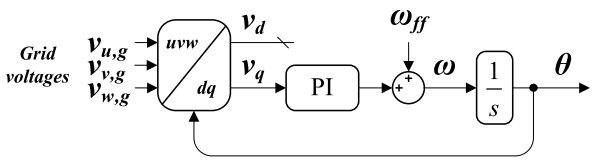


Figure 2.6: Block diagram of the PLL based on the synchronous reference frame.

three-phase voltages should be though as the components of a rotating vector. For balanced systems, its module and rotational speed do not change over a single period and the voltage vector describes a circular trajectory on the $\alpha\beta$ plane. The most extended technique used for frequency-insensitive grid synchronization in three-phase systems is the Phase-Locked Loop (PLL) based on the synchronous reference frame, where the angular position of the voltage vector is tracked regulating to zero, by a feedback loop, the quadrature component on the synchronous frame. Fig. 2.6 depicts the basic block diagram of this type of PLL. Here, three-phase grid voltages $(v_{u,g}, v_{v,g}, v_{w,g})$ are transformed into the dq components through the Clarke's and Park's transformations in cascade, then the PI controller acts for keeping $v_q \simeq 0$. Moreover, a feed-forward contribution to the frequency (ω_{ff}) is added to the PI output, helping the PLL to converge onto the grid frequency ω. Finally, the angle θ is obtained as integration of the frequency.

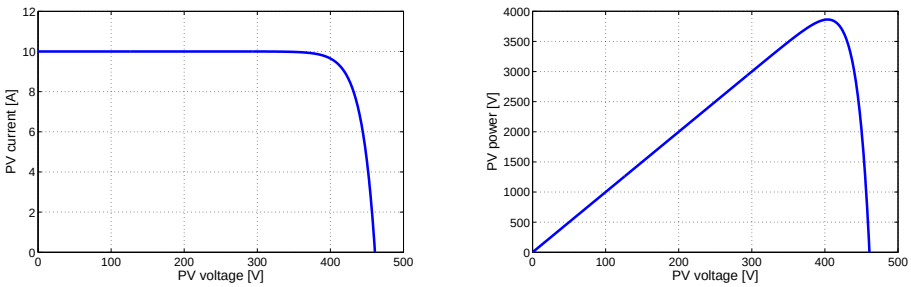


Figure 2.7: Voltage-Current characteristic and voltage-Power characteristics of a PV field.

2.3.3 Maximum Power Point Tracking

Maximum Power Point Tracking (MPPT) is a well known technique for optimally harvest energy from PV panels. The current-voltage characteristic of a silicon PV cell is given by (2.4), where I_{pv} is the photon-generated current, I_0 represent the cell reverse saturation current, $kT/q = 25.7\,\text{mV}$ at $25\,^{\circ}\text{C}$. Moreover, I_{pv} depends on the solar irradiance as stated by (2.5), where G is the light intensity in W/m^2 and $G_0 = 1000\,\text{W}/\text{m}^2$. The I-V curve for a typical 3.8 kW PV field is shown in Fig. 2.7(a).

$$I = I_{pv} - I_0\left(e^{qV/kT} - 1\right) \tag{2.4}$$

$$I_{pv} = I_{pv}(G_0)\frac{G}{G_0} \tag{2.5}$$

PV systems are of course influenced by external factors, primarily irradiation and temperature. Anyhow, given a certain combination of irradiation and temperature, the power delivered by a PV field versus the voltage follows a curve like that of Fig. 2.7(b).

For the best performance of the PV system, it is of fundamental importance to force the PV panels to work at their maximum power, i.e. at the voltage where the maximum of the power-voltage curve occurs. Since this continuously varies with irra-

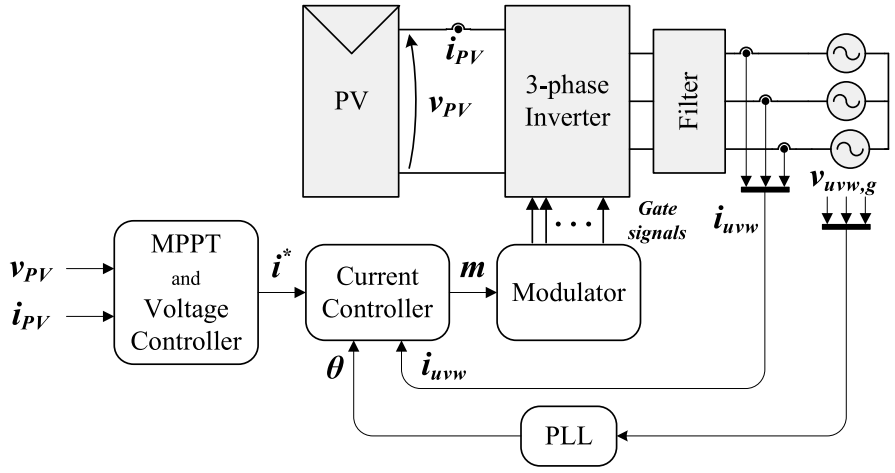


Figure 2.8: Block scheme of the control for a three-phase PV inverter.

diation and temperature changes, it becomes mandatory to track the maximum power point in real time. This is done by controlling the DC Link voltage (directly connected to the PV panel or field, depending on the installation) according to some algorithm that tries to track the maximum power point (MPP). In practice, the MPPT block is what determines the set-point of the current for the current control loop. Several MPPT algorithm can be found in literature. They can be mainly grouped into off-line and on-line methods. The first rely on the knowledge of the system parameters and on the off-line calculation of the optimum control law. On the contrary, off-line methods continuously try to track the MPP by perturbing the working point and observing the effects of the perturbation. In literature, several variants of this basic idea were investigated in order to obtain good MPPT performance, also with little steady-state oscillations, basically adapting the magnitude of the perturbation depending on the working condition itself.

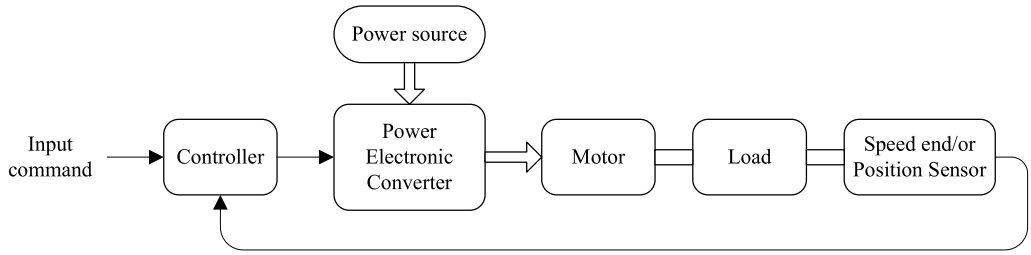


Figure 2.9: Block scheme of a drive system.

2.4 Motor Drives

A high-level scheme of a motion control system is depicted in Fig. 2.9. The energy flow between source and mechanical output is normally controlled by the combination of a power electronic converter, where the control of the energy flow actually occurs, and an electromechanical converter, i.e. an electrical machine, that acts as drive mechanism.

Electrical machines exhibit some general features, valid throughout all the variety of types and sizes.

- They have a mainly inductive behavior
- Depending on the rotating speed, they act as both loads and sources of induced electromotive force (EMF).
- Both power direction, from the converter to the load and vice versa, can, in most cases, occur.

On the other hand, modern motor drives usually are designed to satisfy the following requirements:

- Ability to adjust the frequency according to the desired output speed
- Ability to adjust the output voltage so as to maintain a constant air gap flux in the constant-torque region.
- Ability to supply a rated current on a continuous basis at any frequency.

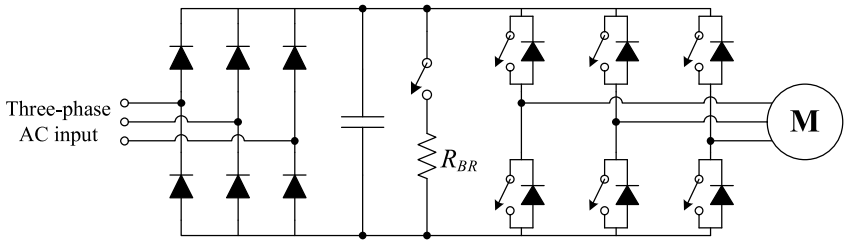


Figure 2.10: Frequency-variable motor drive: three-phase diode rectifier, DC-link capacitor, breaking circuit, three-phase inverter and motor.

Basically, the utility input is rectified by means of either a controlled or an uncontrolled rectifier and then converted again into AC to supply the motor with a three-phase voltage adjusted in magnitude and frequency. Fig. 2.10 shows the schematic of such a system. As already mentioned, the control of both the frequency and the magnitude of the voltage output is up to the inverter. Modulation techniques are further mentioned in chapter 3, here it is enough to say that a typical switching frequency (around $10 \div 20$ kHz) on the inductive load results in a sinusoidal output current, only effected by a small ripple (if not, some output filter might also be adopted).

When the motor is controlled in braking mode, the current direction gets reversed. If a simple diode rectifier is employed, a breaking resistor is generally adopted for dissipating the excess of energy that otherwise could cause the DC-link voltage to reach destructive levels. Generally a dedicated switching device opens and closes the breaking resistor path in dependence to the DC-link voltage.

2.4.1 Control of speed and position

Controlling the speed and/or position of the motor shaft starts with the basic scheme of Fig. 2.9. Depending on the specific application and on the type of machine employed, many different more detailed solution exist. For the purpose of this chapter, only a quick general-terms description is here provided.

Generally, the majority of the control schemes employ a inner torque loop and an outer speed loop, usually adopting PIs or PIDs as controlling blocks. In those applica-

tions where the position must be controlled too, a further outer loop for its control is introduced. Regarding the type of transducer adopted as position and/or speed sensor, the most common choices in modern systems are incremental encoders or resolvers. Only for very accurate servo drives, more refined absolute-position sensors are employed.

A special category of control strategies is that where a physical transducer is not even present, replaced by some algorithm able to estimate speed and position (the latter comes easily as integration of the former) of the rotor basing on the electrical quantities feeding the motor and/or on its equivalent model. Of course, this approach reduces the complexity of the physical system, but increases that of the control algorithm.

In certain applications, some refined figures can be required, such as efficiency maximization, maximization of the torque versus the current, or the minimization of the torque ripple. Generally, torque vs ampere maximization goes along with efficiency maximization; on the contrary, torque ripple minimization turns out to detriments efficiency to a certain extent.

Chapter 3

Modulation techniques

3.1 Pulse-Width Modulation

Pulse-width modulation implies to operate the two switching devices of each inverter leg in a complementary fashion, so to fix output voltage (i.e. the leg center) either to 0 V or to the full DC input voltage, resulting in $0 - V_{DC}$ pulses. The actual modulation occurs by varying the duty-cycle of these high-frequency pulses by means of a low-frequency signal, determined by the control loop. Widths of pulses are determined by the comparison of the low-frequency modulating wave and the high-frequency carrier (typically triangular or sawtooth shaped) so to translate the modulation

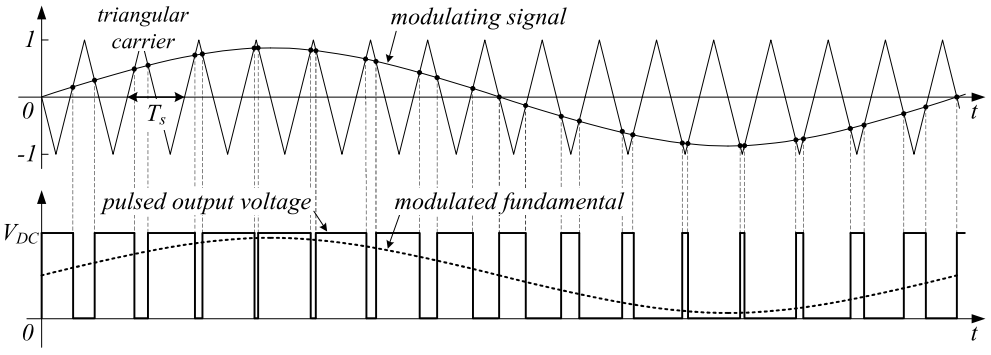


Figure 3.1: Pulse-width modulation.

amplitude into the duration of the positive pulses. In Fig. 3.1 a general example of this strategy is given. A triangular carrier of period T_S is compared with a low-frequency modulating signal: when this signal results above the carrier the output voltage takes the positive value; vice versa, when the modulating signal is below the carrier, it becomes zero. Following this principle, output pulses are modulated in with according to the value of the modulating signal and, as result, the output fundamental assumes its same evolution.

3.1.1 Sinusoidal PWM

The sinusoidal PWM (SPWM) is a well known technique that uses the pulse-width modulation described before, adopting three sinusoidal modulating signals, one for each of the three inverter legs. For a three-phase system, fundamentals of the output voltages referred to the negative terminal N of the DC link are given in equations (3.1), where V_{DC} is the input DC voltage, m is the modulation index and ω_0 is the fundamental output frequency. In these expressions, the subscript 1 denotes that they are for the fundamentals and not for the actual pulsed voltages.

$$v_{UN,1}(t) = \frac{V_{DC}}{2} \cdot [1 + m \cdot \sin(\omega_0 t)] \tag{3.1a}$$

$$v_{VN,1}(t) = \frac{V_{DC}}{2} \cdot [1 + m \cdot \sin(\omega_0 t - 2\pi/3)] \tag{3.1b}$$

$$v_{WN,1}(t) = \frac{V_{DC}}{2} \cdot [1 + m \cdot \sin(\omega_0 t + 2\pi/3)] \tag{3.1c}$$

The fundamental line-to-line output voltages are given by:

$$v_{UV,1}(t) = \frac{\sqrt{3}}{2} \cdot m \cdot V_{DC} \cdot \sin(\omega_0 t + \pi/6) \tag{3.2a}$$

$$v_{VW,1}(t) = \frac{\sqrt{3}}{2} \cdot m \cdot V_{DC} \cdot \sin(\omega_0 t - \pi/2) \tag{3.2b}$$

$$v_{WU,1}(t) = \frac{\sqrt{3}}{2} \cdot m \cdot V_{DC} \cdot \sin(\omega_0 t + 5\pi/6) \tag{3.2c}$$

The operating principle of the sinusoidal PWM modulation with a triangular carrier of period T_S, for a three-phase full-bridge inverter, is given in Fig. 3.2. Here a

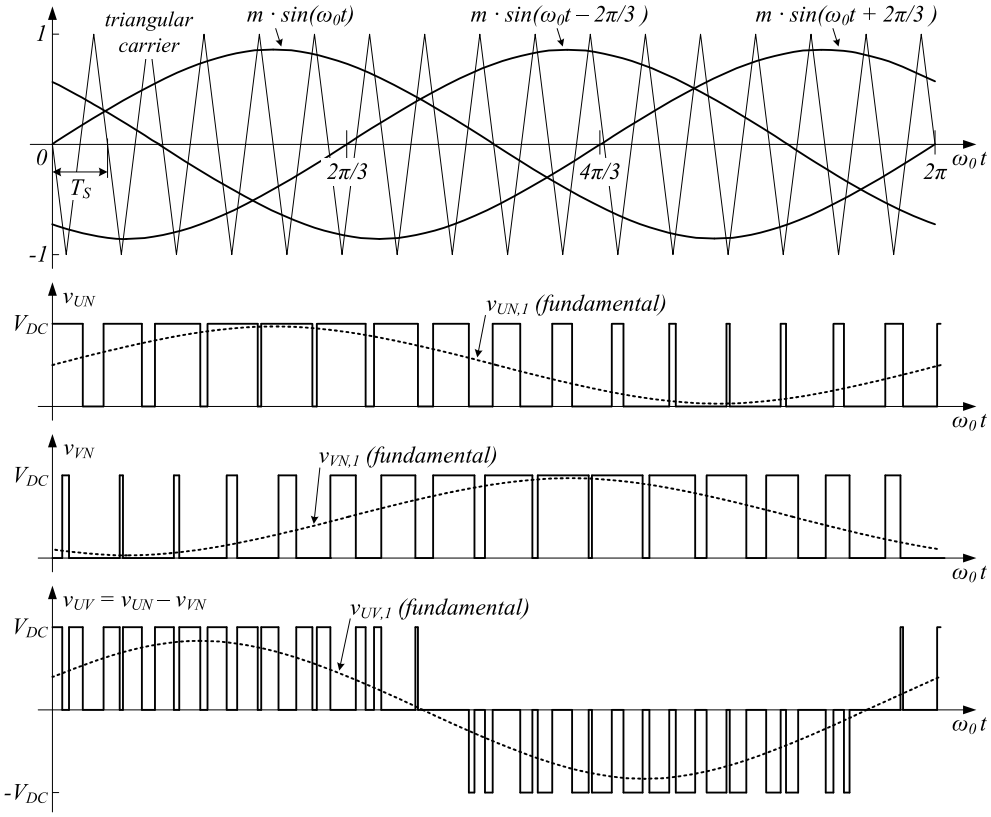


Figure 3.2: Sinusoidal PWM.

small frequency-modulation ratio ($f_S/\omega_0 = 16$) is chosen for clarity of representation. With reference to the inverter of Fig. 3.3, v_{UN} results to be modulated by the couple of switches T_1-T_2, or better by the duty-cycle of their on-time. The same is for the other legs and the couples of switches T_3-T_4 and T_5-T_6. The output voltage linearly depends on the modulation index up to the limit of $m = 1$, while, for higher m, the modulation introduces distortion and the fundamental amplitude does not grow linearly with m. This behavior is summarized in 3.4, which shows the relationship between m and the fundamental of the line-to-line voltage normalized to V_{DC}.

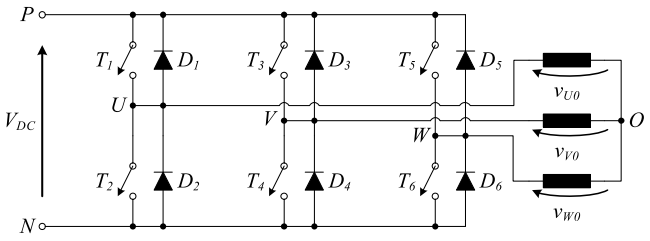


Figure 3.3: Three-phase bridge.

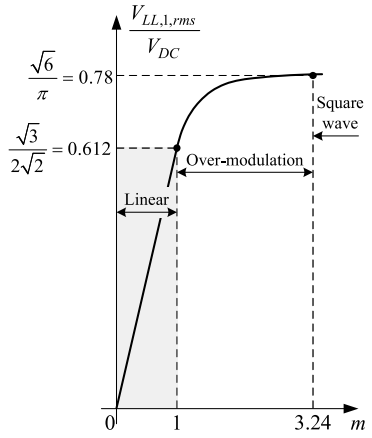


Figure 3.4: Line-to-line voltage, normalized to the DC link voltage V_{DC} as function of the modulation index m. The over-modulation limit ($m = 3.24$) is for $f_S/\omega_0 = 15$.

3.1.2 Third Harmonic Injection

In order to increase the output voltage without introducing over-modulation, the modulation signal can be modified with the addition of a new contribution having three times the fundamental frequency and amplitude equal to one sixth of the original amplitude. In Fig. 3.5 an example of this method is showed, the following signals are plotted: the sinusoidal modulation signal having amplitude equal to 1 (the maximum in the linear region); the third harmonic having an amplitude of 1/6; the total signal resulting by the sum of the previous two. Note that in the line-to-line voltages the third

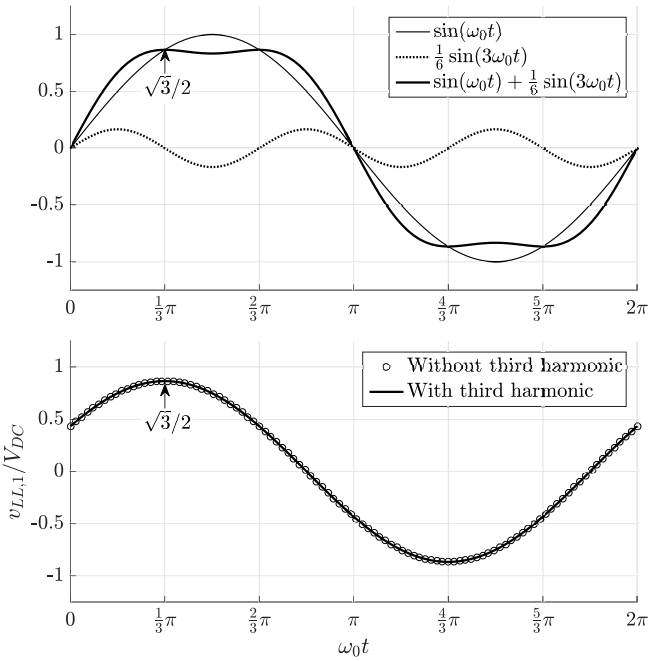


Figure 3.5: Injection of third harmonic. Line-to-line voltage reaches a peak value equal to $V_{DC}\sqrt{3}/2$.

harmonic components cancel each other out, resulting in pure sinusoid both with and without the third harmonic injection. Here the peak of the line-to-line voltage results equal to $V_{DC}\sqrt{3}/2$. Fig. 3.6 shows the case where this strategy makes more sense: the total modulation signal (fundamental plus third harmonic) has been increased by a factor $2/\sqrt{3}$, so to fully exploit the linearity range. The line-to-line voltage can reach a peak value equal to V_{DC}, then exhibiting an increase of about 15 % over the case without injection.

3.1.3 Space-Vector PWM

Space Vector pulse width modulation (SV-PWM or simply SV) is a modulation strategy that synthesizes the output reference voltage V_{ref} by a linear combination of the

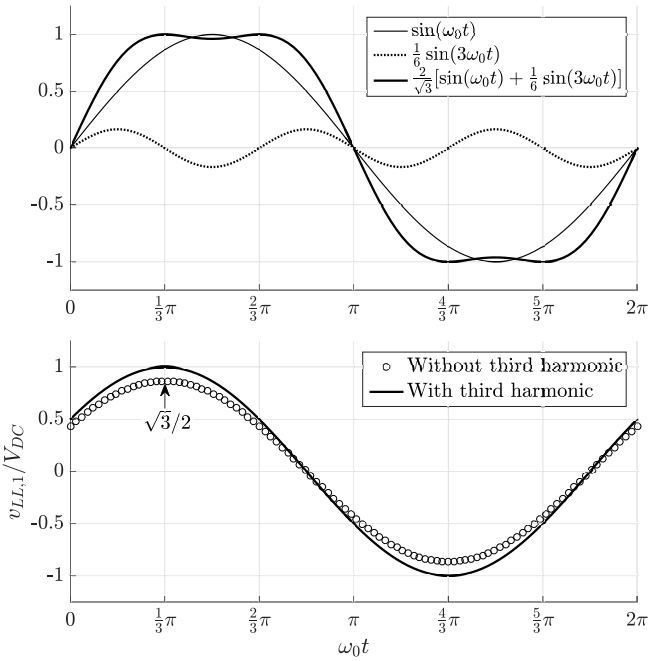


Figure 3.6: Injection of third harmonic increased by $2/\sqrt{3}$. Line-to-line voltage reaches a peak value equal to V_{DC}.

so called space vectors, which are the vectorial representation of the three-phase output voltage for all the possible switching states of the inverter. For a three-legs bridge, eight switching states are possible, six active states and two zero states. Under the notation of equations (1.2) and (1.3), active states are $S_1 = [100]$, $S_2 = [110]$, $S_3 = [010]$, $S_4 = [011]$, $S_5 = [001]$ and $S_6 = [101]$; zero states are $S_7 = [000]$ are $S_8 = [111]$. The eight basic vectors V_j, representing the voltages at inverter output for each space state, lie on the stationary reference frame $\alpha\beta$ as shown in Fig. 3.7: active vectors have a unitary length and are equally spaced 120° apart, zero vectors are instead represented as dots in the origin. The first way of synthesizing the average reference voltage over a sample time, is by means of the two closest basic active vectors and both the zero voltage vectors. In this way, voltage excursion and current ripple are minimized and it is also possible to perform only single-leg transitions. Fig. 3.8 offers an example of

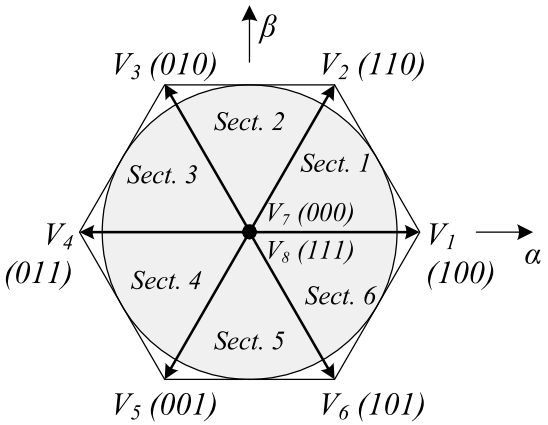
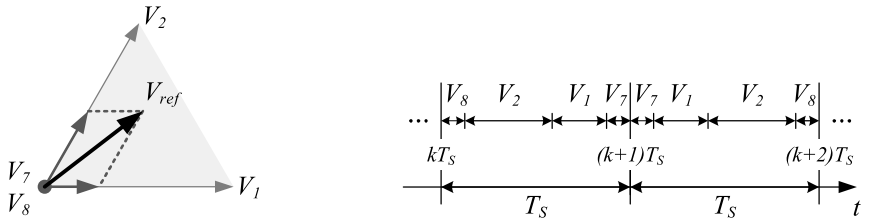


Figure 3.7: Space vector diagram on the stationary reference frame.



(a) Vectorial representation.

(b) Vector usage over time.

Figure 3.8: Generation of V_{REF} in sector 1 as linear combination of V_0, V_1, V_2 and V_7.

this approach, applied for a generic V_{ref} in sector 1, i.e. between 0° and 60°. Active vectors are modulated so to add up to the reference voltage, zero vectors then fulfill the remaining portion of the sampling period.

Decomposing space vectors into their $\alpha\beta$ coordinates, they can be expressed as:

$$\begin{cases} V_j = \begin{pmatrix} \cos(\theta_j) \\ \sin(\theta_j) \end{pmatrix} & \text{for } j = 1,2,\ldots,6 \\ V_j = \begin{pmatrix} 0 \\ 0 \end{pmatrix} & \text{for } j = 7,8 \end{cases} \tag{3.3}$$

The reference voltage vector V_{ref} is built from the weighted sum of the adjoining active vectors V_i and V_k, other then the zero vectors V_7 and V_8, as given in (3.4), where x, y and z are the weighting coefficients. Note that, from now on, subscripts i and k always denote a couple of adjacent space vectors, i.e. 1 and 2, 2 and 3, 3 and 4, 4 and 5 , 5 and 6 or 6 and 1.

$$V_{ref} = x \cdot V_i + y \cdot V_k + z \cdot (V_7 + V_8) \tag{3.4}$$

Given the $\alpha\beta$ coordinates of the reference vector, the modulation function has first to calculate these coefficients. For doing that, equation 3.4 can be expressed in the stationary coordinates as:

$$V_{ref} = \begin{pmatrix} \alpha_{ref} \\ \beta_{ref} \end{pmatrix} = x \begin{pmatrix} \cos(\theta_i) \\ \sin(\theta_i) \end{pmatrix} + y \begin{pmatrix} \cos(\theta_k) \\ \sin(\theta_k) \end{pmatrix} + z \begin{pmatrix} 0 \\ 0 \end{pmatrix} \tag{3.5}$$

That can be rewritten as a system of two equations:

$$\begin{cases} \alpha_{ref} = x \cdot \cos(\theta_i) + y \cdot \cos(\theta_k) \\ \beta_{ref} = x \cdot \sin(\theta_i) + y \cdot \sin(\theta_k) \end{cases} \tag{3.6}$$

Solving the system for x and y leads to:

$$\begin{cases} x = \dfrac{\alpha_{ref} \sin(\theta_k) - \beta_{ref} \cos(\theta_k)}{\sin(\theta_k)\cos(\theta_i) - \sin(\theta_i)\cos(\theta_k)} \\ y = \dfrac{\beta_{ref} \cos(\theta_i) - \alpha_{ref} \sin(\theta_i)}{\sin(\theta_k)\cos(\theta_i) - \sin(\theta_i)\cos(\theta_k)} \end{cases} \tag{3.7}$$

Regarding coefficient z, modulating the zero vectors, from the fact that their usage is aimed to fulfill the sampling period (see Fig. 3.8(b)), it follows that the modulating coefficients add up to one:

$$x + y + z = 1 \tag{3.8}$$

Hence, after x and y have been calculated, it is trivial to obtain z as:

$$z = 1 - x - y. \tag{3.9}$$

Since θ_i and θ_k can only assume six combinations of values, the expressions in (3.7) and (3.9) can be precalculated for all the six possible cases, as summarized in Tab. (3.1).

Table 3.1: Modulating coefficients as functions of α_{REF} and β_{REF}.

Sector	θ_i, θ_k	x	y	z
1	0, 60	$\alpha_{ref} - \beta_{ref}/3$	$2\beta_{ref}/3$	$1 - \alpha_{ref} - \beta_{ref}/3$
2	60, 120	$\alpha_{ref} + \beta_{ref}/3$	$-\alpha_{ref} + \beta_{ref}/3$	$1 - 2\beta_{ref}/3$
3	120, 180	$2\beta_{ref}/3$	$-\alpha_{ref} - \beta_{ref}/3$	$1 + \alpha_{ref} - \beta_{ref}/3$
4	180, 240	$-\alpha_{ref} + \beta_{ref}/3$	$-2\beta_{ref}/3$	$1 + \alpha_{ref} + \beta_{ref}/3$
5	240, 300	$-\alpha_{ref} - \beta_{ref}/3$	$\alpha_{ref} - \beta_{ref}/3$	$1 + 2\beta_{ref}/3$
6	300, 0	$-2\beta_{ref}/3$	$\alpha_{ref} + \beta_{ref}/3$	$1 - \alpha_{ref} + \beta_{ref}/3$

3.1.4 Linearity range

Considering vectors normalized to the input voltage V_{DC}, the limit on the amplitude of the reference vector V_{ref} can reach the unity only in correspondence of the active basic vectors. In between the basic vectors, the limit on the average voltage vector amplitude is limited to the hexagon with vertices on the same basic vectors. Anyhow, the reference voltage must be intended to rotate at the synchronous speed with its constant amplitude and therefore it must be limited to the shaded circle of Fig. 3.7. According to this, the maximum amplitude of V_{ref} is:

$$\left|V_{ref}\right|_{MAX} = \cos\left(\frac{\theta_1}{2}\right) = \cos(30°) = \frac{\sqrt{3}}{2} \simeq 0.866 \tag{3.10}$$

For a balanced three-phase load, the phase voltage has a peak value $2/3$ times the module of the reference vector (see Fig. 3.9. The limit on the phase voltage is:

$$\left|V_{phase}\right|_{MAX} = \frac{2}{3}\left|V_{ref}\right|_{MAX} = \frac{\sqrt{3}}{3} = \simeq 0.577 \tag{3.11}$$

Hence, the limits on the line-to-line voltage and its RMS value for SV PWM are:

$$\left|V_{LL}\right|_{MAX} = \sqrt{3}\left|V_{phase}\right|_{MAX} = 1 \tag{3.12}$$

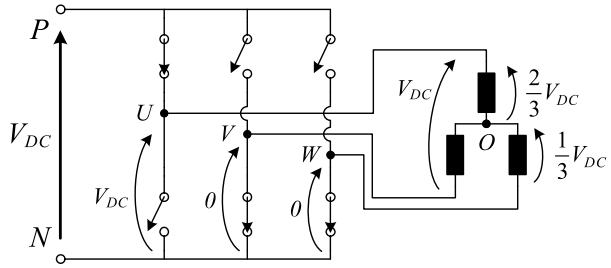


Figure 3.9: Three-phase inverter performing state 1 (vector V_1) on a balanced load.

$$|V_{LL,rms}|_{MAX} = \frac{1}{\sqrt{2}}|V_{LL}|_{MAX} = \frac{1}{\sqrt{2}} = \simeq 0.707 \tag{3.13}$$

In Fig. 3.4 it was shown that the upper linearity limit for S-PWM results in an RMS value of the line-to-line fundamental equal to $0.612V_{DC}$. Comparing the limits for S-PWM and SV-PWM highlights that SV better utilizes the input DC voltage, resulting in a $v_{LL,1}$ higher for a factor $2/\sqrt{3}$ (about 15 % increase). This is the same achievable with third harmonic injection, as discussed in the previous paragraph.

3.2 Dead-Time Compensation

Pulse widths of the two switching devices in each inverter leg in practice are not perfectly complementary. A short period of time must be introduced between the turn-off of one of the two devices and the turn-on of the other one, in order to prevent both devices to be simultaneously on, ultimately creating a disruptive short circuit of the DC link. This delay is usually referred to as dead time (here symbolized by T_d), dwell or blanking time.

When the width of modulated pulses becomes smaller than the dead time, they in practice are not performed. Because of the presence of freewheeling diodes, during dead times the output voltage depends on the current direction. Of course, fast devices need short dead times and so they limit this unwanted phenomenon to a small modulation range, but still it can not be eliminated completely. In order to compensate the distortion introduced by dead times, several countermeasures have been proposed

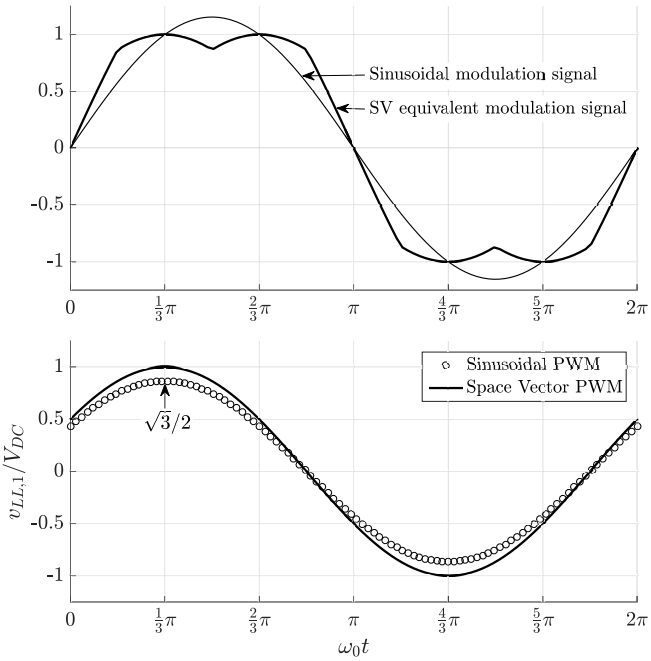


Figure 3.10: Space vector equivalent modulation signal and line-to-line fundamental compared to S-PWM.

over the years. Despite the need for a separate dead-time compensator can be eliminated in the case of a fast current control, that can compensate for the distortion arising in the low-modulation regions, a dedicated compensator -or a compensating function -is needed when such a high-bandwidth control is not present in the system, or when it must achieve very little harmonic distortion. Over the years, both software and hardware as well as feed-back and feed-forward approaches have been proposed. Despite this wide range of possibilities, as introduction to the work of this thesis, in this chapter only software feed-forward compensation is explained.

Adopting a software feed-forward compensation only needs to know the sign of each phase current, basing on which a different expression of the modulation index is adopted, as explained in the following.

Taking into account effects of dead time T_d and storage time during turn-off of de-

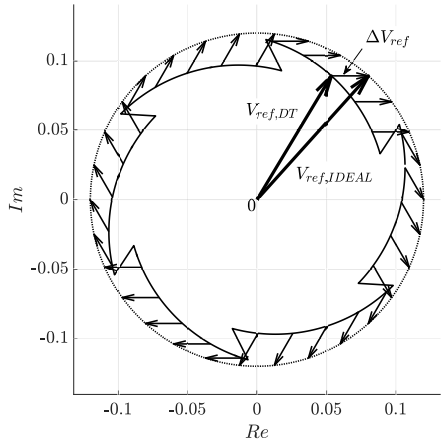


Figure 3.11: Trajectory of the distorted reference vector because of dead time. Plot parameters are: $m = 0.12$, $T_d = 1\,\mu s$, $T_{st} = 1\,ns$, $f_s = 20\,kHz$.

vices T_{st}, the voltage vector (averaged over a sampling period T_s) is actually effected by an error [20]:

$$\Delta V_{ref} = \frac{T_d - T_{st}}{T_s} \cdot \frac{2}{3} \left[\text{sign}(i_U) + e^{j2\pi/3} \text{sign}(i_V) + e^{j4\pi/3} \text{sign}(i_W) \right] \tag{3.14}$$

Hence, the resulting voltage vector is

$$V_{ref,DT} = V_{ref,IDEAL} - \Delta V_{ref} \tag{3.15}$$

Fig. 3.11 shows how this phenomenon effect the trajectory of reference vectors on the stationary reference frame. The software compensating function has to know signs of the currents and the storage time T_s, or at least a good estimation of it, then it is trivial to compensate the reference voltage vector by adding to the computed reference voltage a contribution equal to ΔV_{ref}.

3.3 Modulations with reduced common-mode voltage

Despite the fact that two-level three-phase transformerless inverters are widely used in electronics, it is also well known that they exhibit poor CMV characteristics. The existence of several common-mode capacitive paths between the converter and ground (see Fig. 1.4), permits leakage currents to flow at every CMV variation, thus high-frequency pulse-width modulation produce high common-mode leakage currents [21]. In motor drive applications, this may lead to motor bearing failures, EMI noise that causes inverter drive trip, or interference with other electronic equipment in the vicinity [22]. In PV applications, leakage current detriments efficiency and, also, strict rules exist about the injection of common-mode currents into the grid. For these reasons, a lot of research was focused onto this topic over the last two decades. Considering the capacitive nature of the aforementioned common-mode path, this problem can be faced by reducing as much as possible the CMV in the amplitude and/or in the frequency of its variations. Ultimately, a constant CMV would not produce such leakage currents.

Space vector is the more suitable family of modulations for facing this problem, since it acts governing the actual state of all the switching devices. In principle, a constant CMV is not difficult to obtain: it is enough to adopt only states having the same CMV, but, unfortunately, this approach is not free from drawbacks which, in some cases, turn out to be too severe. In the past, several authors dealt with the CMV-related problem adopting variations of the basic SV PWM patterns [23, 24]. Unfortunately, all these ideas suffer from some drawbacks such as not complete elimination of the CMV, high current ripple or distortion, or even being not practically feasible. In [25] a combined algorithm with satisfactory CMV reduction performance is proposed, but it still exhibits CMV variations over the PWM period, although reduced in amplitude and frequency compared to a traditional modulation. In this chapter, a brief survey of these reduced common-mode voltage PWM (RCMV-PWM) is given.

Differently from SVPWM, which make use of all active and inactive vectors, RCMV-PWM methods only utilize some combination of the active ones. Detailed vector patterns for all of them (and in dependence to the regions defined in Fig. 3.12)

are given in Tab. 3.2. Also, they are here listed and briefly described.

- Active Zero-State (AZSPWM): instead of the actual zero-voltage vectors (V_0 and V_7), a pair of opposite active vectors are put in place for the same duration to effectively act -on average, over the sampling period -as a zero-voltage vector. Three sub-variants of this idea were reported in literature, addressed as AZSPWM1-3, each one adopting a different combination of opposite vectors.
- Remote States (RSPWM): three active vectors 120° apart from each other are used. Either groups V_1-V_3-V_5 or V_2-V_4-V_6 can be adopted and, also, various sequences can be chosen within the same group. Four variants were reported for this class of modulation, named RSPWM1, RSPWM2A-B and RSPWM3.
- Near States (NSPWM): the voltage vector closest to the reference and its two right and left neighbors are used. Also, they are put in sequence so to obtain the minimum number of switching occurrences. With this method, devices in one of the three legs do not switch within each sampling cycle.
- Discontinuous (DPWM): it is very similar to the classical SVPWM, with the only difference that one of the two inactive states is avoided and, as consequence, CMV is subjected to one less variation step.

Frequency and polarity of CMV is different for each RCMV-PWM. For RSPWM1 and RSPWM2, CMV frequency is theoretically zero, implying no CMV variation, which is the most attractive condition. Similarly, in RSPWM3, CMV is constant, but only for a 60° interval. In AZSPWM2 and AZSPWM3, the CMV varies at the PWM frequency, however steps are smaller than with SVPWM. For all the other RCMV-PWM, CMV frequency and number of steps are higher, thus they are less attractive. Actually, only SVPWM, DPWM1, AZSPWM1 and NSPWM make use of one switching event at a time, instead all the other RCMV-PWMs methods need simultaneous switching of two inverter legs. In practice, this would cause big line-to-line voltage reversals, resulting in significant - or even intolerable - output ripple.

In conclusion, only AZSPWM1 and NSPWM turn out to be feasible alternatives for the reduction of the CMV in two-level three-phase transformerless inverters.

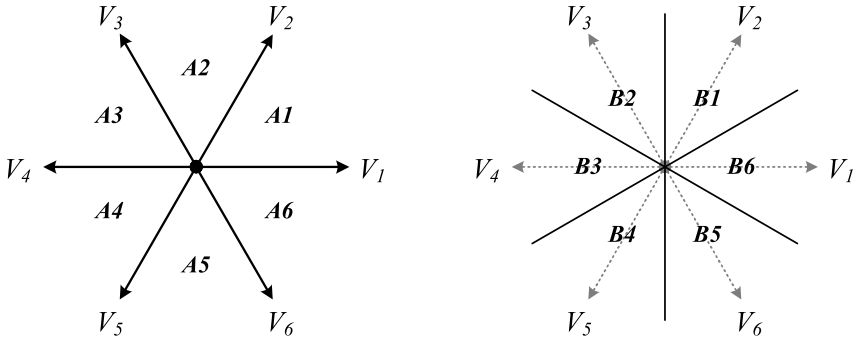
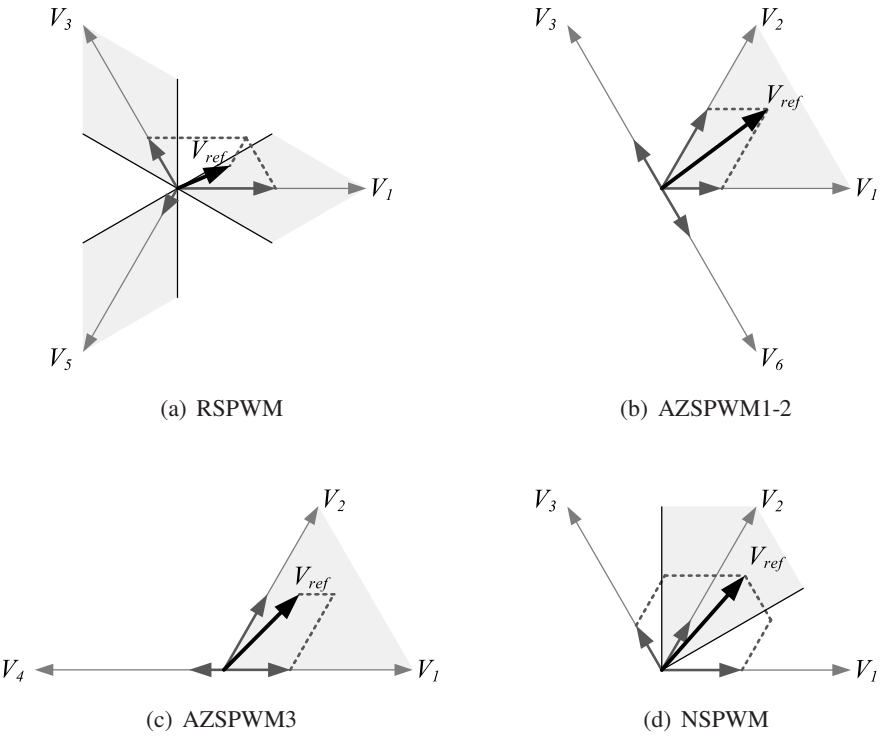


Figure 3.12: Definition of A- and B-regions on the SV diagram.



(a) RSPWM

(b) AZSPWM1-2

(c) AZSPWM3

(d) NSPWM

Figure 3.13: Reference voltage formation for the RCMV-PWM. Shaded areas indicate the regions where the depicted sets of vectors are employed.

Table 3.2: Vector patterns for various space-vector methods.

	A1	A2	A3	A4	A5	A6
SVPWM	8217128	8237328	8437348	8457548	8657568	8517168
AZSPWM1	3216123	5321234	5432345	6543456	1654561	2165612
AZSPWM2	6213126	1324231	2435342	3546453	4651564	5162615
AZSPWM3	12421	13532	34643	45154	56265	61316
RSPWM1	31513	31513	31513	31513	31513	31513
RSPWM2A	31513	13531	13531	15351	15351	31513
RSPWM2B	42624	42624	24642	24642	26462	26462

	B1	B2	B3	B4	B5	B6
RSPWM3	31513	42624	13531	24642	15351	26462
NSPWM	21612	32123	43234	54345	65456	16561

	B1	A1	B2	A2	B3	A3	B4	A4	B5	A5	B6	A6	B1
DPWM1	82128		23732		84348		45754		86568		61716		
		21712		82328		43734		84548		65756		86168	
DPWM2	82128		23832		84348		45854		86568		61816		
		21812		82328		43834		84548		65856		86168	

Chapter 4

H8 converter

4.1 Introduction

The core of this work of thesis is the development of a new architecture of three-phase transformerless inverter. Key feature of the project is the reduction of the CMV. This follows the trend of the recent years of introducing novelties that deal with the CMV-related problems in transformerless inverters. Despite the fact that good ideas were already proposed, this work was motivated by the necessity of exploring the simple idea of decoupling DC and AC sides of the inverter with switching devices, which is a strategy that has already been demonstrated to be effective in single phase converters. Alongside the novel architecture, also the modulation was developed with the CMV reduction in mind, exploiting the degrees of freedom given by SV modulation.

This chapter exposes the details of the topology, but for now components are treated in the most general way: switching devices are intended as mono-directional switches with ideal anti-parallel diodes, also no precise values are given for resistors and capacitors. This is for avoiding confusion mixing together considerations about topology and functioning with those regarding semiconductor technology and design. The other subsections are dedicated to the adopted modulation, the system control and finally to simulation results.

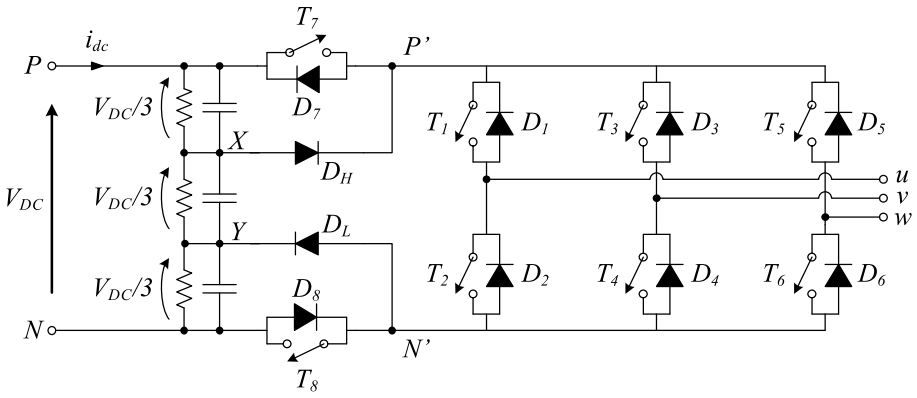


Figure 4.1: H8 inverter.

4.2 Architecture of the converter

The architecture of H8 inverter is shown in Fig. 4.1. Deriving from the H6 traditional structure and having a total of eight active devices, it was named “H8”. It differs from a traditional H6 for the presence, at the DC side, of a network composed by a three-levels voltage divider, two active devices and two clamping diodes. Details on these add-ons are discussed in the following subsections.

4.2.1 Voltage divider

The capacitive divider placed on the DC side of the inverter has the purpose to obtain from the DC-link the intermediate levels:

$$V_{YN} = \frac{V_{DC}}{3} \tag{4.1}$$

$$V_{XN} = \frac{2}{3} V_{DC} \tag{4.2}$$

These two levels are useful to match the CMV values respectively during the odd (V_1, V_3, V_5) and even (V_2, V_4, V_6) active states, as will be further explained in Sec. 4.3. In order to ensure a good partition of the voltage across the capacitors (i.e. not determined by their ESRs), three resistors were added in parallel to them and their value was chosen high enough to ensure acceptably low DC losses. In order to obtain

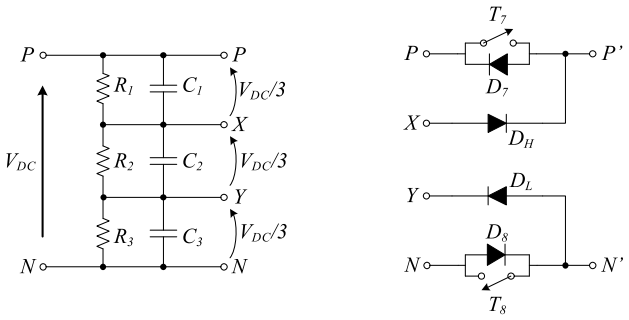


Figure 4.2: DC-side of H8 inverter: voltage diver (a) and decoupling network (b).

an equal voltage division, $R_1 = R_2 = R_3 = R_{DC}$. Consequently, power loss on the resistive divider is given by:

$$P_{DC} = \frac{V_{DC}^2}{R_1 + R_2 + R_3} = \frac{V_{DC}^2}{3R_{DC}} \tag{4.3}$$

Given the maximum acceptable loss value $P_{DC,MAX}$, it must be ensured that

$$P_{DC} = \frac{V_{DC}^2}{3R_{DC}} \leq P_{DC,MAX} \tag{4.4}$$

Hence, R_{DC} must be chosen so that:

$$R_{DC} \geq \frac{V_{DC}^2}{3P_{DC,MAX}} \tag{4.5}$$

4.2.2 DC-decoupling and voltage clamping

As shown in Fig. 4.2(b), H8 includes two switching devices referred to as T_7 and T_8 which act as DC-decoupling devices during the current freewheeling phases. On the contrary, during active states they are kept on, so to ensure the usual conduction path from the DC source to the inverter legs. In this condition they inevitably introduce on-state losses that detriment the overall efficiency of the converter. However, if they are chosen accurately, this drawback can still be of acceptable impact. As a matter of

fact, the six "classical" devices in the bridge must withstand the entire supply voltage, whereas across T_7 and T_8 only one third of it appears, so they can be chosen with a smaller breakdown voltage, which usually goes with smaller on-state resistance. It is also worth to be mentioned that, instead, their current rate must be the same of the other six devices.

Moving to the diodes named D_H and D_L, the first is placed between the intermediate point of the divider X and the upper bridge rail, labeled as P'; reciprocally, the latter is placed between the negative bridge rail (N') and the intermediate point of the divider Y. The purpose of these diodes is to clamp the voltage at the high - or low - side of the bridge during the upper - or bottom - current freewheeling phases. Actually, they happen to be off for most of the time, since they are only forced on for a short period, when the inverter enters into a zero state. The actual duration of this period depends on the time necessary for the charge redistribution to occur and this, given a certain supply voltage, is ultimately up to physical parameters of the components, such as stray capacitances and resistances. This process is more deeply explained in the following section dedicated to the reduction of the CMV.

4.3 Common-mode voltage reduction

As introduced in chapter 1, CMV is defined as the average of the voltages between the inverter outputs and the negative DC source (addressed as N):

$$V_{CM} = \frac{V_{uN} + V_{vN} + V_{wN}}{3} \tag{4.6}$$

Table 4.1 summarizes the common mode voltage values at the inverter output, both for a traditional three-phase inverter and for the proposed H8 topology. In the case of a traditional H6, the CMV varies from 0 to V_{DC}, with a $V_{DC}/3$ step at every state commutation. Instead, the H8 topology only presents two values: $V_{DC}/3$ for all the odd states and $2V_{DC}/3$ for all the even ones. This is possible for the presence of the DC-decoupling devices (T_7 and T_8) and of the voltage-clamping diodes (D_H and D_L).

When the inverter leaves an active state entering into a zero state, it goes through the following five steps, here referred to the transition from state 1 to state 7 as case of example:

1. Inverter is in state 1 (100), T_7 and T_8 are both on.

2. While current is flowing, T_8 is switched off.

3. As T_8 switches off, inductive load forces diode D_L to turn on (Fig. 4.4(a)). Bottom bridge rail is brought to $V_{DC}/3$, meaning $V_{N'N} = V_{DC}/3$.

4. T_1 switches off, dead time between state 1 and state 7 starts.

5. T_2 switches on, dead time ends. Inverter is in state 7 (000).

In more general terms, before the freewheeling phase (state 7 or 8), one DC-decoupling device (T_8 or T_7) is switched off and this causes the clamping diode (D_L or D_H) to turn on, thus clamping the voltage on the upper or lower rail of the bridge to the same value that CMV had during the previous active state ($V_{DC}/3$ or $2V_{DC}/3$). On state voltages across diodes are not taken into account now for simplicity and because they do not change qualitatively the behavior of the system.

Fig. 4.4 shows the configurations of the inverter which are put in place at every transitions from one active state to the following inactive one. As a matter of fact, during these temporary phases the three legs still maintain the previous configuration. For example, during transition from state 1 to state 7 (Fig. 4.4(a)), terminals u and w have potential equal to $V_{DC}/3$, while terminal u maintains the previous potential equal to V_{DC}. Extending the same analysis to all the cases, it is possible to see that:

- Odd states (Figs. 4.4(a), 4.4(c) and 4.4(e)): one output port remains at V_{DC} and the other two are fixed to $V_{DC}/3$ by diode D_L.

- Even states (Figs. 4.4(b), 4.4(d) and 4.4(f)): one output port remains at zero and the other two are fixed to $2V_{DC}/3$ by diode D_H.

As consequence, $V_{CM} = V'_{CM}$ for the odd cases, whereas $V_{CM} = V''_{CM}$ in the even one, where:

$$V'_{CM} = \frac{1}{3}\left(1 + \frac{1}{3} + \frac{1}{3}\right) V_{DC} = \frac{5}{9} V_{DC} = 0.55 V_{DC} \tag{4.7a}$$

$$V''_{CM} = \frac{1}{3}\left(0 + \frac{2}{3} + \frac{2}{3}\right) V_{DC} = \frac{4}{9} V_{DC} = 0.44 V_{DC} \tag{4.7b}$$

Unfortunately, this implies that CMV does not remain constant throughout a PWM period, instead it varies from $V_{DC}/3$ to $5V_{DC}/9$ (odd cases) or from $2V_{DC}/3$ to $4V_{DC}/9$ (even cases) at every transition from an active to a zero vector. Despite this means that a totally constant CMV can not be achieved, these variations have a relatively small excursions if compared to those typical of traditional solutions. In particular, for the two cases, they result to be:

$$\Delta V'_{CM} = \frac{5}{9} V_{DC} - \frac{1}{3} V_{DC} = +\frac{2}{9} V_{DC} = +0.22 V_{DC} \tag{4.8a}$$

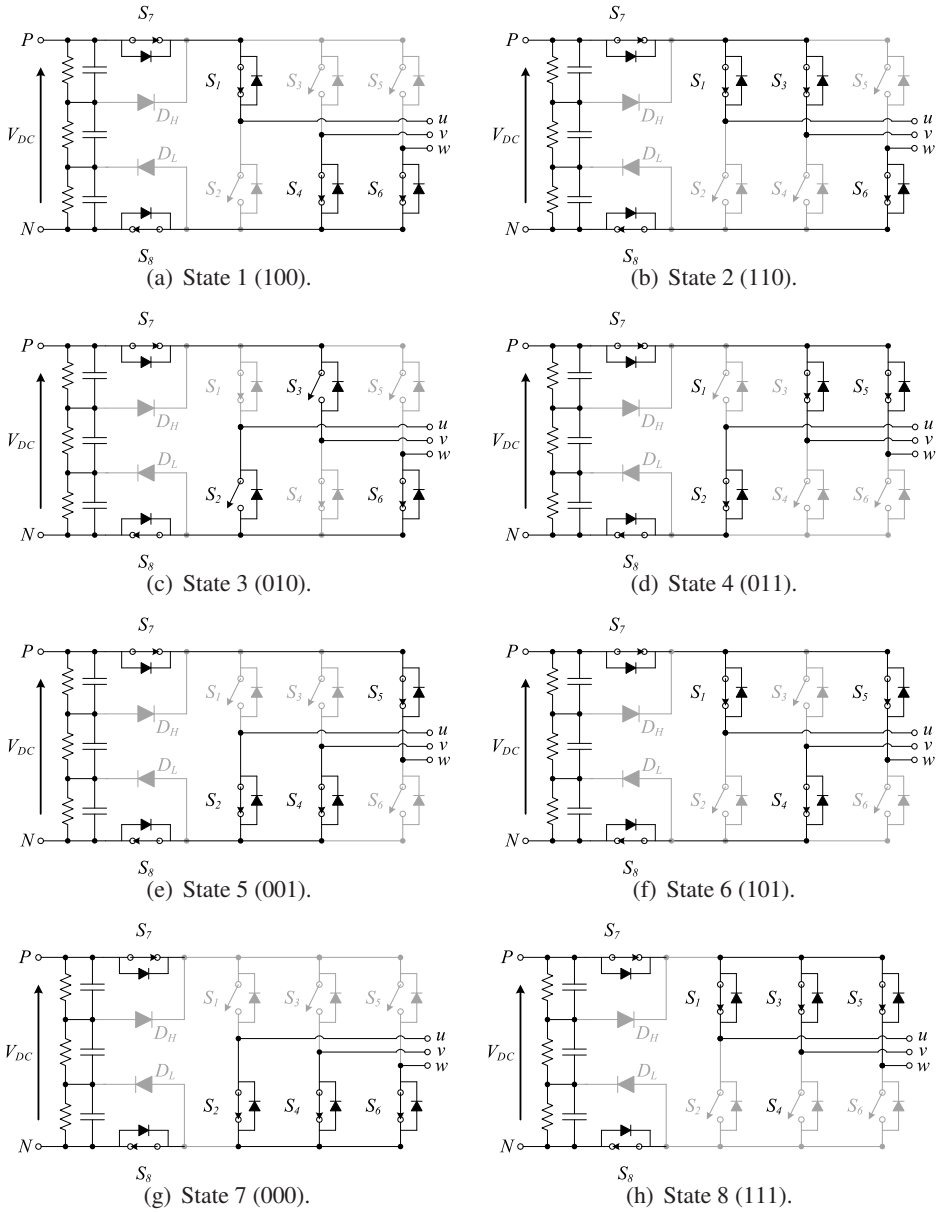
$$\Delta V''_{CM} = \frac{4}{9} V_{DC} - \frac{2}{3} V_{DC} = -\frac{2}{9} V_{DC} = -0.22 V_{DC} \tag{4.8b}$$

It is worth to be noted that the described process implies D_H or D_L turn on only for few nanoseconds, charging or discharging the stray capacitance of the switching devices, therefore not causing a significant unbalance in the voltage divider. Anyhow, they are passive devices, so they need a current flowing in the load inductances in order to turn on. In case of zero current this does not occur, hence the decoupling strategy does not help and the CMV deteriorates.

Moreover, as already mentioned, since the two clamping diodes ensure the voltage across T_7 and T_8 to be only one third of the total DC bus, devices with a reduced breakdown voltage can be adopted, reducing than the additional losses and cost that these devices introduce.

Table 4.1: Common-mode voltage (V_{CM}) values

	Vector	$\frac{V_{uN}}{V_{DC}}$	$\frac{V_{vN}}{V_{DC}}$	$\frac{V_{wN}}{V_{DC}}$	V_{CM}/V_{DC} H6	V_{CM}/V_{DC} H8
	V_1	1	0	0	$1/3$	$1/3$
	V_2	1	1	0	$2/3$	$2/3$
	V_3	0	1	0	$1/3$	$1/3$
	V_4	0	1	1	$2/3$	$2/3$
	V_5	0	0	1	$1/3$	$1/3$
	V_6	1	0	1	$2/3$	$2/3$
H6	V_7	0	0	0	0	
	V_8	1	1	1	1	
H8	V_7	$1/3$	$1/3$	$1/3$		$1/3$
	V_8	$2/3$	$2/3$	$2/3$		$2/3$



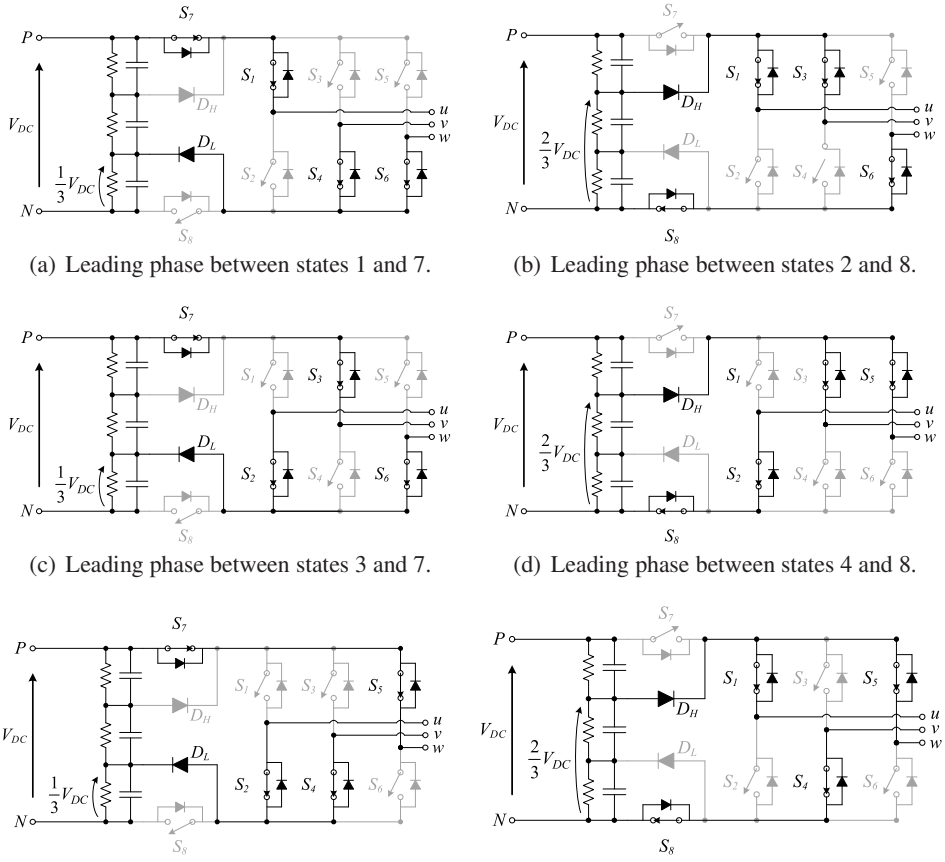
(a) State 1 (100). (b) State 2 (110).

(c) State 3 (010). (d) State 4 (011).

(e) State 5 (001). (f) State 6 (101).

(g) State 7 (000). (h) State 8 (111).

Figure 4.3: Switching configurations of the H8 inverter for the eight SV states. Devices are depicted in black if on, in gray if off.



(a) Leading phase between states 1 and 7.

(b) Leading phase between states 2 and 8.

(c) Leading phase between states 3 and 7.

(d) Leading phase between states 4 and 8.

(e) Leading phase between states 5 and 7.

(f) Leading phase between states 6 and 8.

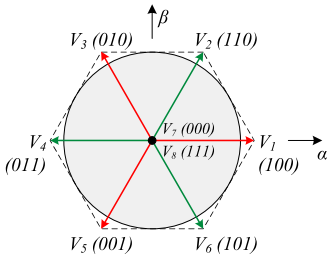
Figure 4.4: Switching configurations of the H8 inverter during transitions from active to inactive states. Devices are depicted in black if on, in gray if off

4.4 Space-Vector modulation

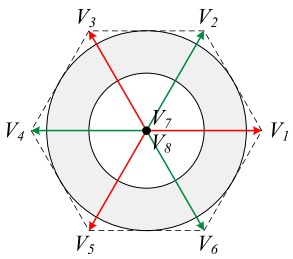
The modulation adopted for the control of the inverter is a novel SV strategy, specifically developed with the H8 architecture in mind, with the aim to achieve CMV to vary as little as possible (as previously discussed, $\pm 2V_{DC}/9$ variations are unavoidable). Also, single-leg commutations were a mandatory feature, this in order to ensure feasibility in practice. In the following, this strategy will be addressed as Constant Common-Mode Voltage SV (CCMV-SV), discussed in the following subsection. Unfortunately, this strategy suffers from the main drawbacks of being applicable only for modulation indexes lower than 0.5 (see the shaded area in Figs. 4.5(c) and 4.5(d)). In order to overcome to this limitation, a different control strategy must be put in place when a higher modulation index is needed. In such a case, a Near-State SV (NS-SV) is adopted, which extends the modulation index range up to $\sqrt{3}/2$ (see the shaded area in Fig. 4.5(b)). Compared to CCMV-SV, NS-SV performs worse in terms of CMV, but in conjunction with the proposed topology it ensures advantages over conventional three-phase inverters and traditional modulations. The following two subsections discuss in further details the two developed modulation strategies.

4.4.1 Constant Common-Mode Space Vector (CCMV-SV)

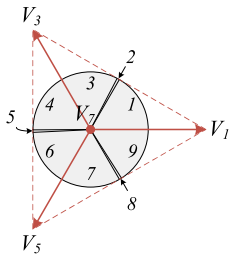
In order to maintain a constant CMV at the inverter output, this SV strategy only makes use of those vectors exhibiting the same V_{CM}. Table 4.1 shows the ratios between V_{CM} and V_{DC} for all the eight SV states. As a matter of fact, odd active vectors (V_1, V_3 and V_5) exhibit $V_{CM} = V_{DC}/3$, while even active vectors (V_2, V_4 and V_6) have $V_{CM} = 2V_{DC}/3$. This is also true considering the H6 and, indeed, several modulations were proposed in literature attempting to keep common-mode voltage constant by using only a set of vectors that exhibit the same V_{CM} [23]. Nevertheless, those modulations do not make use of inactive vectors (V_7, V_8), and this results in simultaneous commutations of more than one bridge leg. On the contrary, adopting the H8 architecture, V_{CM} values of the inactive vectors, thanks to the DC decoupling, can match them of the active states. In this context, it is possible to obtain the same CMV values with all the odd vectors (V_1, V_3, V_5 and V_7), or with all the even ones (V_2, V_4, V_6 and



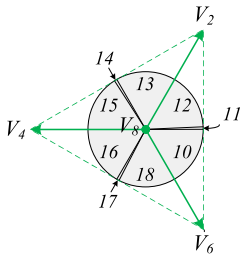
(a) SV vectors diagram.



(b) The region where SVPWM is used $(0.5 \leq m < \sqrt{3}/2)$.



(c) Linearity region $(m < 0.5)$ and modulation zones numbering for odd CCMV-SV.



(d) Linearity region $(m < 0.5)$ and modulation zones numbering for even CCMV-SV.

Figure 4.5: Space Vector diagrams in the $\alpha\beta$ plane. Odd vectors are red colored, even vectors are green colored.

Table 4.2: Vectors usage in CCMV-SV modulation strategy

Angles	Odd vectors	Even vectors
$0° - 60°$	V_1, V_3, V_7	V_2, V_6, V_8
$60° - 20°$		V_2, V_4, V_8
$120° - 180°$	V_3, V_5, V_7	
$180° - 240°$		V_4, V_6, V_8
$240° - 300°$	V_5, V_1, V_7	
$300° - 360°$		V_2, V_6, V_8

V_8). As already mentioned, at every transition from an active state to an inactive one, CMV becomes equal to $4V_{DC}/9$ or to $5V_{DC}/9$ (see Eq. 4.7), leading to a $\pm 2V_{DC}/9$ variation of CMV.

The reference vector in the $\alpha\beta$ plane is synthesized by the use of the two nearest odd or even vectors with the proper modulated duration, plus the proper inactive state fulfilling the remaining time in the PWM period. Applying this scheme, the points which can be synthesized are included in two equilateral triangles having vertexes on the applied active vectors (see Fig. 4.5(c) and 4.5(d)). The maximum modulation index which is possible to maintain throughout the entire rotational period is 0.5. This is a rather limiting feature for an electric drive, therefore a different modulation strategy has been adopted for modulation indexes greater than 0.5 (NS-SV), which is exposed in subsection 4.4.2.

In order to perform a single leg commutation for each state transition, the $\alpha\beta$ plane has been divided into different zones, each one featuring different state sequences. Considering the odd vectors case, shown in Fig. 4.5(c), there are six 60°-wide zones (nr. 1, 3, 4, 6, 7 and 9), plus 3 zones without a specific angular width, represented as very narrow slices (nr. 2, 5 and 8). Such narrow zones are intended to represent SV sequences just applied for a single PWM period, because they are necessary for matching the state sequences performed in their two adjacent zones. An equivalent subdivision exists for the dual case adopting even vectors. Table 4.2 summarizes the

vectors usage for all the zones, both for odd and even CCMV-SV strategy. In order to achieve symmetry during the switching period, in the 60°-wide zones one of the two active states is split into two separated slots of time at the margin of the sequences. The pulse pattern during a switching period is shown in Fig. 4.6 for all the zones in the $\alpha\beta$ plane, both in case of even and odd vectors. In case of no 60°-wide zones (2, 5, 8, 11, 14 and 17) the symmetry is not maintained because, for their native purpose, in those cases sequences must begin and finish with different active states. Moreover, the location of these zones in the $\alpha\beta$ plane implies that the two modulation values for the active states will be approximately equal. Featuring only three states instead of five, these intermediate slots must last half the time than the others, otherwise the output current would have a bigger ripple.

4.4.2 Traditional Space-Vector

Whenever the control loop requires for the inverter a modulation index higher than 0.5, the control function automatically changes to the traditional space vector modulation strategy (SVPWM) which provides an extension of the modulation range up to $\sqrt{3}/2$. This strategy, already introduced in Chapter 3, makes use of the two adjacent active vectors and both the two zero vectors. States sequences have been chosen in order to ensure single leg commutations throughout 360°. During each PWM period the time dedicated to inactive vectors is equally distributed between both V_7 and V_8; sequences exhibit a central symmetry and active states are put in place according to the minimum difference (in terms of switching configuration) they have with respect to the previous or subsequent inactive state. The resulting pulse pattern is shown in Fig. 4.7, along with the evolution of CMV. It is wort to be mentioned that this modulation applied to a traditional three-phase converter would exhibit CMV varying from zero to V_{DC} within each PWM period, whereas adopting the H8 architecture limits the V_{CM} excursion in the range from $V_{DC}/3$ to $2V_{DC}/3$. In comparison to CCMV-SV, more common-mode voltage is present, but still the H8 structure helps to keep its excursion limited.

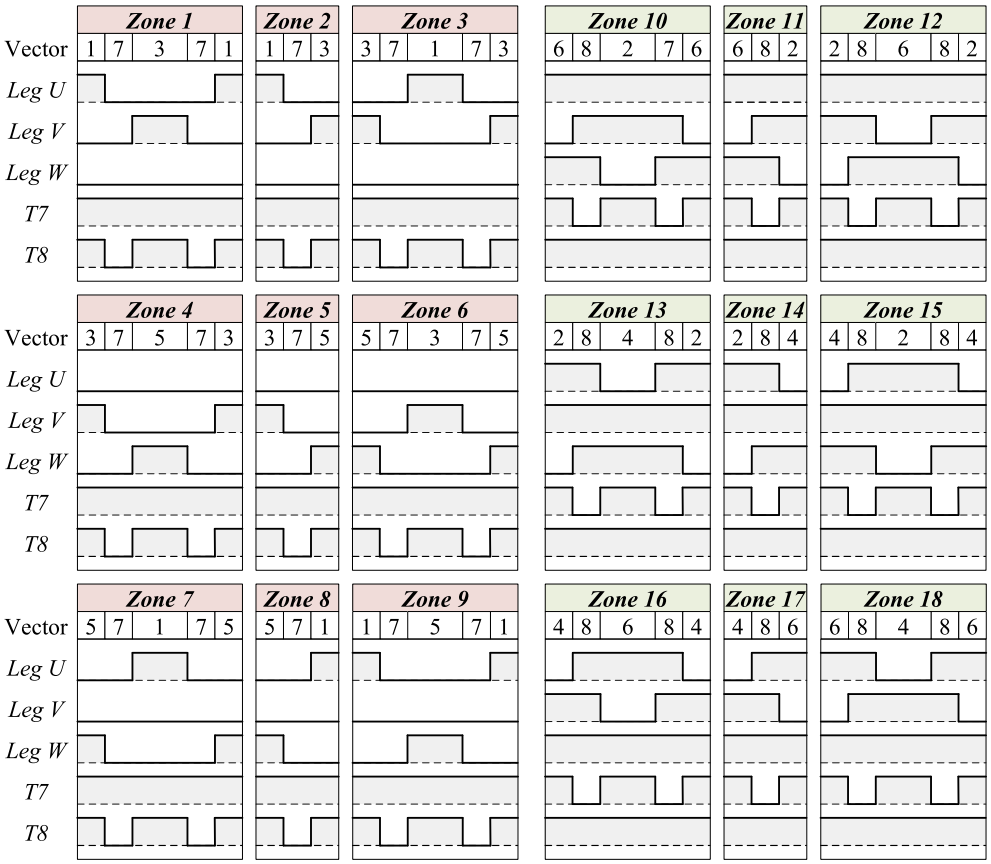


Figure 4.6: State sequences fo CCMV-SV in H8 converter. Zones from 1 to 9 employ odd vectors, zones from 10 to 18 even ones.

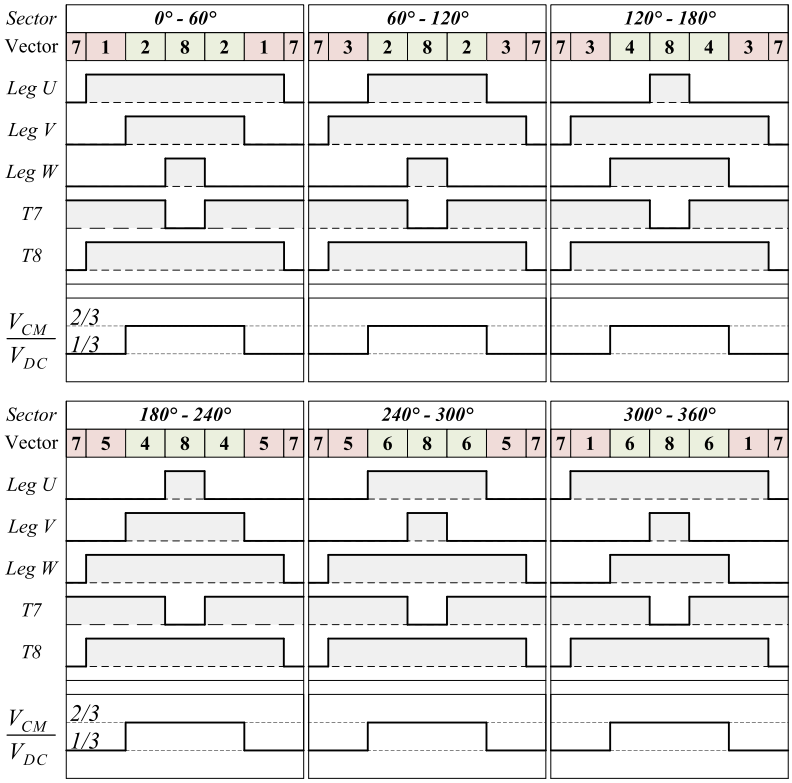


Figure 4.7: Vectors usage and switch pulse pattern throughout the rotational period for the SVPWM. For each angular sector only one PWM period is represented. Odd vectors are highlighted in red, even vectors in green. Widths of the time slots are chosen as case of example.

4.5 Control

The control scheme adopted for H8 converter for a grid connected (PV) application is depicted in 4.8. Current control is performed in the synchronous reference frame, i.e. on dq-transformed quantities. Balanced sinusoidal three-phase quantities turn in constant values when transformed in the dq synchronous frame, therefore, with a PI for each of the two dq components, it is possible to perform the control of the three-phase currents with zero steady-state error.

It must be said that reference values are here considered as input signals from some external MPPT block, not subject of this work.

In addition to the PI-regulated components of the modulation index, dq feed-forward contributes ($m_{FF,d}$ and $m_{FF,q}$) are added in the control loops. For counterbalancing the presence of the grid voltages at the inverter output, the feed-forward contribution must be

$$m_{FF,dq} = \frac{\sqrt{3}}{2}\frac{v_{LL,dq}}{V_{DC}} \tag{4.9}$$

Where $v_{LL,dq}$ is the dq-transformed line-to-line voltage and V_{DC} is the DC supply voltage. In Fig. 4.8, the k_{FF} is not actually a constant, instead it is a function of V_{DC}, defined as:

$$k_{FF} = \frac{m_{FF,dq}}{v_{LL,dq}} = \frac{\sqrt{3}}{2V_{DC}} \tag{4.10}$$

Synchronization to the three-phase grid is made by means of a PLL based on the synchronous reference frame, where the angular position of the voltage vector is tracked regulating to zero, by a feedback loop, the quadrature component on the synchronous frame. Its scheme is shown in Fig. 4.9. Line-to-line voltages (v_{uv}, v_{vw}, v_{wv}) are transformed into the dq components, then the PI controller acts for keeping $v_{LL,q} \simeq 0$, while $v_{LL,d}$ is not used. Moreover, a feed-forward contribution to the frequency (ω_{FF}) is added to the PI output, helping the PLL to converge onto the grid frequency (close, but not always exactly equal, to 50 Hz). Finally, the angle θ_{LL} is obtained as integration of the frequency. This is in phase with the direct component of line-to-line voltages ($v_{LL,d}$), thus with v_{uv}. From the vectorial diagram of three-phase

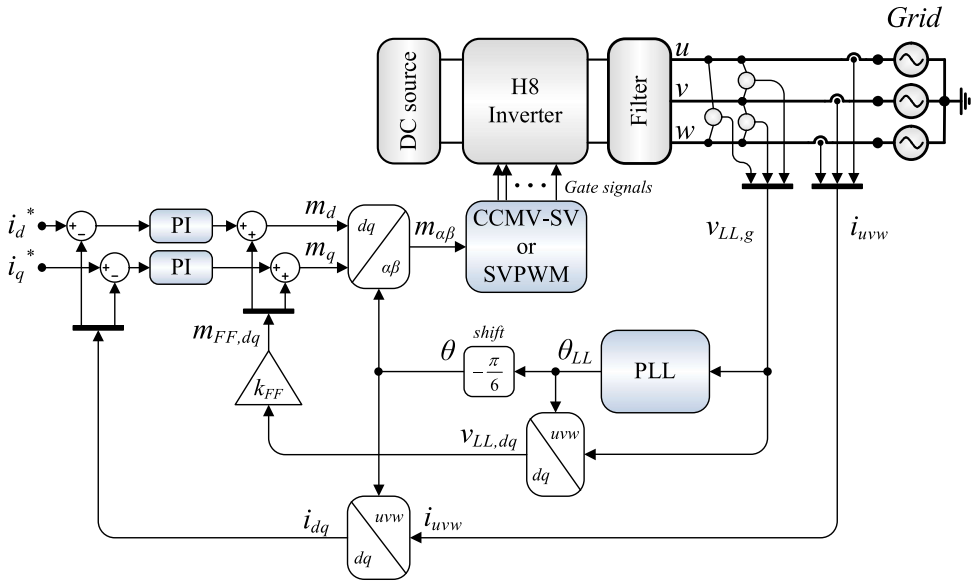


Figure 4.8: Control scheme, grid-connected output.

voltages, it can be observed that the angle θ in phase with the u-line voltage is

$$\theta = \theta_{LL} - \frac{\pi}{6} \tag{4.11}$$

For this reason, a "shift" block is introduced in the control scheme of Fig. 4.8.

The modulator performs CCMV-SV or SVPWM modulation described in Sec. 4.4, depending on the modulation magnitude. The change of strategy is executed across the threshold of 0.5, with a hysteresis window of 0.05.

It is worth to be noted that there are eight gating signals from the modulator to the inverter, not six like in traditional three-phase converters, because of the presence of the two additional DC-decoupling devices that need to be independently controlled.

4.6 Simulations

A model of the inverter has been designed with the toolbox PLECS®, allowing to develop and test the H8 features in a MATLAB®/Simulink® control environment.

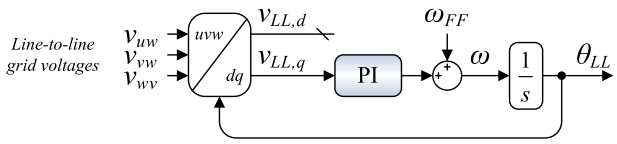


Figure 4.9: Block scheme of the PLL.

Simulations were carried out to develop and verify the proposed architecture and modulation; electro-thermal simulations were also carried out for evaluating the impact of the DC-decoupling hardware on the efficiency and the harmonic content at the inverter output. Simulation modalities and results are hereinafter presented.

4.6.1 Electric simulations

As the purpose of this work is to present the novel inverter architecture along with the proposed modulation strategies, it was introduced a RL load in wye connection $3 \times (L_{f,j} + R_{m,j})$, where $j = 1,2,3$ denotes each line. In this condition, the electrical angle θ was generated with a sawtooth source of frequency f_e, without the necessity of the PLL block (with a RL load there is no grid to synchronize with). In a real implementation with a motor as load, the angle information can come from a transducer, like an encoder or a resolver, or it can be estimated with a sensorless algorithm.

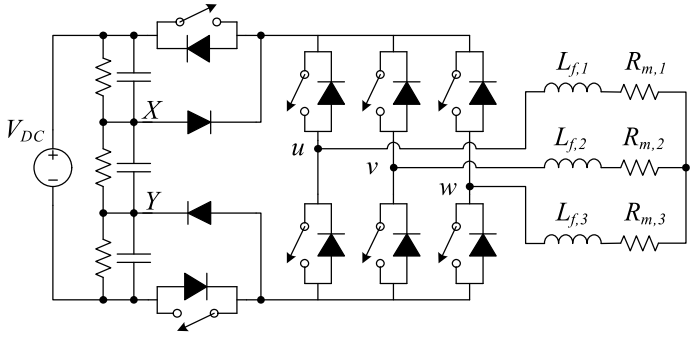
Performance of H8 architecture performing CCMV-SV or SVPWM where compared to those of a traditional H6 structure performing SVPWM. For all the configurations, the same simulation environment was used, with only some minor changes to the inverter or modulation blocks.

The main parameters used for the simulations are given in Tab. 4.3.

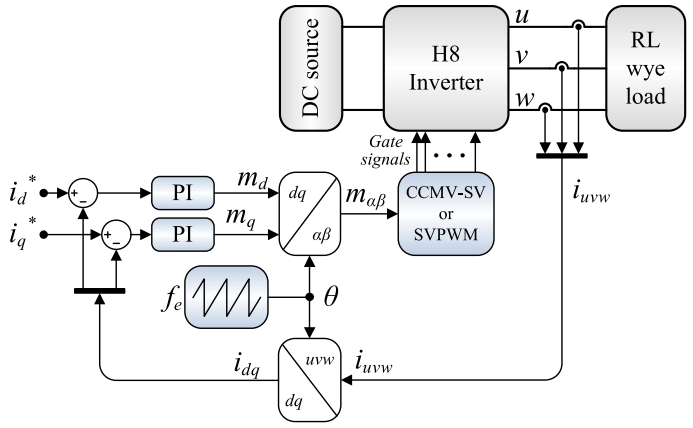
In Fig. 4.11, V_{CM} is shown for the three cases of comparison, normalized to V_{DC}: H6 with SVPWM, H8 with SVPWM and H8 with CCMV-SV. H6 exhibits a V_{CM} varying from 0 to 1 at the switching frequency, with six total transitions of amplitude $1/3$. H8 inverter with SVPWM halves the number of the transitions and limits the excursion within the range from $VDC/3$ to $2VDC/3$. Last, H8 with CCMV-SV performs an almost constant V_{CM} that, depending to the odd or even vector usage, can be equal to $1/3$ or $2/3$. Actually, for the last two cases adopting H8 architecture,

Table 4.3: Simulation parameters

Parameter	Symbol	Value
Supply voltage	V_{DC}	600 V
Switching frequency	f_{SW}	10 kHz
Electrical frequency	f_e	50 Hz
Wye load	$3 \times (L_f + R_m)$	$3 \times (2\,\text{mH} + 10\,\Omega)$



(a)



(b)

Figure 4.10: Simulated scheme. (a) Power network. (b) Overall system configuration.

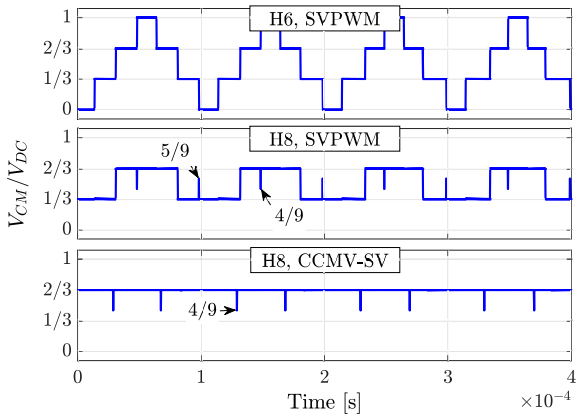


Figure 4.11: CMV evolution over four PWM periods in case of H6 with SVPWM, H8 with SVPWM and H8 with CCMV-SV (even vectors).

V_{CM}/V_{DC} exhibits spikes at $4/9$ and $5/9$, again depending on the odd or even vectors usage. These spikes occur in the transitions from active to inactive states, confirming what discussed in Sec. 4.3. For this comparison, a modulation index $m = 0.5$ was adopted for all the cases.

Figs. from 4.12 to 4.15 show output currents for the same configurations of the system (H6 with SVPWM, H8 with SVPWM and H8 with odd and even CCMV-SV). It can be seen that both H6 and H8 modulated with SVPWM perform substantially the same. Instead, H8 modulated with CCMV-SV exhibit an asymmetrical current ripple for the upper and bottom part of the sinusoid. When even vectors are used (Fig. 4.15) it is bigger on the bottom, while when odd vectors are, the opposite happens. This is consequence of the fact that odd states are characterized by two legs to 0 and one leg to V_{DC}, while, on the contrary, even states have two legs to V_{DC} and one leg to 0. It can be observed that ripple is comparable to that typical of SVPWM only in those portions where it is smaller. Unfortunately, the asymmetrical shape and the increased amount of ripple (on average) over SVPWM, represent relevant drawbacks for CCMV-SV, confirming the premise that reducing CMV does not come free from disadvantages.

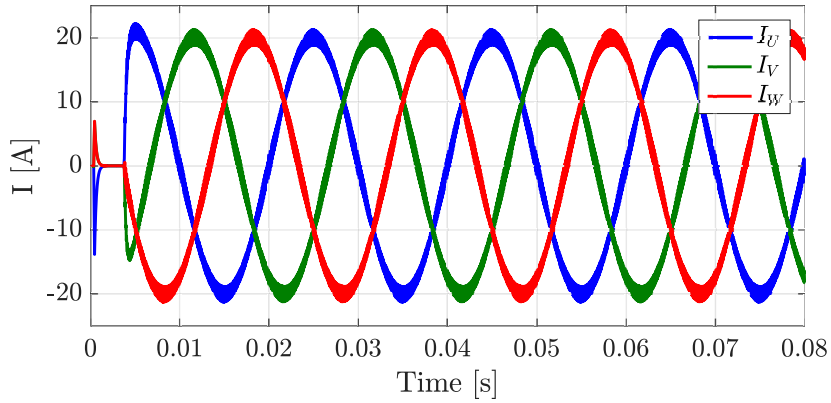


Figure 4.12: Current waveforms for H6 inverter with SVPWM modulation. Reference amplitude is 20 A.

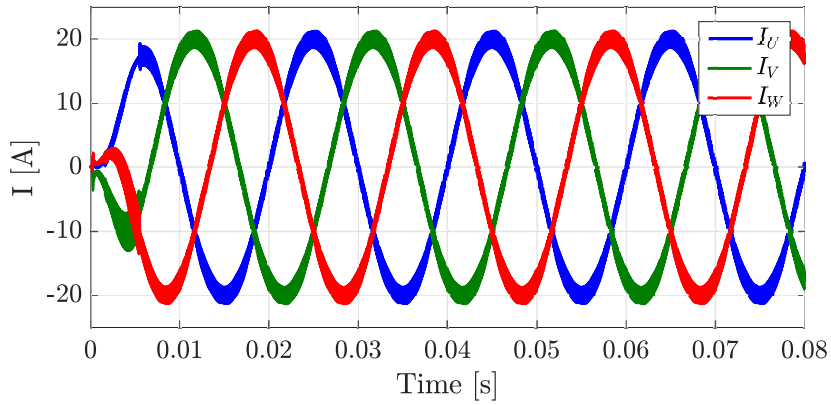


Figure 4.13: Current waveforms for H8 inverter with SVPWM modulation. Reference amplitude is 20 A.

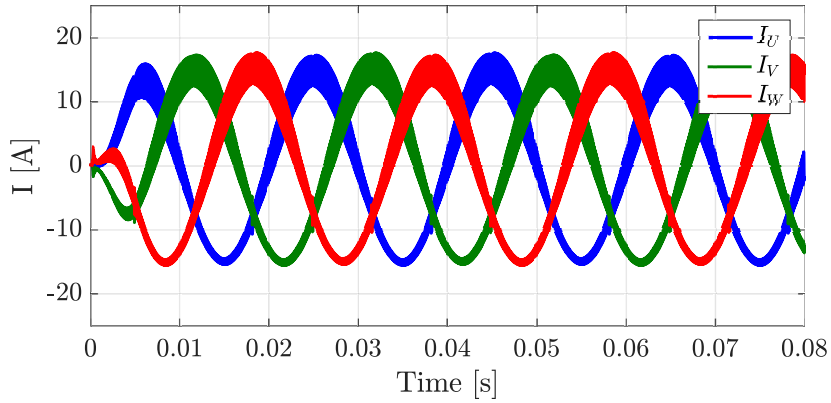


Figure 4.14: Current waveforms for H8 inverter with CCMV-SV modulation using odd vectors. Reference amplitude is 15 A.

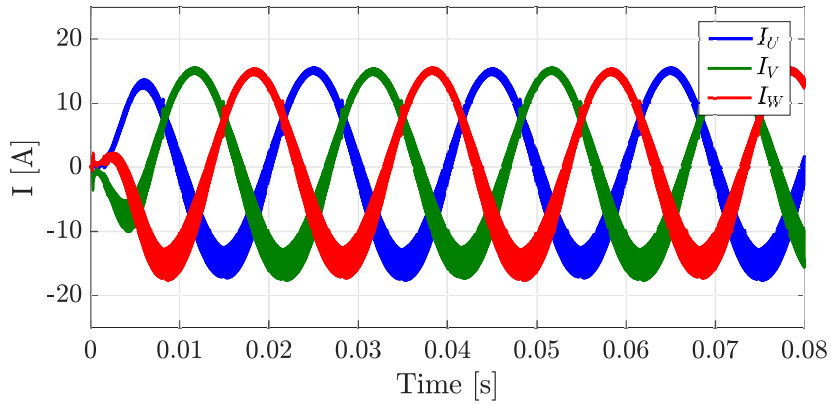


Figure 4.15: Current waveforms for H8 inverter with CCMV-SV modulation using even vectors. Reference amplitude is 15 A.

The spectrum of the output voltage was also investigated. Harmonic content of the common- and differential-mode voltages are depicted in Fig. 4.17 and Fig. 4.18, where the amplitudes of harmonics are normalized respectively to V_{DC} and to the amplitude of the fundamental. It is possible to see how the harmonic content of the CMV is reduced for CCMV-SV over SVPWM of about four decades, while the spectrum of the DMV is in essence the same for all the three examined cases. For this comparison, all simulations were conducted with $m = 0.4$ and for a simulation time of 0.5 s, hence lasting 25 fundamental cycles ($f_e = 50$ Hz).

As expected, another drawback of CCMV-SV consists in the increased distortion of the output voltage. This was investigated evaluating the weighted total harmonic distortion (WTHD), which is expressed as [26]:

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n}\right)^2}}{V_1} \tag{4.12}$$

Figure 4.16 reports WTHD for the two investigated modulations against the modulation index. As expected, CCMV-SV exhibits a bigger output distortion than SVPWM, resulting in a WTHD from 30% to 80% higher, depending on the modulation index. On the other hand, SVPWM exhibits the same WTHD both in case of H6 and H8.

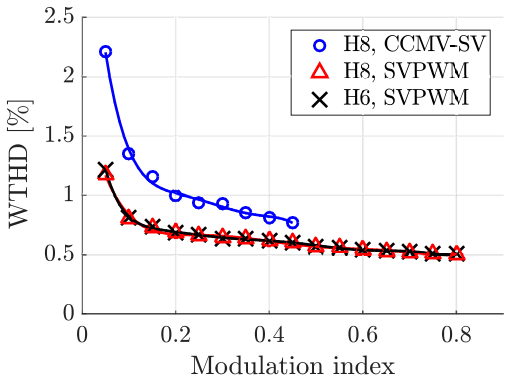


Figure 4.16: WTHD evolution against the modulation index for different configurations of the system.

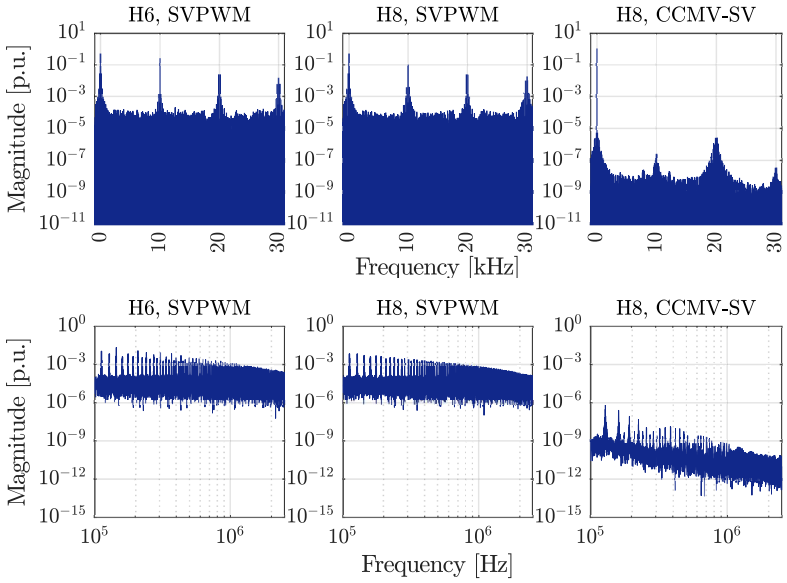


Figure 4.17: FFT of the CMV normalized to the supply voltage.

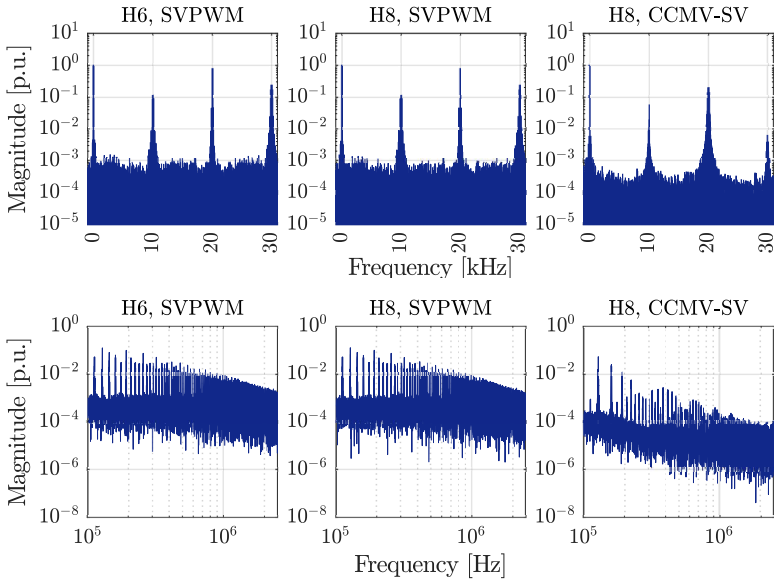


Figure 4.18: FFT of the line-to-line voltage normalized to the fundamental.

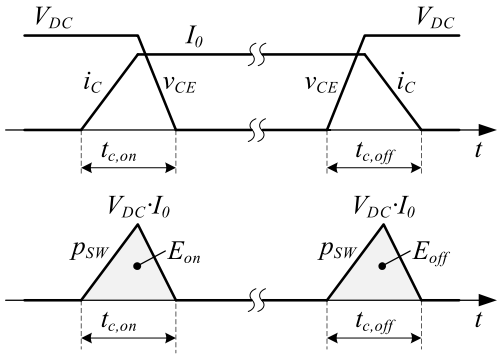


Figure 4.19: Switching losses in an IGBT.

4.6.2 Electro-thermal simulations

As already explained in Section 4.2, the proposed H8 has two additional devices for the decoupling of the DC side, which are inevitably responsible for additional losses. It was important to investigate their impact on the overall efficiency, comparing H8 and H6 in this respect. Electro-thermal simulations were conducted in the Simulink/PLECS environment, were it was possible to embed a model for the switching and conduction losses of power devices (Infineon IKW50N65H5 IGBT). Considering an IGBT with collector current i_C and collector-emitter voltage v_{CE}, during turn-off and turn-on they assume the evolution depicted in Fig. 4.19. Switching losses arise because during turn-on voltage drops only after that current has risen, while, conversely, during turn-off current drops only after that voltage has risen. Also, during conduction some losses are also present, since on-state voltage is not zero. Instantaneous power loss and energy lost during turn-on and turn-off are given by:

$$p(t) = v_{CE}(t) i_C(t) \tag{4.13}$$

$$E_{on} = \int^{t_{c,on}} p(t)\, dt \tag{4.14}$$

$$E_{off} = \int^{t_{c,off}} p(t)\, dt \tag{4.15}$$

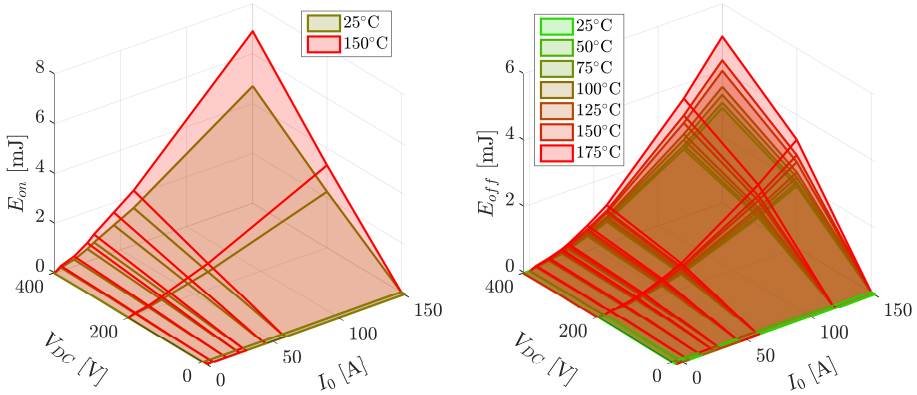


Figure 4.20: Switching losses for Infineon IKW50N65H5 Silicon IGBT.
(a) Turn-on. (b) Turn-off.

Switching losses were modeled through a couple of multidimensional look-up tables, where value of switching energy are tabulated as function of on-state current, off-state voltage and junction temperature. Values were carried out from the device datasheet only for few combinations of current, voltage and temperature. Basing on those values, the simulation tool performs linear interpolation at every simulation step. Figure 4.22 illustrates the performance for three investigated configurations of the system. In particular, comparing the cases involving SVPWM modulation on H8 and H6 allows to evaluate the losses arising from the additional devices on the DC side of the H8 topology. In accordance with expectations, H8 detriments efficiency a little. For example, at $m = 0.4$, it goes from 98.37% with H6 to 97.93% with H8. The worsening is of 0.44% for that value of m and 0.45% on average over the entire modulation range. Furthermore, comparing the cases with the same H8 configuration and the two proposed modulations, it is possible to observe that CCMV-SV performs better than SVPWM, with an efficiency improvement from 0.3% to 1.75% depending on the modulation index.

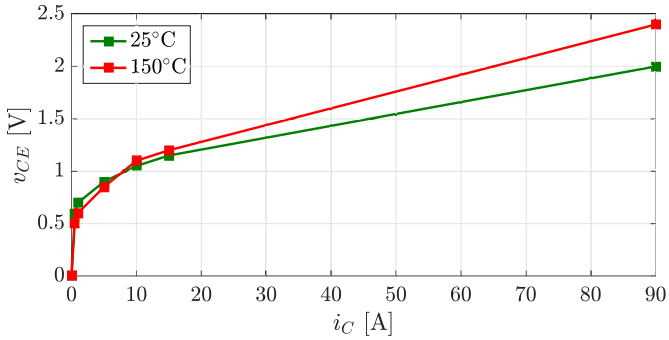


Figure 4.21: Conduction voltage for Infineon IKW50N65H5 Silicon IGBT.

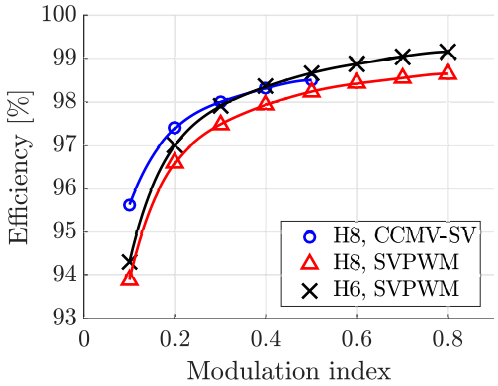


Figure 4.22: Efficiency performance for different combinations of the system.

Table 4.4: Comparison of H8 with different modulations and H6

Topology	H6	H8	H8
Modulation	SVPWM	SVPWM	CCMV-SV
DC clamping	No	Yes	Yes
Maximum mod. index	1	0.866	0.5
CMV	High	Medium	Low
WTHD %	0.5 – 1.25	0.5 – 1.25	0.75 – 2.25
Efficiency	Medium	Low	High

Chapter 5

Converter prototype

5.1 System overview

In order to prove the effectiveness of the H8 architecture and the proposed modulation strategies, a prototype of the converter was designed and built from the ground up. In order to prevent EMI problems control and power circuitry were separated on two different boards, interleaved by an interface card. The overall system setup is schematically shown in Fig. 5.1, it is composed of three separate boards:

- Control board: hosts the microcontroller that performs the SV modulation and the current control.
- Power board: hosts the H8 inverter (gate drivers and switching devices), receives optical gating signals and feeds-back measurements information via current signals.
- Interface board: hosts the conditioning circuitry for the measurements signals and the optical transmitters for the gating signals.

Circuitries of the three boards are supplied by an AC/DC power supply connected to the single phase utility. It is mounted on the Power board and provides a triple voltage output (5 V and $\pm$15 V), distributed throughout the three boards. In the

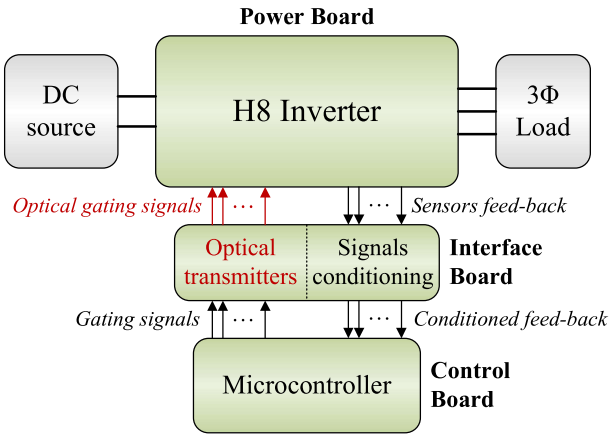


Figure 5.1: Scheme of the three-boards-based experimental setup.

experimental setup, control and Interface boards are arranged in a stack, as shown in Fig. 5.2, while Power board is positioned separately, as shown in 5.4.

Beside the boards, test bed included a commercial DC power supply and a wye connected RL load.

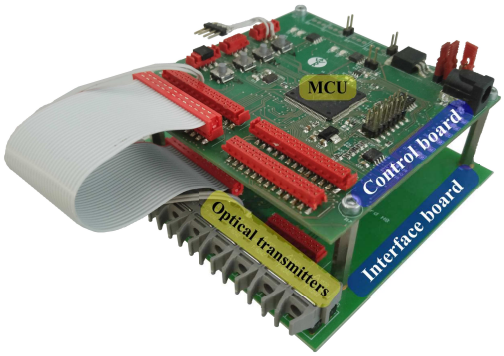
Each portion of the system is more accurately described in the following.

5.1.1 Control board

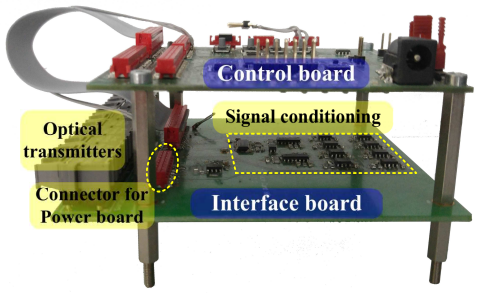
The adopted control board is features a Freescale® MPC5643L®, a 120 MHz, 32 bit microcontroller unit. Four PWM channels are dedicated to the control of the eight switching devices of the H8 inverter, 8 Analog to Digital Converter (ADC) channels acquire the conditioned measurement signals.

Control board also embeds a 3.3 V voltage regulator, the protection circuit for the ADC, communication peripherals (CAN, UART) and other minor elements (buttons, switches and LEDs). A 26-ways ribbon cable connects the logic to the Interface board, carrying control, feed-back and supply signals. A perspective view of the board is given in Fig. 5.2(a).

It is worth to mention that this is a general-purpose board, therefore some of its functionalities and peripherals are not exploited for this project.



(a) Perspective view.



(b) Side view.

Figure 5.2: Control and Interface boards in the stacked arrangement.

5.1.2 Interface board

The Interface board serves as a bridge between the Control and the Power ones.

Gating signals from the microcontroller are converted into optical binary signals (light = ON, dark = OFF) and transmitted to the Power board by means of 10 optical fibers (1 global enable, 8 for gates and 1 for output relays).

Each of the eight current-based signals coming from LEM® transducers (from the Power board) are conditioned by means of a two-stages circuitry, shown in Fig. 5.3.

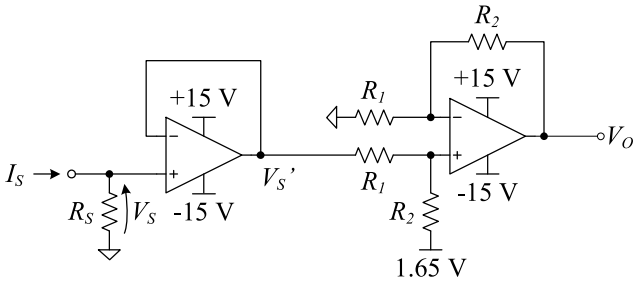


Figure 5.3: Signal conditioning circuit.

The first conditioning stage converts the current signal I_S coming from the sensor into a buffered voltage V_S' by means of the resistor R_S. The second stage is an adder with gain that outputs V_O which is in turn acquired and converted from the ADC interface on the Control board. For current sensors, $I_S \in [-50\,\text{mA}, 50\,\text{mA}]$, while for voltage sensors (which also output current-based signals) $I_S \in [-25\,\text{mA}, 25\,\text{mA}]$. Resistance R_S was chosen so to produce $V_S \in [-2.5\,\text{V}, 2.5\,\text{V}]$, hence:

$$R_S = \frac{V_{S,MAX}}{I_{S,MAX}} = \begin{cases} \dfrac{2.5}{50 \cdot 10^{-3}} = 50\,\Omega & \text{for current sensors} \\ \dfrac{2.5}{25 \cdot 10^{-3}} = 100\,\Omega & \text{for voltage sensors} \end{cases} \tag{5.1}$$

Output voltage V_O must be in the ADC interface range, from 0 V to 3.3 V, so an offset voltage equal to 1.65 V is adopted as well as a gain $G_S = R_1/R_2$. The conditioned signal is given by:

$$V_O = V_S' \cdot G_S + 1.65 \tag{5.2}$$

Hence, the gain must be:

$$G_S = \frac{V_{O,MAX} - 1.65}{V_{S,MAX}'} = \frac{3.3 - 1.65}{2.5} = 0.66 \tag{5.3}$$

For resistors R_1 and R_2, conservative values of 10.39 kΩ and 6.2 kΩ were chosen, leading to a gain of 0.5957, a bit smaller than the theoretical 0.66. In practice R_1 was made by the series of two resistors of 10 kΩ and 390 Ω.

As said, eight sensors are present on the Power board, so the described circuit is replied eight times on the Interface board. In addition, a fault circuit is present and makes use of a SR latch that is set in case of overcurrent. The fault signal is acquired in the MCU that disables the modulation when a logic 1 is detected.

5.1.3 Power board

The Power board hosts the H8 inverters with their driving circuits and the DC link divider. The numerousness of the sections on the board is summarized in Tab. 5.1, where values in brackets represent additional elements. In fact, the board was designed for implementing the H8 inverter as well as a four-legs inverter. For this reason, the layout embeds four switching legs, moreover some 0 Ω elements make possible to short-circuit the DC-decoupling network for implementations different from the H8. However, in this version of the board, implementing H8, the fourth leg is not used at all. Fig. 5.4 depicts the Power board as it appears in the three-boards system, with the main portion of the circuitries highlighted for ease of comprehension.

Table 5.1: Numerousness of the sections on the Power board. Values in brackets represent additional elements, available for implementing a four-legs inverter.

Description	Count
AC/DC supply	1
Optical receivers	10 (+2)
Isolated supplies	6 (+1)
Gate drivers	10 (+2)
Power switches	10 (+2)
Current sensors	3
Voltage sensors	5
Output relays	3 (+1)

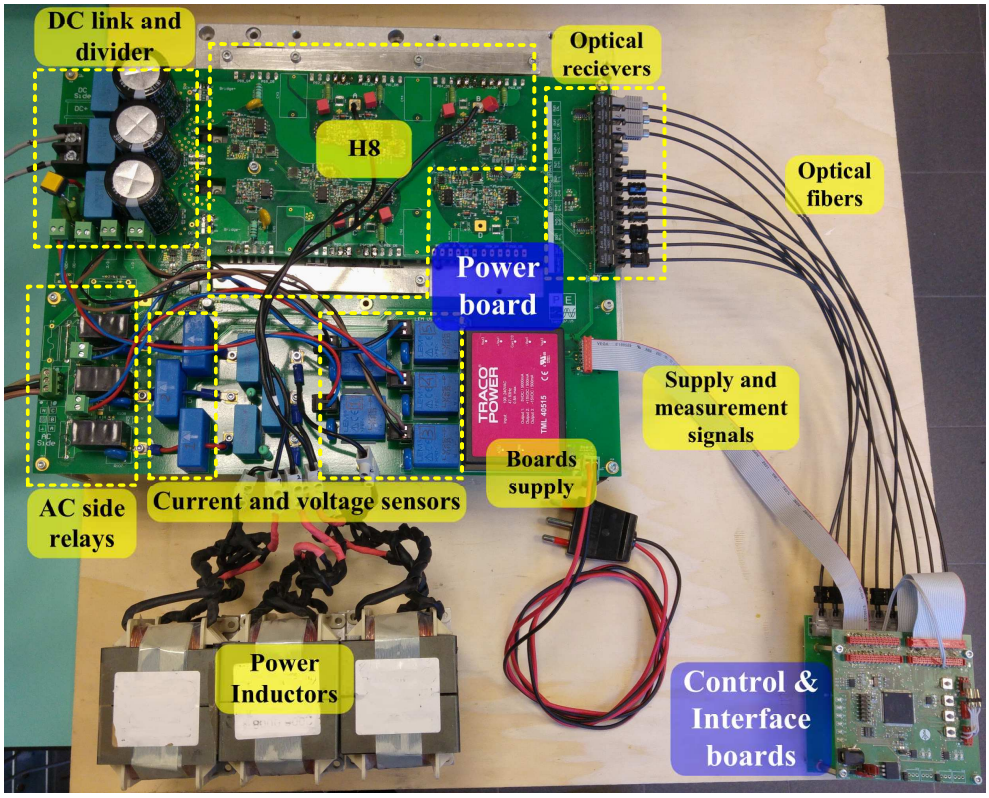


Figure 5.4: System setup with the three boards.

Supply

The Power board hosts a TRACO POWER TML 40515, an encapsulated AC/DC power supply connected to the single phase utility, which provides a triple voltage output, that supply all the circuitries throughout the three boards. The output voltage levels and their usage are:

- +5 V (5 A): control and interface boards, insulated supplies, optical receivers.
- +15 V (0.5 A): LEM sensors, output relays.
- −15 V (0.5 A): LEM sensors.

Insulated supplies

Each of the six insulated power supply is generated by the IC MAX256® that drives a 1:2.5 transformer followed by a voltage multiplier and an adjustable voltage regulator (the LP2954 from Textas Instruments). Voltage multiplier is composed by two capacitors of 220 nF and 1 µF and two Schottky diodes. Regulation of the output voltage is made by tuning an external resistor R_{FB} between the positive output and the FB pin. On the datasheet of the components, the following expression for the output voltage is given:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_2}\right) + I_{FB} \cdot R_{FB} \tag{5.4}$$

Where R_2 is another external resistor between FB pin and the reference ground GND, V_{REF} is the 1.23 V reference voltage and I_{FB} is the FB pin bias current (typically −20 nA). Also, R_2 is suggested to be 100 kΩ for reducing the output error to minimum.

Feedback resistor must be chosen in accordance to the desired output voltage as:

$$R_{FB} = (V_{OUT} - V_{REF}) \cdot \frac{R_2}{V_{REF} + I_{FB} R_2} \tag{5.5}$$

That, given the reported values, becomes:

$$R_{FB} = V_{OUT} \cdot 81\,433\,\mathrm{A}^{-1} - 100.16\,\mathrm{k}\Omega \tag{5.6}$$

For values of the output voltage between 15 V to 20 V, R_{FB} values must be in the range from 1.1 MΩ to 1.5 MΩ.

A simplified drawing of the circuit is illustrated in Fig. 5.5. It must be noted that the same circuit is replied six times in the Power board: two for the DC-decoupling devices, one for all the low-side devices and three for the high-side devices.

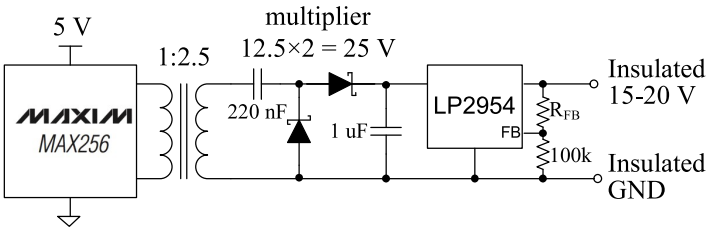


Figure 5.5: Simplified drawing of the insulated power supply circuit.

Gate drivers

For a flexible and independent control of power devices, each of them has its own gate driver fed by the insulated power supply described above. The circuit adopts an optocoupler (Allegro ACPL-3180) plus an additional network for the Miller clamp. Each PWM signal generated by the MCU is gated through a logic AND with an Enable signal. The logic gate is in open drain configuration, so a pull-up resistor connected to 5 V supply is necessary to feed the photodiode of the optocoupler. Moreover, for avoiding it to turn-on in case of malfunctioning of the AND gate, the conduction path is controlled by a BJT connected to the Enable too.

On the insulated side of the gate driver, beside the gate resistor, a network composed by complementary N/P mosfet inverts the gate-driving signal and drives a further N-MOSFETs with very low on-resistance dedicated to the active Miller Clamp function. This addition to the gate drive prevents the power device to turn-on because of the Miller capacitor when the complementary device in the leg turns on.

For ease of comprehension, Fig. 5.6 shows the gate-driver circuit in a simplified fashion, while full schematic is reported in App. A.

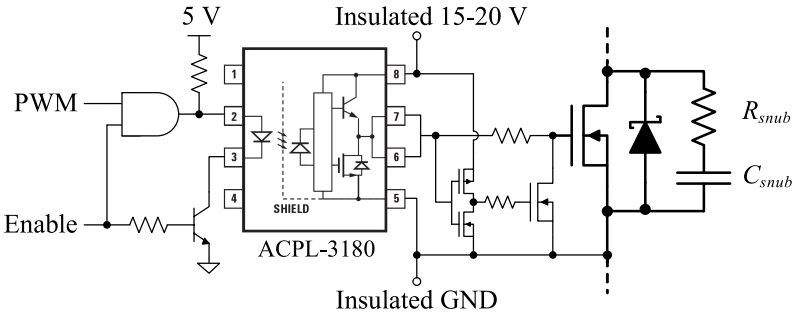


Figure 5.6: Gate driver circuit and power device section.

Power section

The power section embeds the H8 structure, realized with discrete TO-247 power devices. Both IGBTs and MOSFETs can be adopted, provided that insulated supplies are tuned for the appropriate gate voltage, as explained above. In particular, two types of devices were mounted and tested on the board:

- 650 V, 50 A Silicon IGBTs (Infineon IKW50N65H5)
- 1200V, 80 A SiC MOSFETs (Cree C2M0080120D)

Additional anti-parallel discrete diodes in TO-247 package are also mounted in parallel to each device, assisting internal diodes of power switches. The chosen model is the CVFD20065A, a SiC Schottky diode from Cree. In Fig. 5.6 a power MOSFET is depicted as case of example.

In order to reduce ringing after commutations, a RC snubber is present for each device. The snubber was designed following the practical procedure described in [27]. Total parasitic inductance L_{parass} due to tracks and package can be estimated from the ringing arising without the snubber.

$$L_{parass} = \frac{T_{RING}^2}{4\pi^2 C_{parass}} \tag{5.7}$$

Where T_{RING} is the period of the observed ringing and C_{parass} represents a good estimation of the stray capacitance that rings with L_{parass}, derived from the sum of the PCB capacitance and the output capacitance of the power device.

Considering that the optimum value of the snubber resistor R_{SNUB} must equal the characteristic impedance of the LC circuit, it can be derived as:

$$R_{SNUB} = \sqrt{\frac{L_{parass}}{C_{parass}}} \tag{5.8}$$

The snubber capacitor C_{SNUB} comes from a trade off between overdamping (for larger values) and little power losses (for smaller values). As a rule of thumb, a good practice is to set the snubber time constant $\tau_{SNUB} = R_{SNUB}C_{SNUB}$ equal to three times the ringing period. It follows that:

$$\tau_{SNUB} = R_{SNUB}C_{SNUB} = 3 \cdot T_{RING} \tag{5.9}$$

Which leads to the optimal value of the snubber capacitor:

$$C_{SNUB} = 3\frac{T_{RING}}{R_{SNUB}} \tag{5.10}$$

Ultimately, resistor package must be chosen so to handle the power exchanged by the capacitor that, considering the supply voltage V_{DC} and the switching frequency f_{SW}, is:

$$P_{SNUB} = \frac{1}{2}C_{SNUB}V_{DC}f_{SW} \tag{5.11}$$

From the described process applied to the realized power board, the following values were derived: $T_{RING} = 92\,\text{ns}$, $C_{parass} \approx 150\,\text{pF}$, $L_{parass} \approx 1.4\,\text{nH}$, $R_{SNUB} = 98\,\Omega$, $C_{SNUB} = 2.8\,\text{nF}$. Actually, for reducing the power dissipation, a smaller capacitance was adopted. Finally, the snubber was chosen with $C_{SNUB} = 1\,\text{nF}$ and $R_{SNUB} = 100\,\Omega$.

DC-link divider and DC-decoupling

Resistive divider was designed splitting each of the three resistance into three 0.125 W resistors in series, for a total of nine resistors. The power loss for the total divider is $P_{DC,MAX} = 9/8 = 1.125$ W. Considering $V_{DC,MAX} = 900V$, resistive value must satisfy:

$$R_{DC} \geq \frac{V_{DC,MAX}^2}{3P_{DC,MAX}} = \frac{900^2}{3 \cdot 1.125} = 240\,\text{k}\Omega \tag{5.12}$$

Hence, each resistor must be greater than one third of that, i.e. 80 kΩ. The value of 91 kΩ was chosen, which produces in a dissipated power equal to:

$$P_{DC} = \frac{V_{DC}^2}{9 \cdot 91 \cdot 10^3} \tag{5.13}$$

In the worst case of $V_{DC} = 900$ V, P_{DC} results equal to 0.989 W.

Regarding the capacitors in parallel to the resistive divider, they are 400 V electrolytic capacitors with a value of 1 µF each, as common practice in converter of this size.

Clamping diodes D_H and D_L are SiC Schottky diodes CVFD20065A from Cree in TO-220 package. Forward voltage is in the range from 1.35 V to 1.8 V, depending on the working conditions.

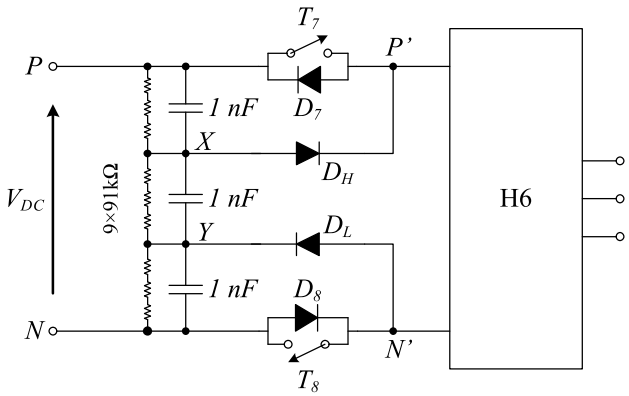


Figure 5.7: DC-link divider and DC-decoupling circuit.

Output stage

The AC output stage of the system includes, for each phase, the filter inductor L_f, a current sensor, a blocking relay and finally a fuse, as depicted in Fig. 5.8.

Relays of the three phases are controlled by one same enabling signal, generated from the MCU and transferred by the Interface card on a dedicated optic fiber. The driving circuit for the relay is composed by a pull-up resistor to 5 V, a BJT to ground and a freewheeling diode.

Current sensors are LEM LA 55-P, 50 A closed loop (compensated) current transducers using the Hall effect. They output a current signal proportional to the measured current, with a 1:1000 transformation ratio.

Regarding the filters, a LC filters with damping resistors is adopted. Another possibility would be a LCL filter: for more versatility, the prototype board has contacts for floating inductors that must be placed next to the board itself, so it is suitable for the addition of another triple of inductors between the delta-RC and the current sensors. As said, the realized system employs the LC configuration. Inductors L_f have a value of 2 mH, but they are actually composed by the series of two 1 mH 12 Arms inductors. The $C_f + R_d$ filter is composed by three 5 µF film capacitors in series with 2.7 Ω damping resistors. They are connected to the floating inductors in delta, as shown in Fig. 5.9.

Finally, three external power resistors R_m are connected at the output connectors. The RL load is indeed composed by L_f and R_m.

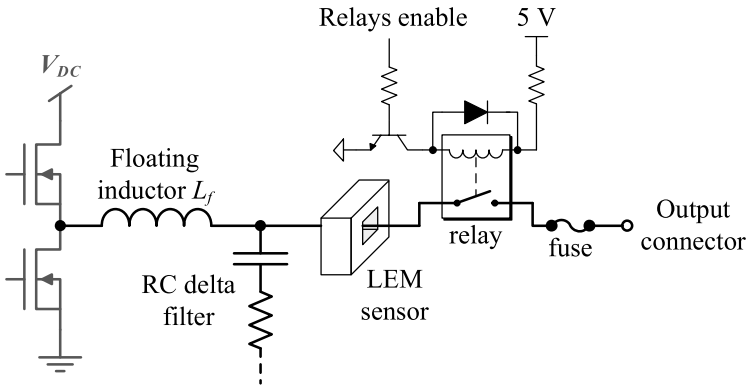


Figure 5.8: Output stage of one phase.

5.2 Experimental results

In order to prove simulation results, the same three operational configurations of simulations (also summarized in Tab. 5.2) were stressed in experimental tests. Fig.

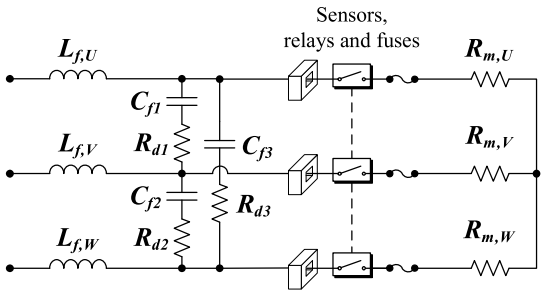


Figure 5.9: Overall output stage with the delta RC filter.

5.10 presents current waveforms both in for H8 performing SVPWM, with a fixed modulation index of 0.6, and in case of H8 with CCMV-SV with a fixed modulation index of 0.25. In the latter, the change in the current ripple behavior at every zero-crossing of the rotational angle is caused by the CCMV-SV modulation changing from odd to even vectors and vice versa. Moreover, in the CCMV-SV case the current ripple results to be higher than the SVPWM case. This is caused by two factors: CCMV-SV performs worse than SVPWM regarding this aspect, DC source voltage in the second testbed was twice that in the first one.

Fig. 5.11 shows the reduction in V_{CM} for H8 over H6 and for CCMV-SV over SVPWM. Plots present the voltage probed with an isolated differential probe between the neutral point of the load and the negative terminal of the DC supply. In the lower part of each figure, electrical angle is depicted too. Globally, V_{CM} evolution results coherent with theory and simulations. For H6 with SVPWM, V_{CM} varies in the range from 0 to V_{DC} at the PWM frequency (Fig. 5.11(a)). For H8 with SVPWM, the excursion is reduced to the range from $V_{DC}/3$ to $2V_{DC}/3$ (Fig. 5.11(b)); finally H8 with CCMV-SV produces a V_{CM} varying between $V_{DC}/3$ and $2V_{DC}/3$ only once every rotational period, when the system changes between odd and even vectors (Fig. 5.11(c)), and exhibiting only small spikes around those main levels.

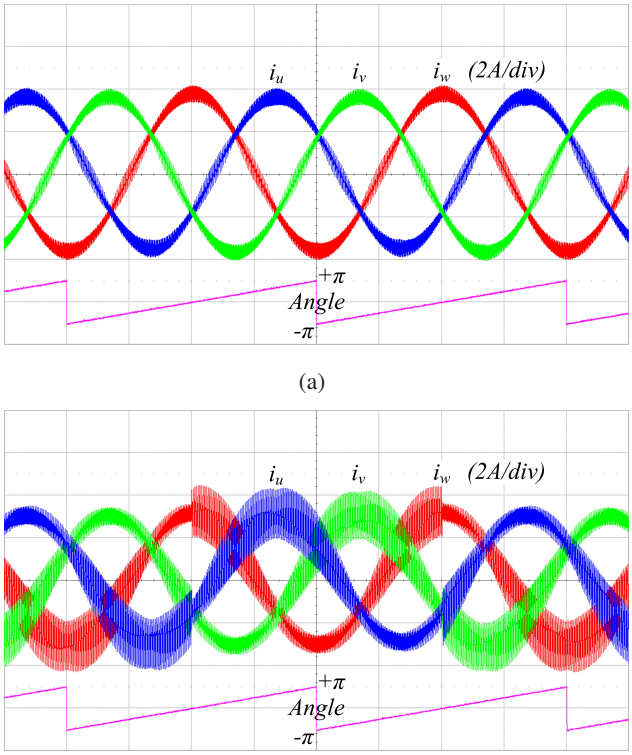
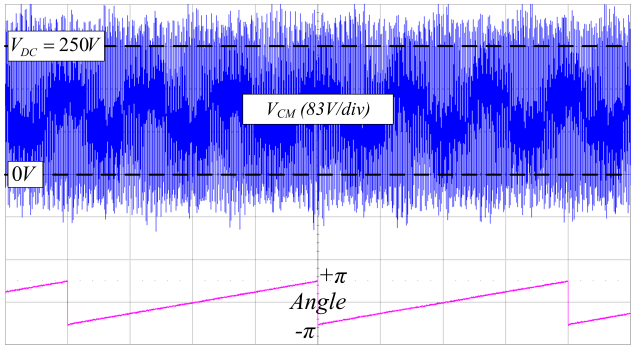
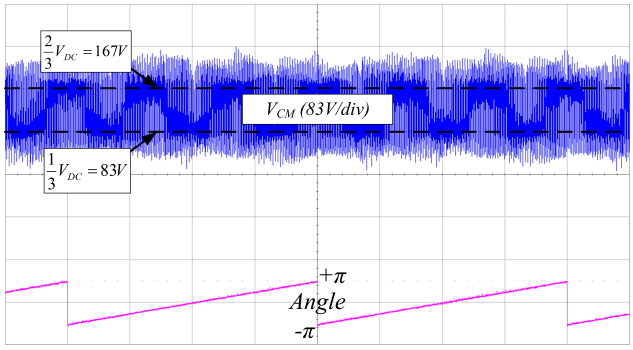


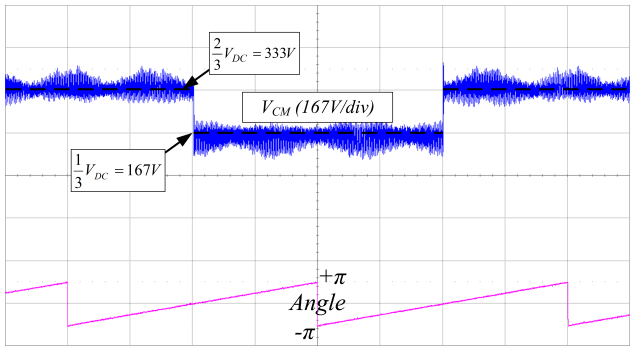
Figure 5.10: Current waveforms for the H8 prototype (blue, green and red) and evolution of the rotational angle (magenta) for two test cases: (a) SVPWM, $V_{DC} = 250\,\text{V}$, $m = 0.6$; (b) CCMV-SV, $V_{DC} = 500\,\text{V}$, $m = 0.25$. Time scale is 5 ms/div.



(a)



(b)



(c)

Figure 5.11: Evolution of CMV and electrical angle for (a) H6 performing SVPWM, $V_{DC} = 250\,\text{V}$; (b) H8 performing SVPWM, $V_{DC} = 250\,\text{V}$; (c) H8 performing CCMV-SV, $V_{DC} = 500\,\text{V}$. Time scale is 5 ms/div.

Table 5.2: Experimental test cases

	1	2	3
Topology	H6	H8	H8
DC decoupling	No	Yes	Yes
Modulation	SVPWM	SVPWM	CCMV-SV
Mod. index m	0.6	0.6	0.25
V_{DC}	250V	250V	500V
f_{SW}		$10kHz$	
f_e		$50Hz$	
Wye load		$3 \times (10\Omega + 2mH)$	

Chapter 6

Conclusions

In this work of thesis, a transformerless three-phase voltage-source inverter with reduced CMV was developed. The project was aimed by the importance taken on by the reduction of the CMV in grounded applications employing transformerless converters. Indeed, inconveniences related to the CMV represent such a significant aspect that a lot of research was conducted over the years trying to remedy them both in the industry and in academia. A survey of the major transformerless three-phase solutions is reported in the thesis with considerations about effectiveness and complexity of each one.

Other than for the hardware architecture, also modulation assumes great importance in the mitigation of CMV. The most effective solutions in this respect were investigated and the most attractive ones were reported in the thesis. Considerations on advantages and drawbacks of each one were also given.

Since this work was not oriented to one particular application from the beginning, photovoltaic generation and controllable motor drives were mentioned as the main field of applicability and the main aspects related to both these fields were exposed.

The developed architecture, addressed as “H8”, is based on the idea of decoupling DC and AC sides of the inverter during freewheeling states. Two switching devices are added to the classical three-phase bridge, for a total of eight, and a couple of clamping diodes is responsible for fixing the CMV during those periods.

A space-vector modulation was developed too, with the aim of keeping CMV as constant as possible. State sequences were thought out for satisfying multiple goals, like constant CMV, single-leg commutations and practical feasibility, also considering the presence of two additional decoupling devices. Limitations and advantages introduced by the H8 topology in this respect were analyzed and reported. Given the strict limitation in the linearity range, a second, more traditional, space-vector modulation was also adopted as extension of the first one when necessary.

Simulations were conducted to verify the functioning of the H8 inverter together with the developed double space-vector modulation. Results confirmed the capability of the system reducing the CMV excursions. Performance comparisons among three main configurations were conducted and reported in the thesis, revealing the benefits that come with the H8 architecture and with the developed modulation. Electro-thermal simulations were conducted too, for investigating the losses introduced by the two additional devices. Switching and conduction losses of a commercial power device were modeled via multi-dimensional LUTs. Comparisons put in evidence that the additional devices do detriment efficiency, but with a still tolerable impact.

A prototype of the converter was designed and realized. Experimental results confirmed simulations regarding synthesization of current waveforms, reduction of CMV and efficiency deterioration over traditional three-phase converters.

Future works, following the work of this thesis, may regard:

- A real-time control of the DC-link divider able to adapt the leading time of DC-decoupling devices for balancing the three-level voltage divider on the DC side.
- A cost evaluation of a commercial product based on the H8 inverter.
- A study on the impact of different semiconductor technologies on the performance of this architecture, also considering wide-bandgap materials like silicon carbide and gallium nitride.

Appendix A

Prototype schematics and layout

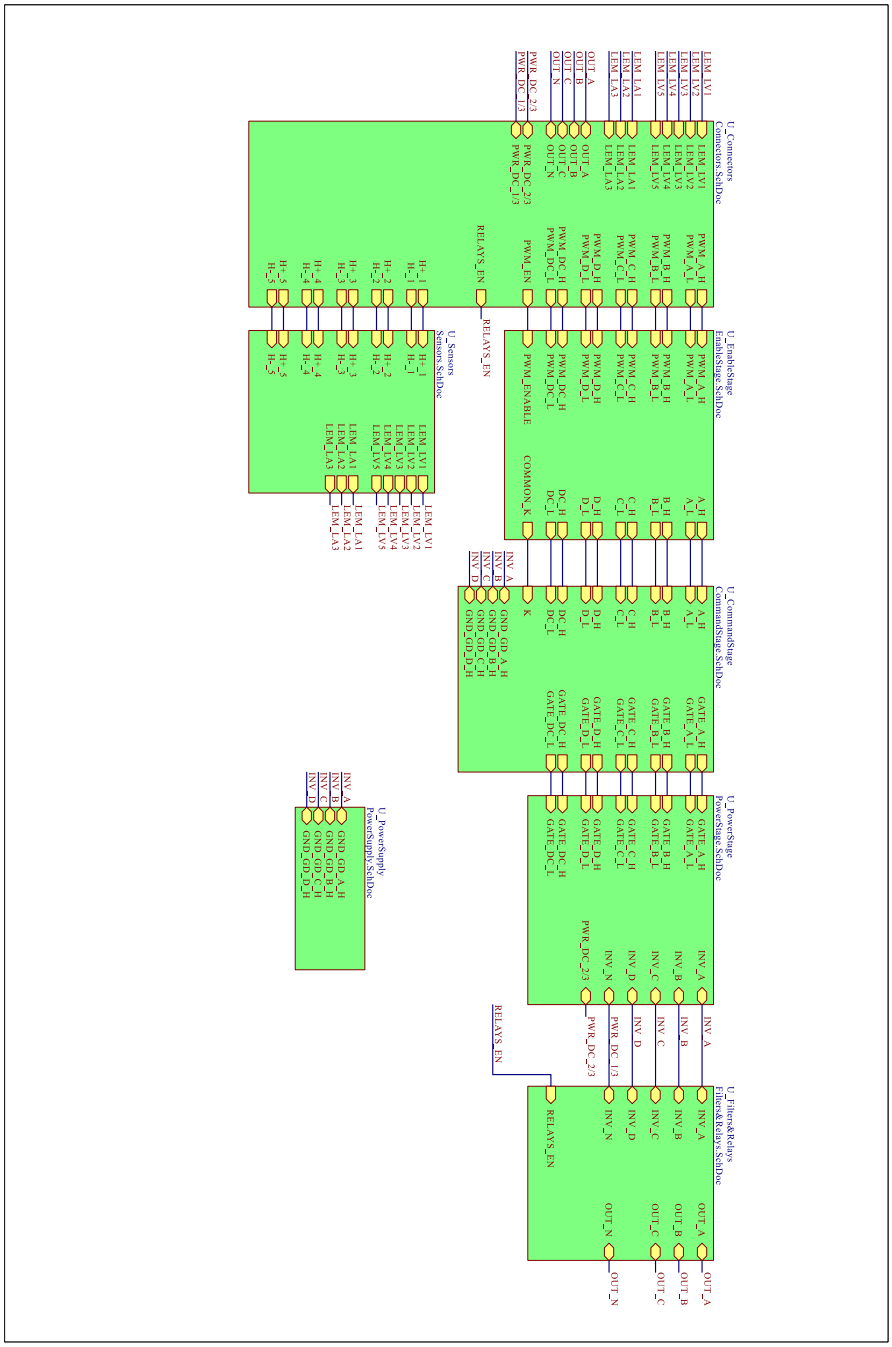


Figure A.1: Top Level.

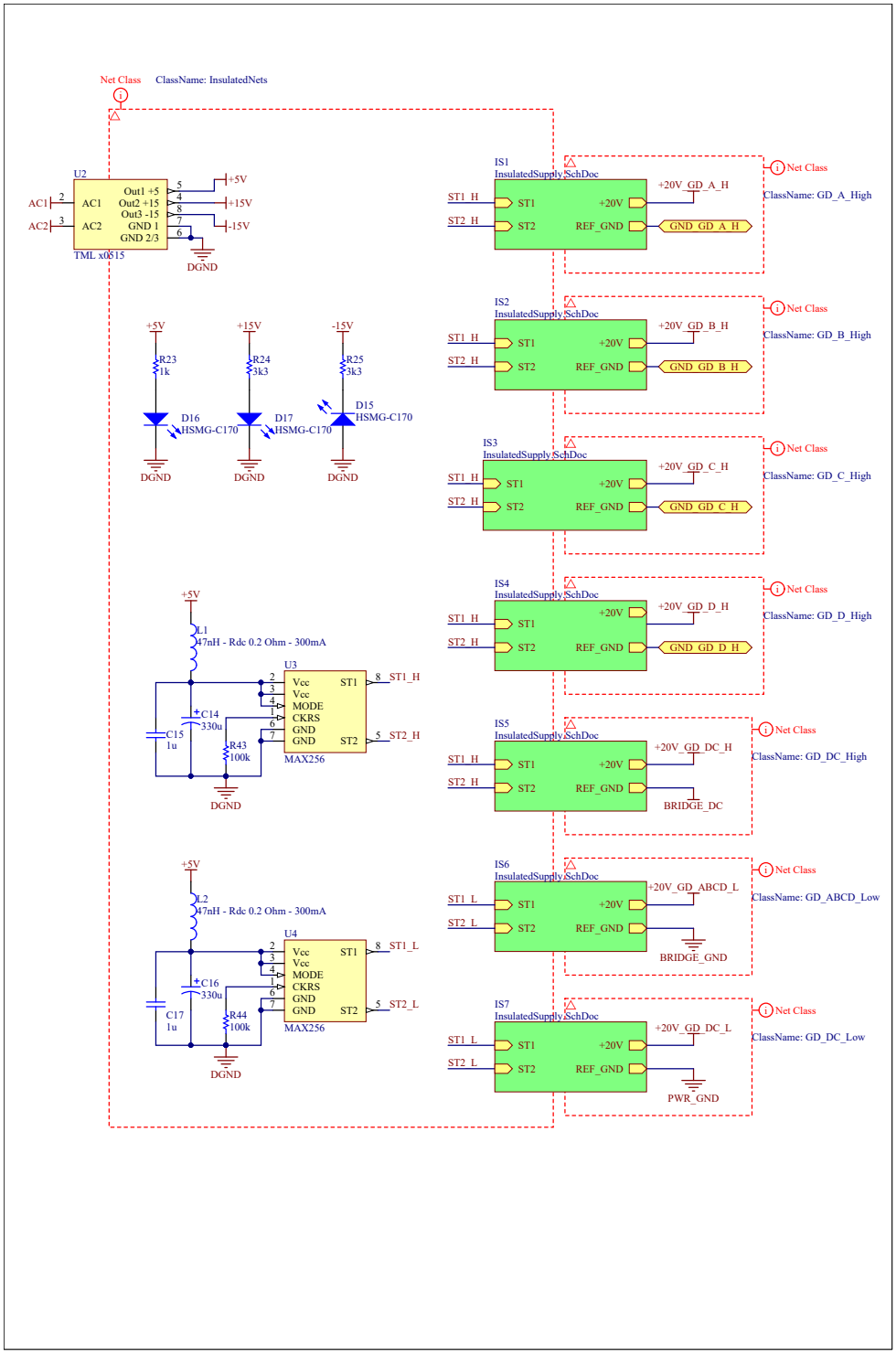


Figure A.2: Power supply.

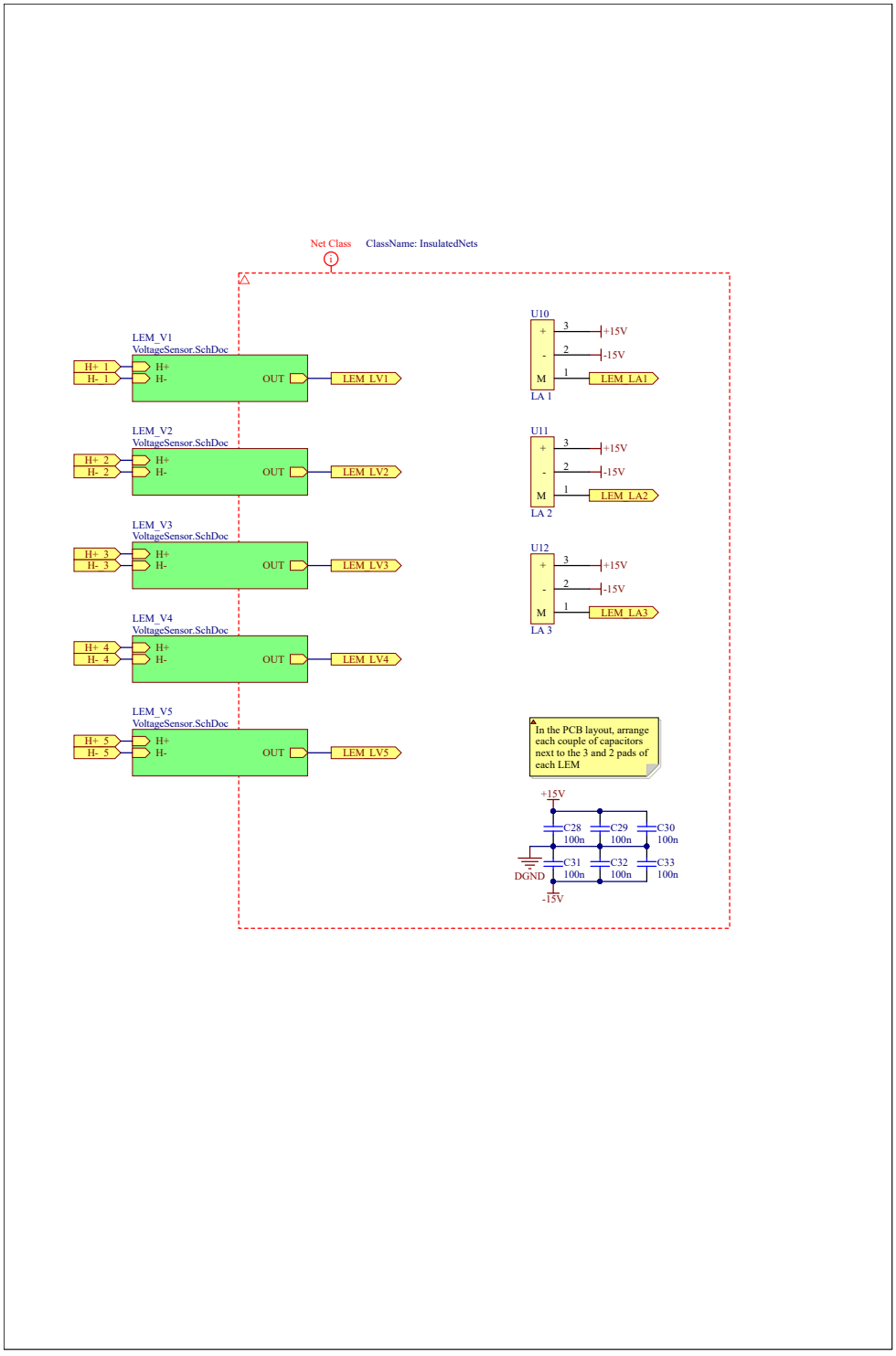


Figure A.3: Sensors.

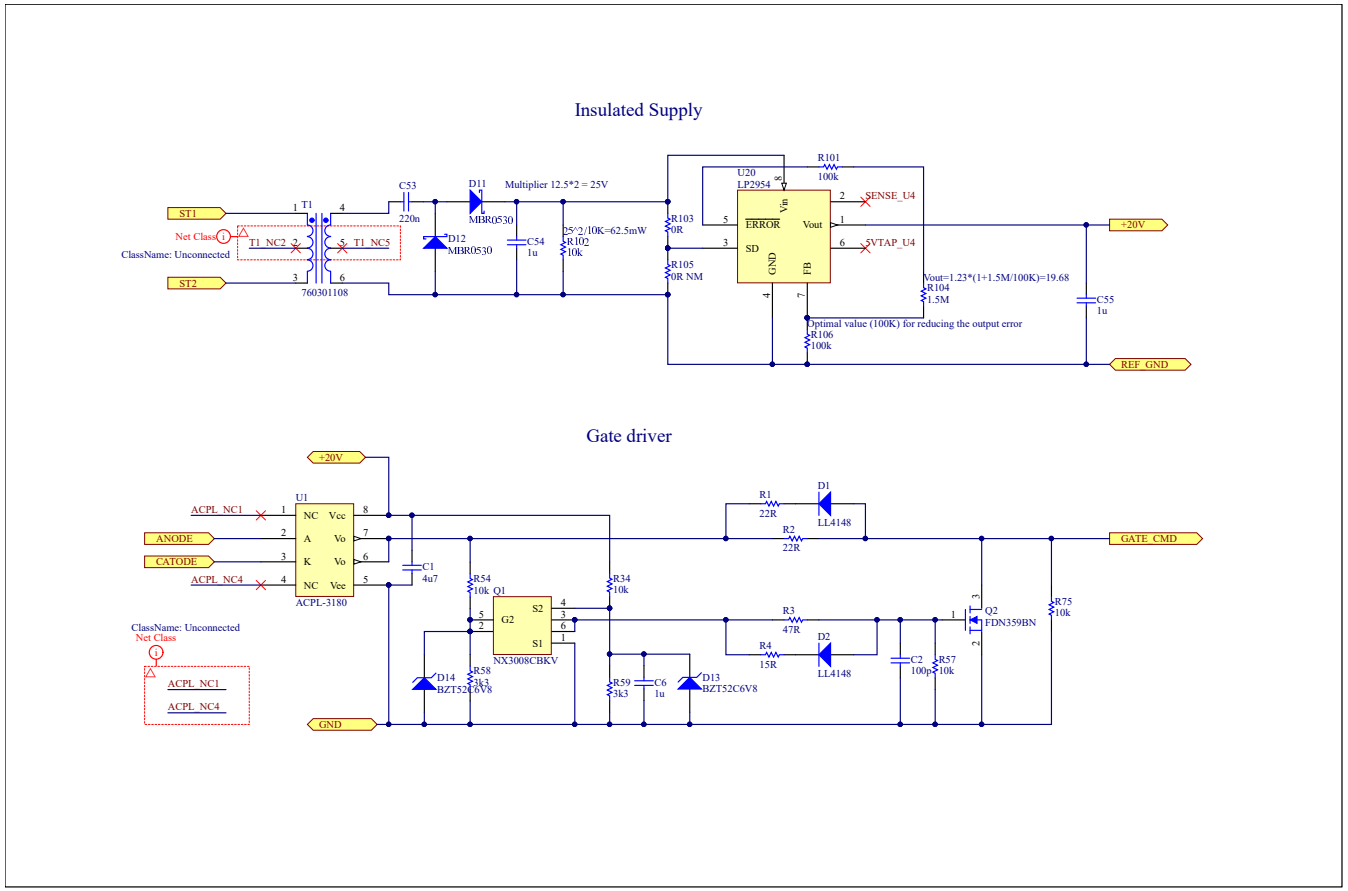


Figure A.4: Insulated supply and gate driver.

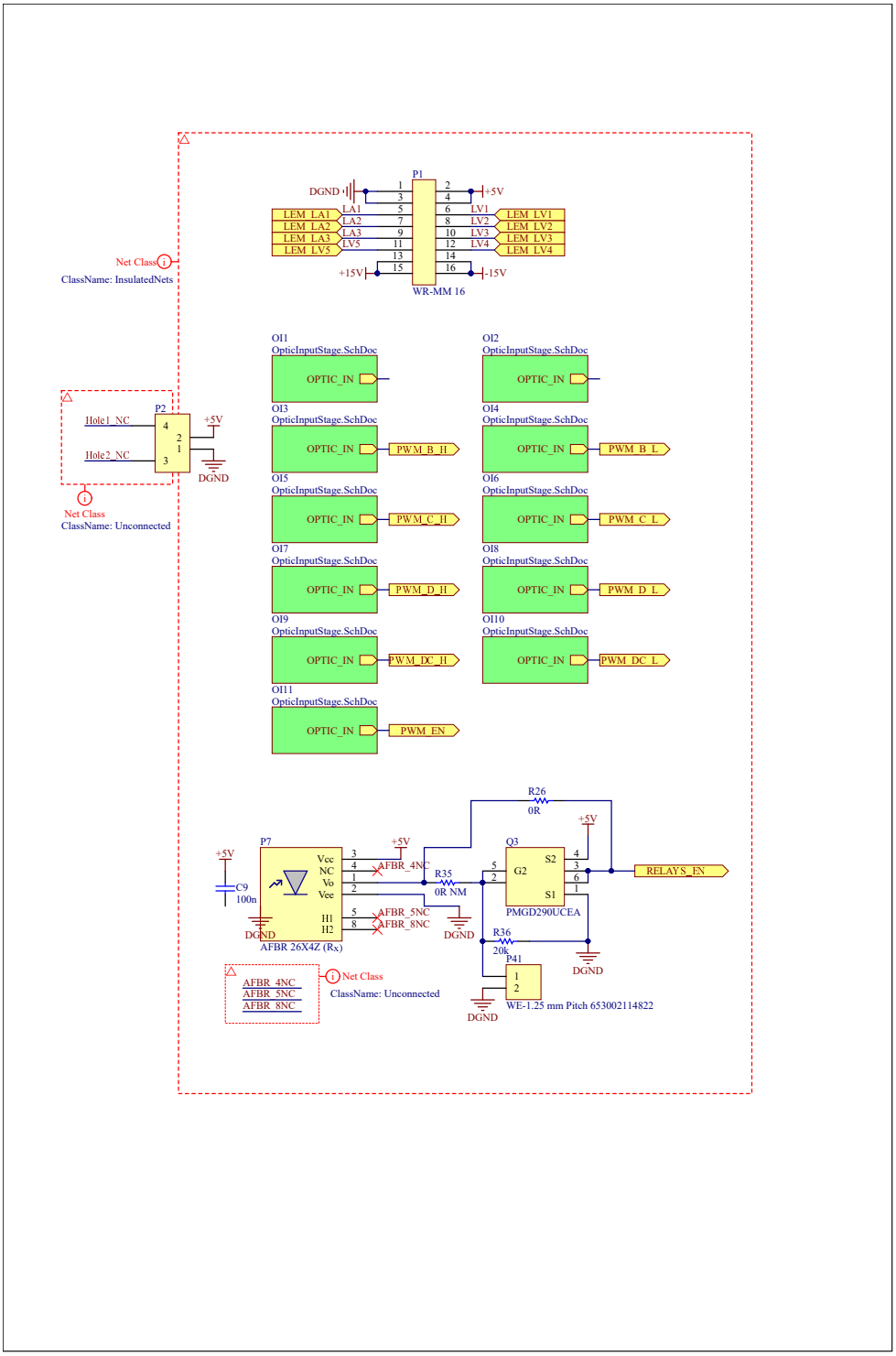


Figure A.5: Connectors (part 1).

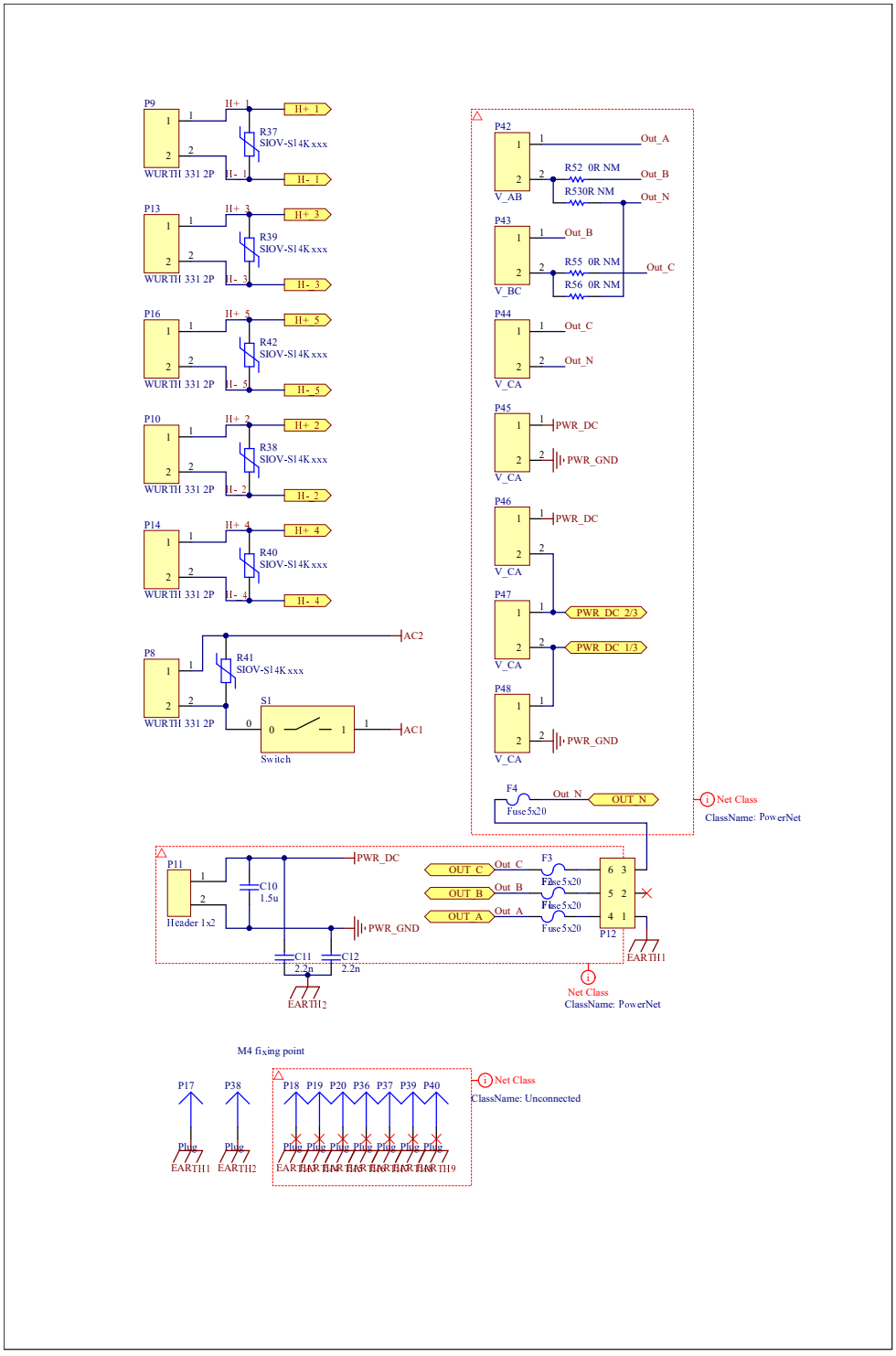


Figure A.6: Connectors (part 2).

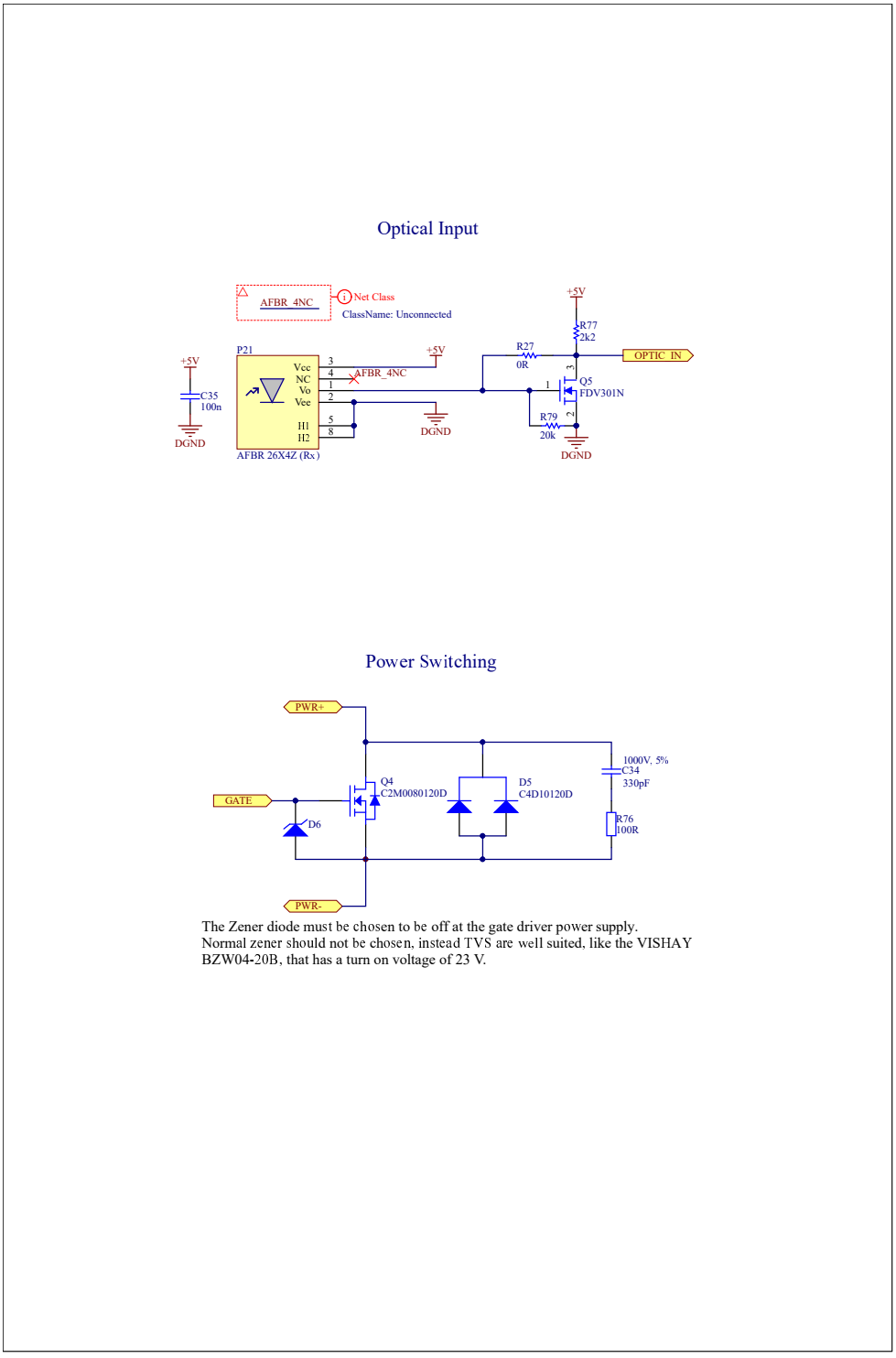


Figure A.7: Optical input stage and power switching block.

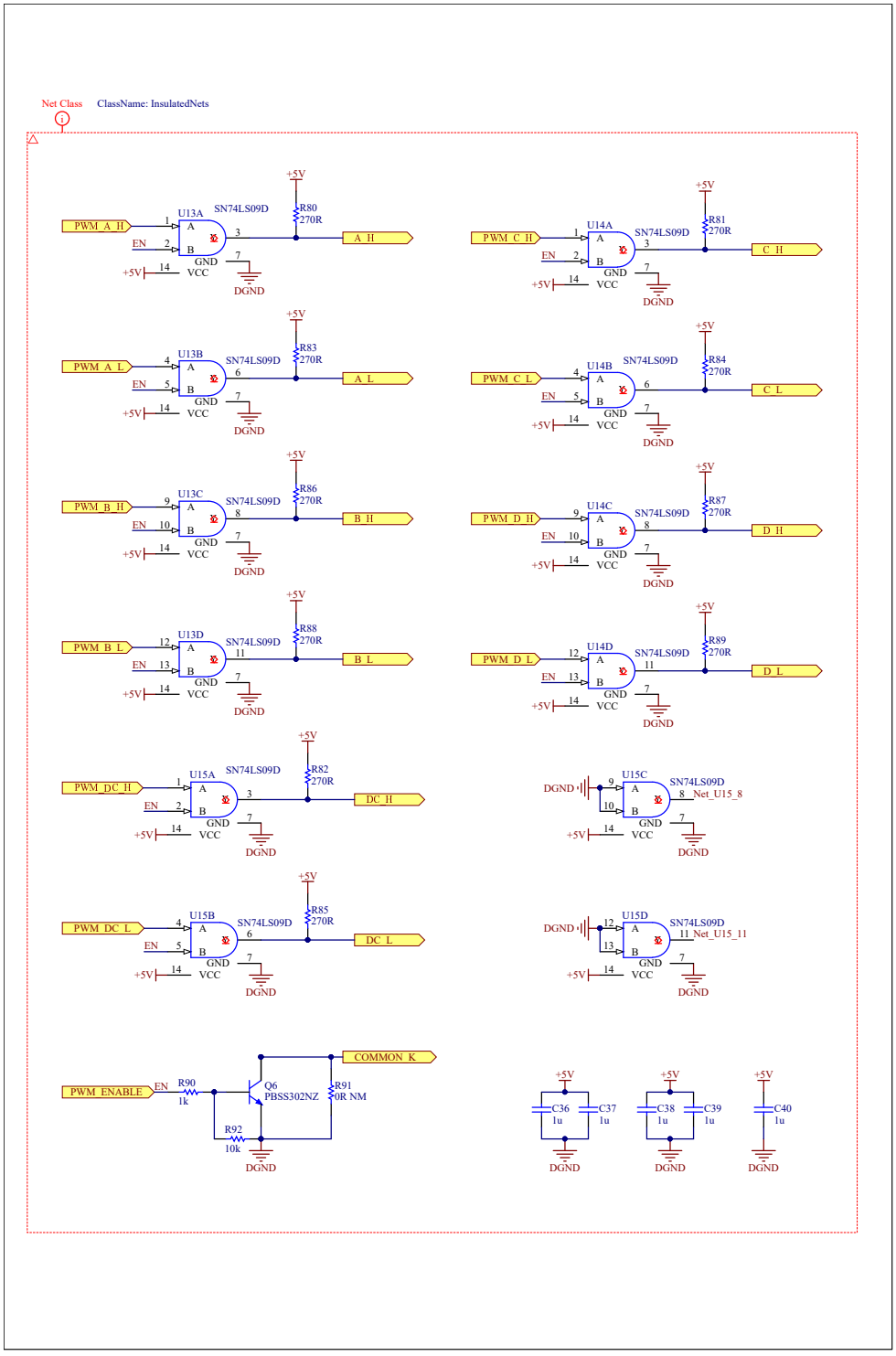


Figure A.8: Enable stage.

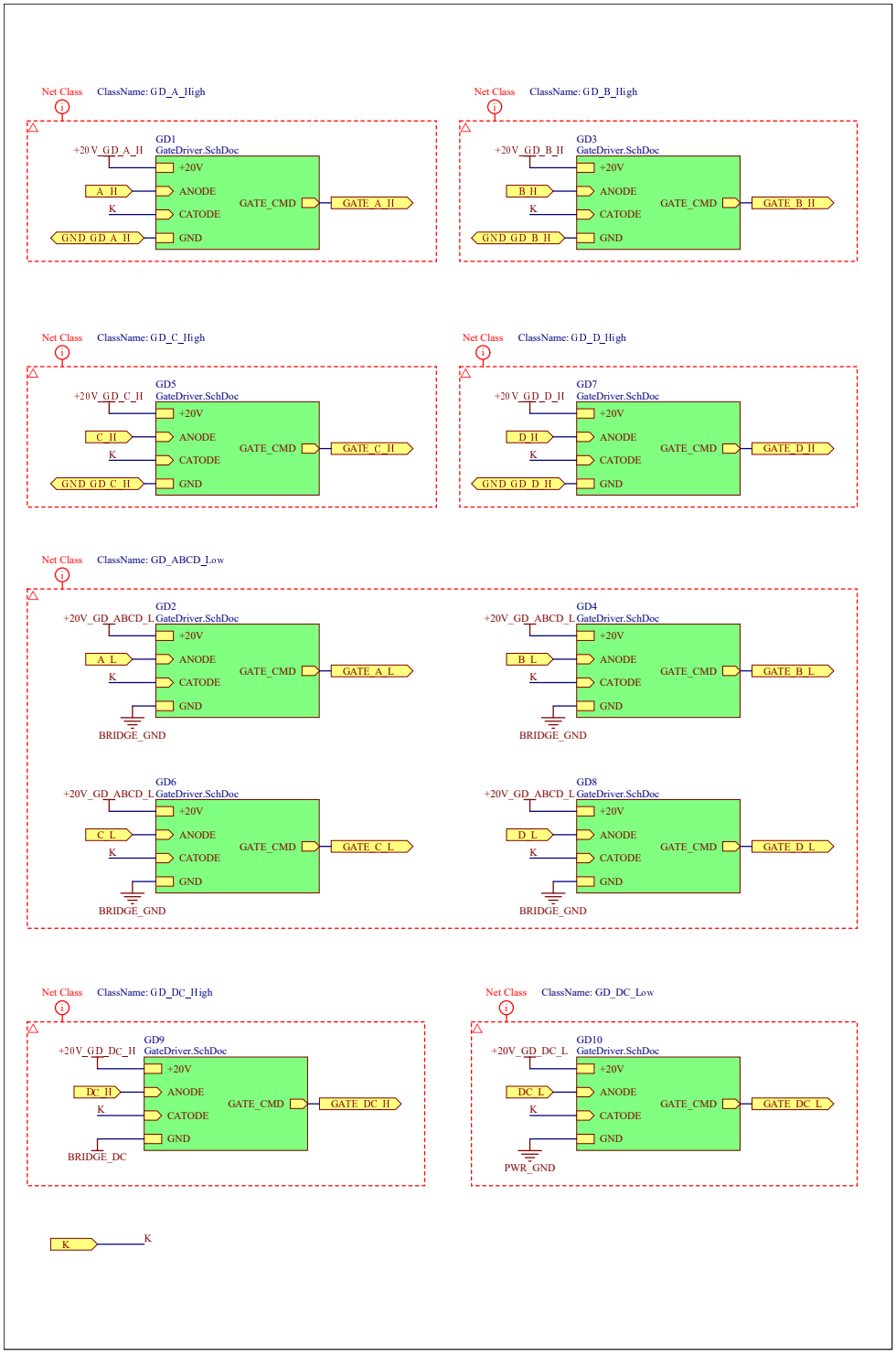


Figure A.9: Command stage.

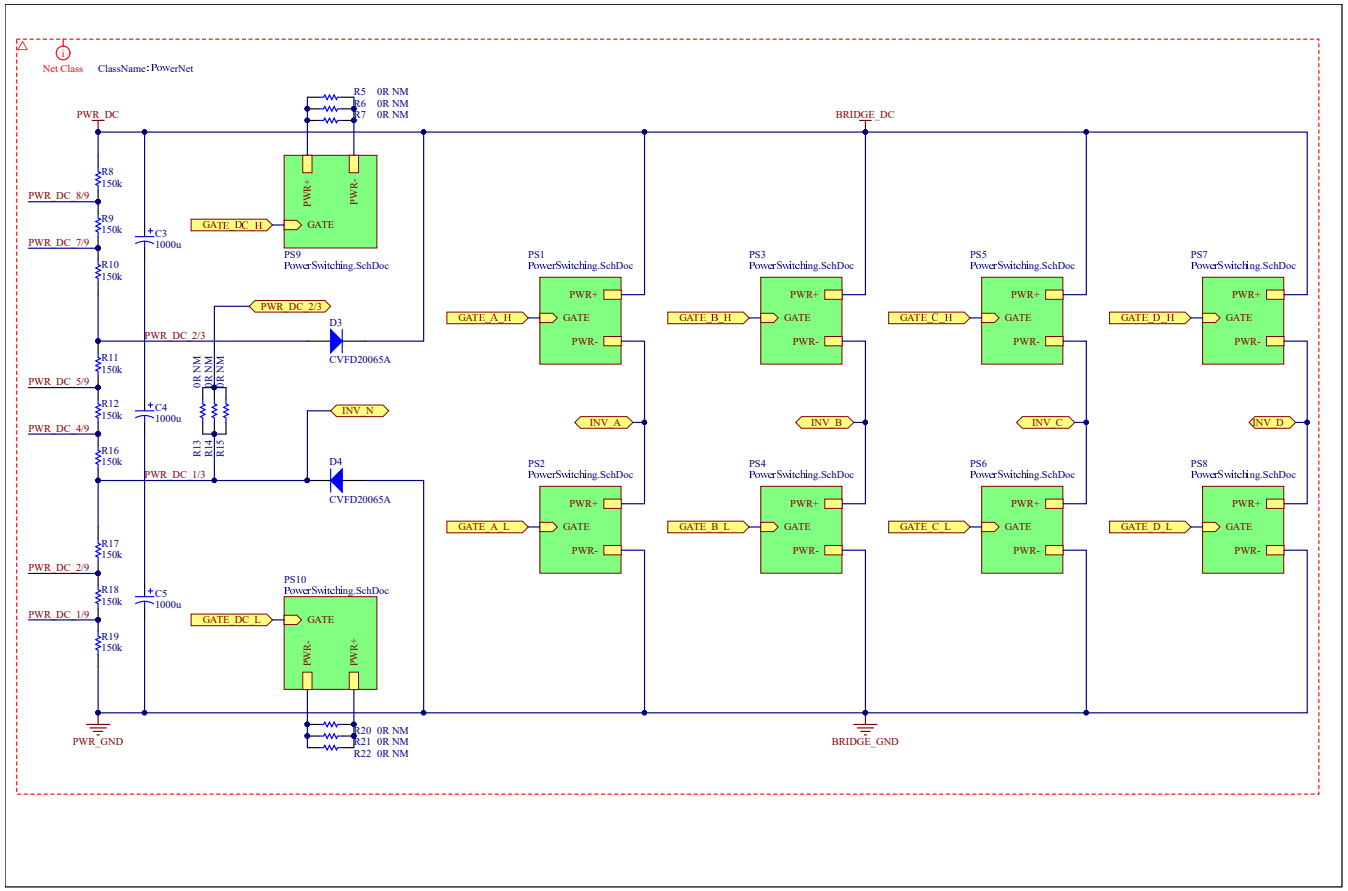


Figure A.10: Power stage.

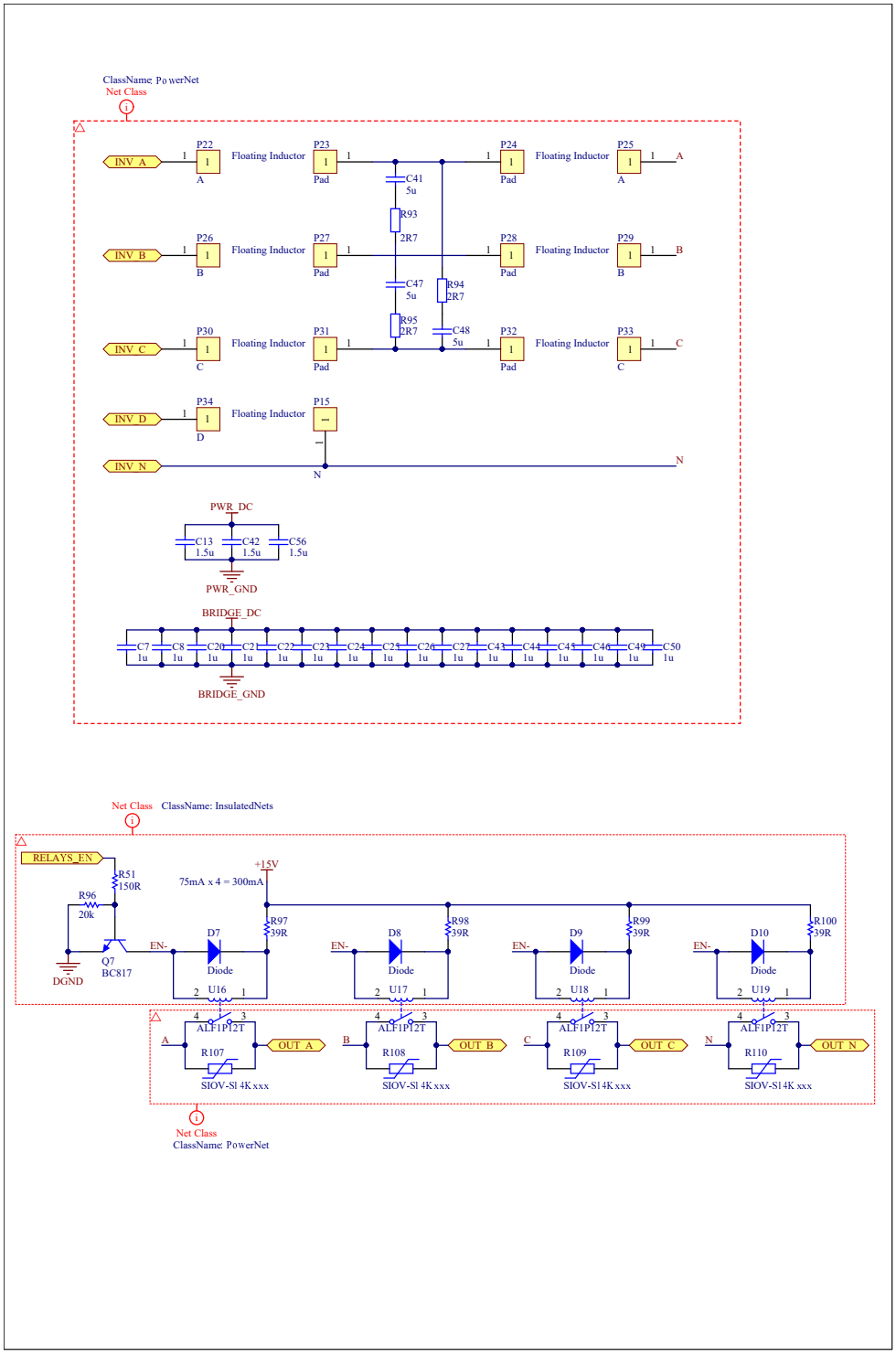


Figure A.11: Filters and relays.

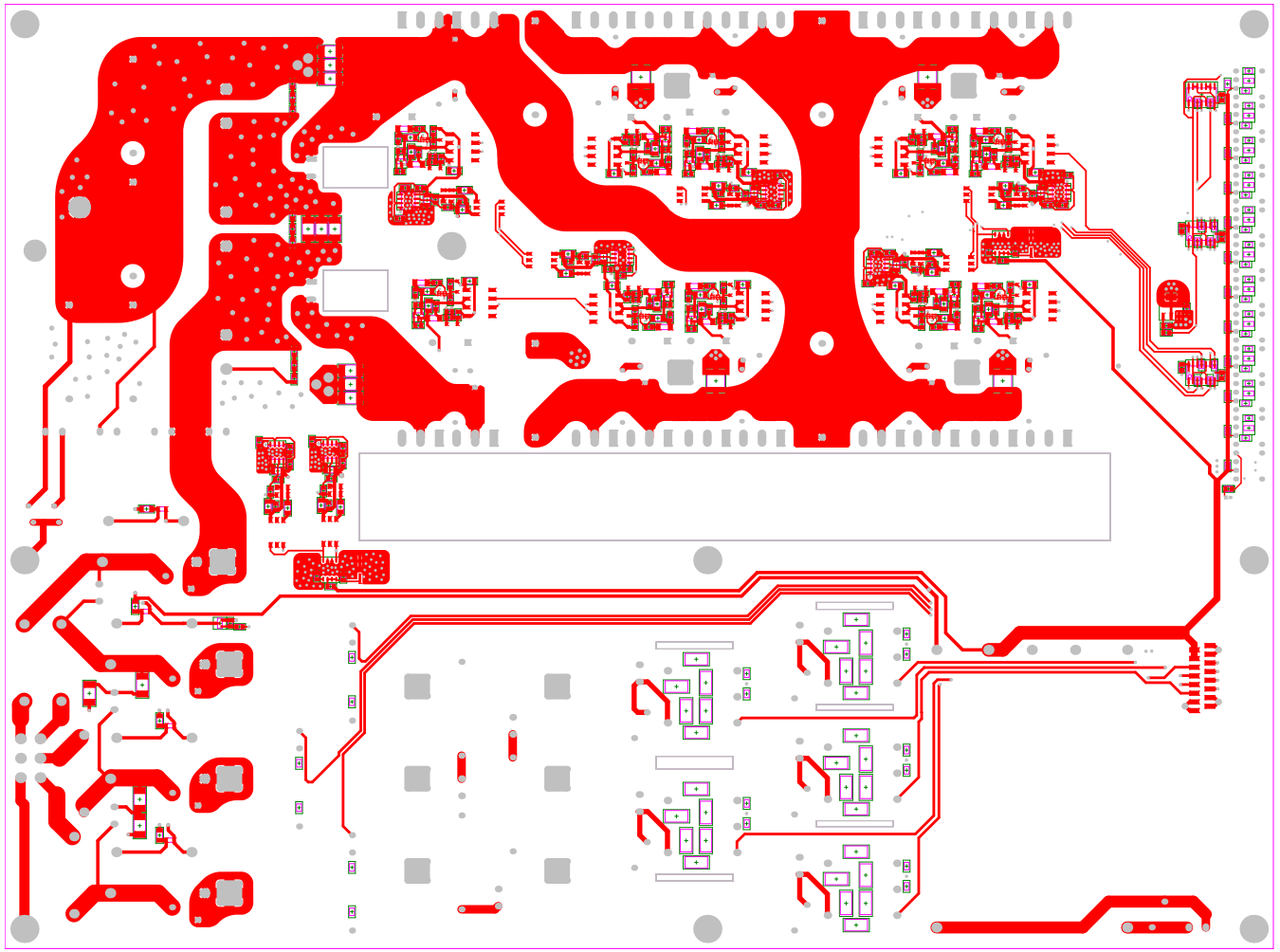


Figure A.12: Top layer.

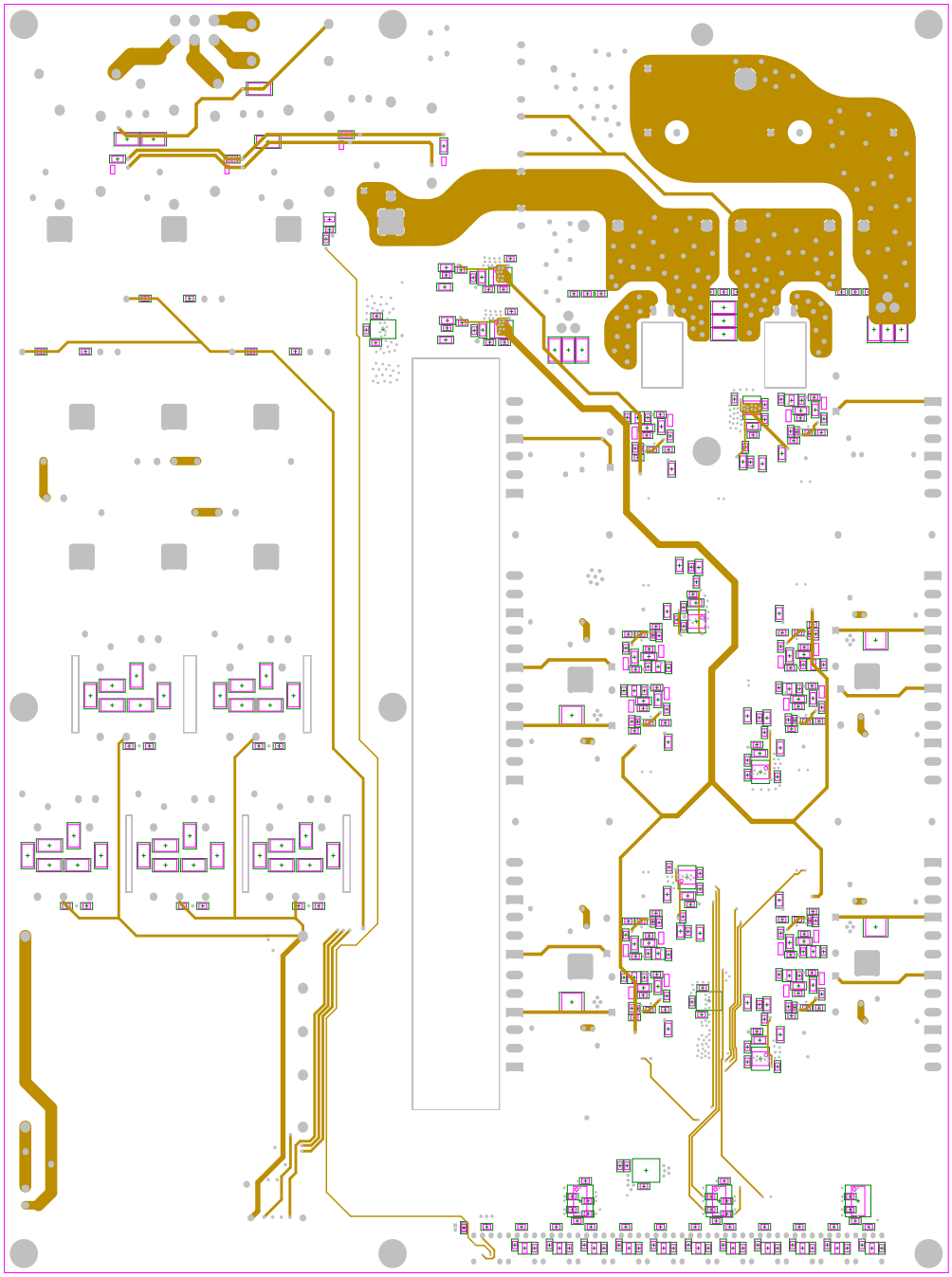


Figure A.13: Mid-layer 1.

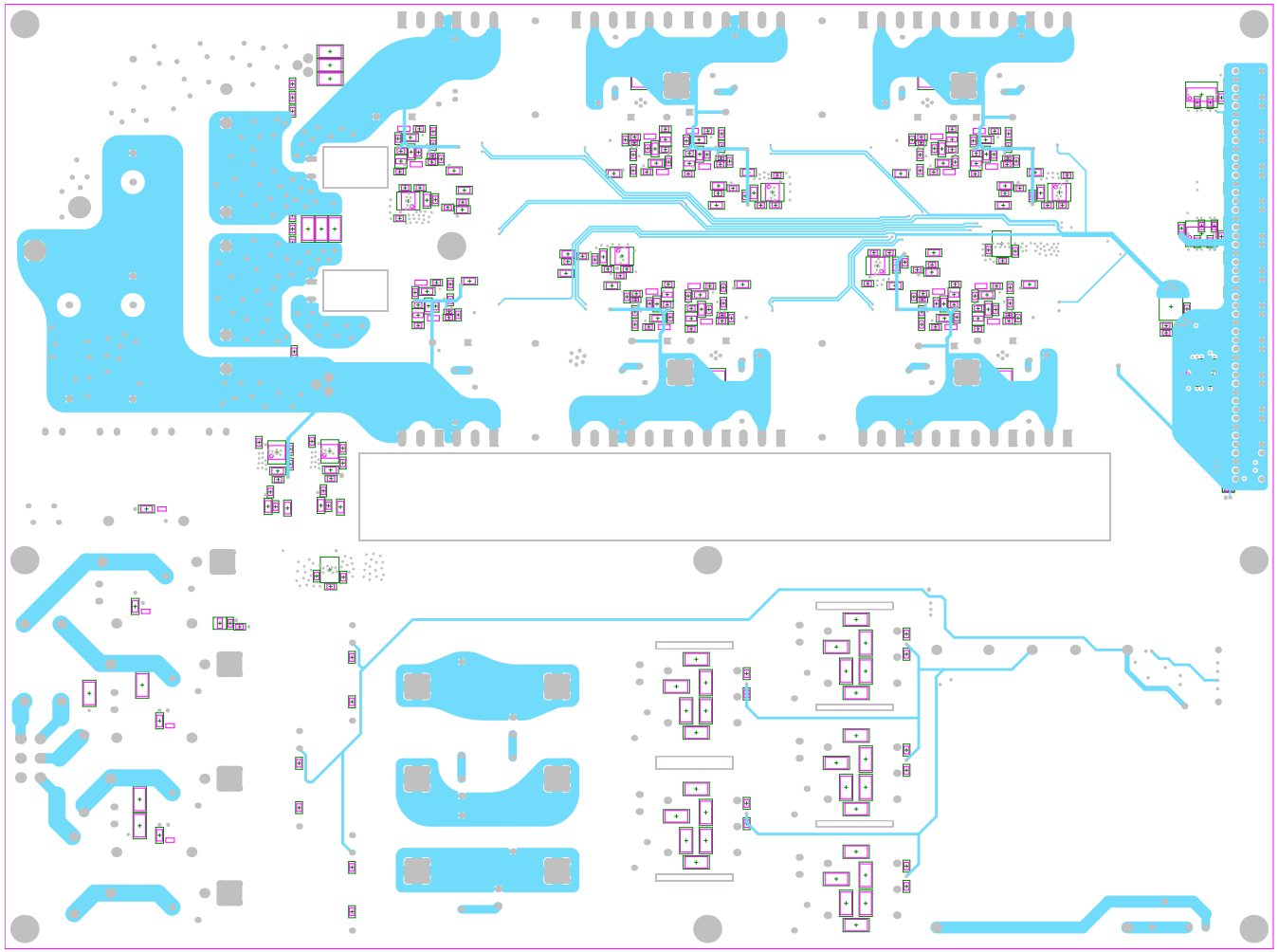


Figure A.14: Mid-layer 2.

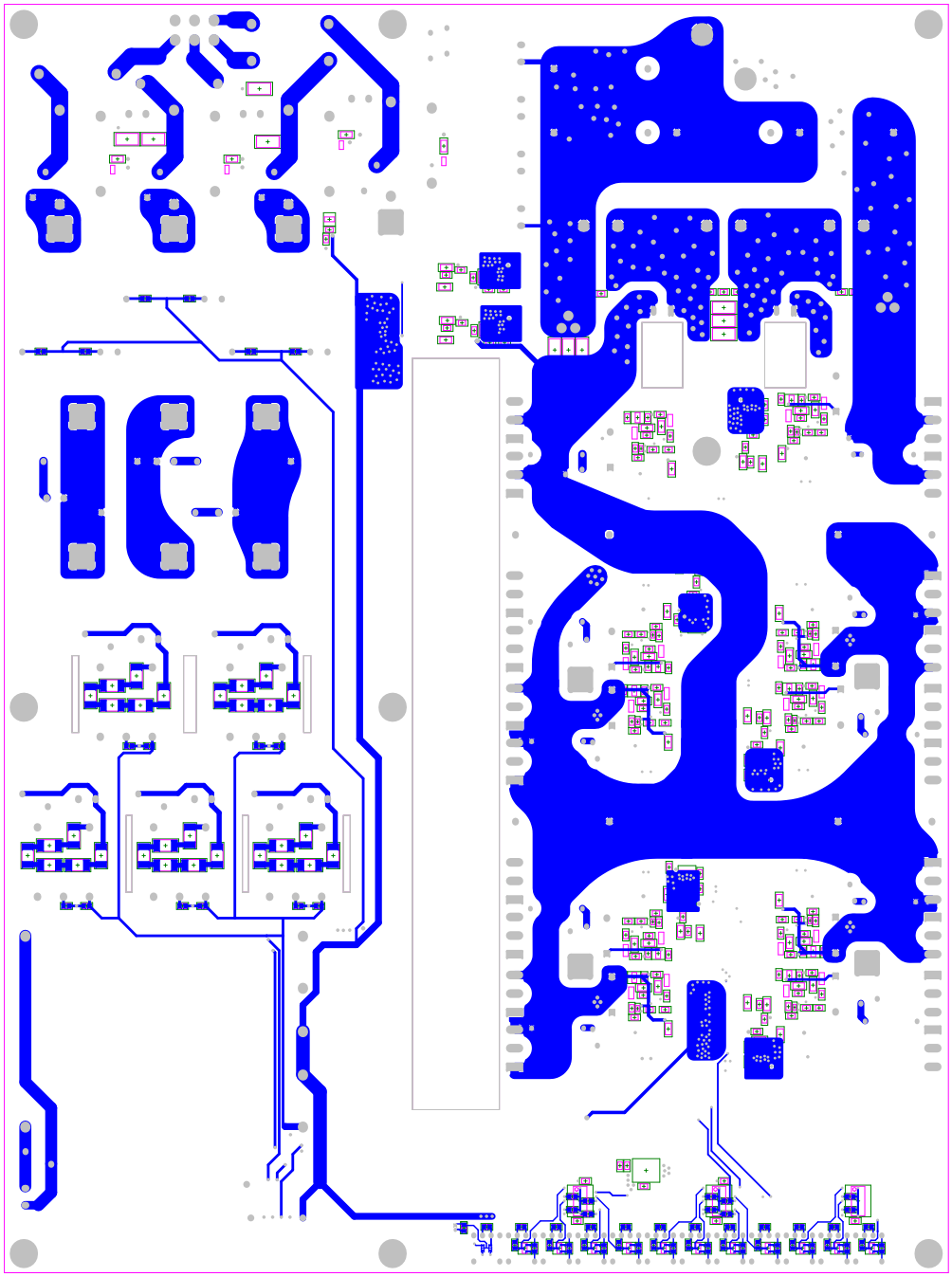


Figure A.15: Bottom layer.

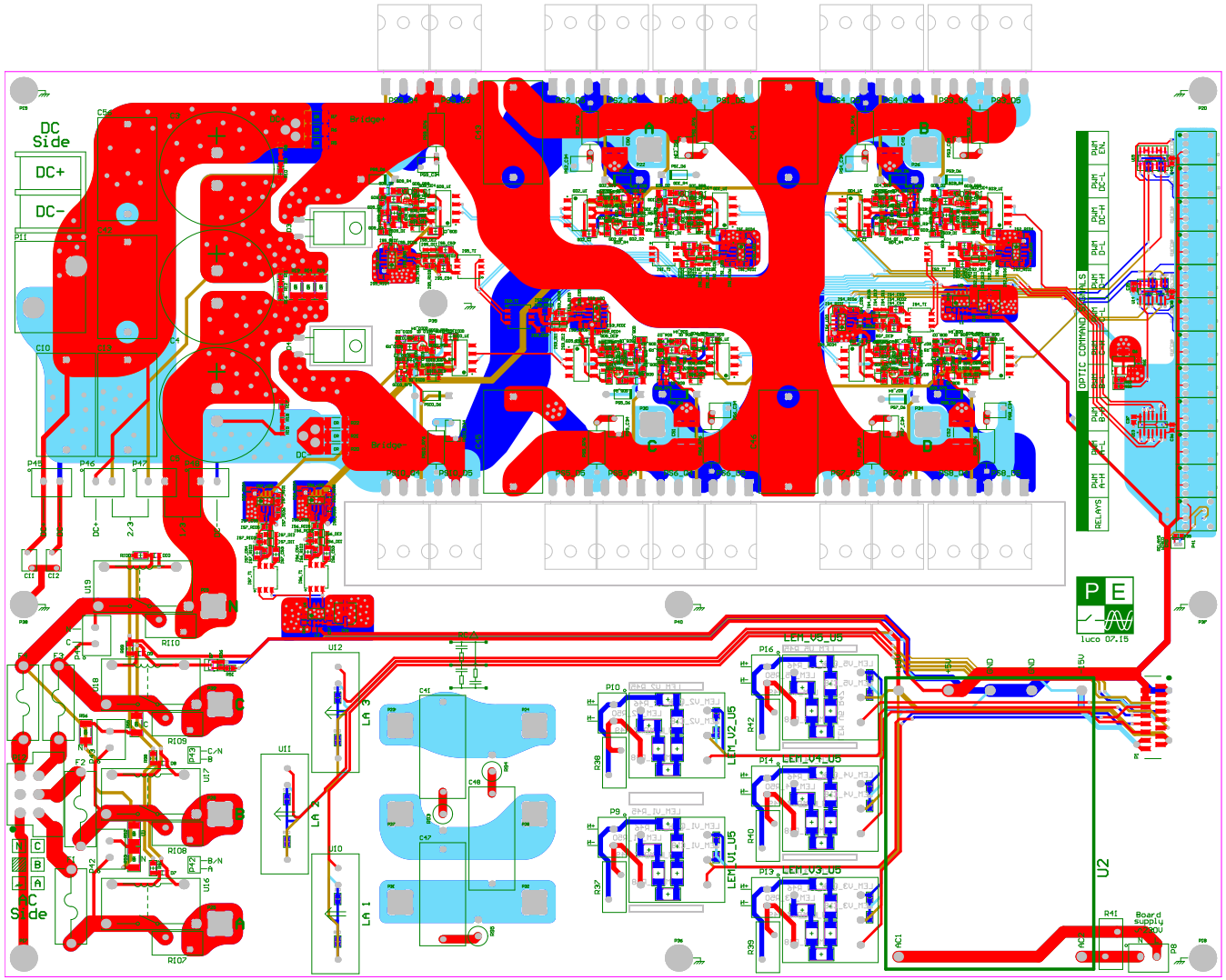


Figure A.16: Comprehensive view of all layers: top (red), mid1 (brown), mid2 (light blue), bottom (dark blue).

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