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Ciclo XXX

ELECTRICAL CHARACTERIZATION OF LOW TEMPERATURE PULSED-ELECTRON-DEPOSITED CU(IN,GA)SE_2 SOLAR CELLS

Coordinator:
Chiar.mo Prof. Enrico Dalcanale

Tutore:
Dott. Enos Gombia
Dott. Massimo Mazzer

Dottorando: Aldo Kingma

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Abbreviations and symbols

A	Ideality factor
$\mathrm{A_j}$	Area of the junction in a solar cell
AC	Alternating Current
ALT	Accelerated Lifetime Test
Al-ZnO	Aluminium doped Zinc-Oxide
AM1.5	Air Mass 1.5
AR	Anti-reflection
AS	Admittance Spectroscopy
BIPV	Building Integrated Photovoltaics
C	Capacitance
c	Speed of light in vacuum, (3×10^8 m/s)
C_0	Highest observed capacitance value, at low frequency and high temperature (in AS)
C_∞	Saturation value of the capacitance, at high frequency and low temperature (in AS)
CB	Conduction Band
CBD	Chemical Bath Deposition
CBE	Conduction Band Edge
CBO	Conduction Band Offset
CIGS	$Cu(In,Ga)Se_2$
CIS	$CuInSe_2$
CGI	Cu to Ga and In ratio (Cu/(Ga+In)) in composition of CIGS
CGS	$CuGaSe_2$
$\Delta C_{\mathrm{N1/N2}}$	Capacitance step related to N1/N2 defect contributions (in AS)
c-Si	Crystalline Silicon
C-V	Capacitance-Voltage profiling
d	Layer thickness (of ODC layer)
DC	Direct Current
DH	Damp Heat
E	Energy
$\vec{\boldsymbol{E}}$	Electric field vector
$\mathrm{E_A}$	Acceptor energy level inside the bandgap
$\mathrm{E_a}$	Activation energy of (dominant) recombination mechanism
$\mathrm{E_C}$	Lowest energy in the conduction band (see CBE)
$\mathrm{E_D}$	Donor energy level inside the bandgap
$\mathrm{E_d}$	Defect energy level inside the bandgap
$\mathrm{E_F}$	Fermi-level
$\mathrm{E_{F,N}}$	Electron Fermi-level
$\mathrm{E_{F,p}}$	Hole Fermi-level
$\mathrm{E_G}$	Bandgap energy of a semiconductor
$\mathrm{E_{ph}}$	Photon energy
$\mathrm{E_T}$	Energy inside the bandgap at which a trap level is centred
EQE	External Quantum Efficiency
$\mathrm{E_V}$	Lowest energy in the valence band (see VBE)

f	Frequency
$\mathrm{f(E,T)}$	Fermi-Dirac distribution
FF	Fill Factor
FTO	Fluoride-dope Tin Oxide
GGI	Relative Ga to Ga and In content (Ga/(Ga+In)) in CIGS composition
h	Planck's constant, $6.62607004 \times 10^{-34}$ m^2 kg/s
HRW	High Resistive Window layer
I	Light intensity
ITO	Indium Tin Oxide
IV	Current-Voltage characteristics
IV-T	temperature-dependent current-voltage measurements
i-ZnO	Intrinsic Zinc-Oxide
$\mathrm{J_0}$	Saturation current density
$\mathrm{J_D}$	Diode current (in the equivalent circuit for a solar cell)
$\mathrm{J_L}$	Current density in a solar cell due to illumination (in the equivalent circuit for a solar cell)
$\mathrm{J_{MP}}$	Current density at the MPP
$\mathrm{J_{SC}}$	Short circuit current density
$\mathbf{k}$	Crystal momentum
$\mathrm{k_B}$	Boltzmann constant, 1.38×10^{-23} m^2 kg s^{-2} K^{-1}
LRW	Low Resistance Window layer
LTPED	Low Temperature Pulsed Electron Deposition
$\mathrm{m_e}$	Electron effective mass
$\mathrm{m_h}$	Hole effective mass
MPP	Maximum Power Point
N	Carrier density
n	Free electron density
N1	Often reported step observed in capacitance at high frequency and low temperature (in AS)
N2	Often reported step observed in capacitance at low frequency and room temperature (in AS)
$\mathrm{N_A}$	Acceptor density
$\mathrm{N_D}$	Donor density
$\mathrm{n_i}$	Free electron density in intrinsic semiconductor
$\mathrm{n_N}$	Free electron density in an N-doped semiconductor
ODC	Ordered Defect Compound
OVC	Ordered Vacancy Compound
p	Free hole density in intrinsic semiconductor
PED	Pulsed Electron Deposition
$\mathrm{p_i}$	Free hole concentration in intrinsic semiconductor
$\mathrm{P_{In}}$	Power incident on a solar cell
$\mathrm{P_{Max}}$	Power output from solar cell at MPP (i.e., maximum power output)
$\mathrm{p_p}$	Free hole density on P-doped semiconductor
poly-Si	Polycrystalline Silicon
PV	Photovoltaic or Photovoltaics
Q	Static charge
q	Elementary charge (1.60217662 × 10^{-19} C)

QE	Quantum Efficiency
QNR	Quasi Neutral Region
RF	Radio-Frequency
R_S	Series resistance
R_{Sh}	Shunt resistance
SCR	Space Charge Region (depletion region)
SLG	Soda Lime Glass
SRH	Shockly-Read-Hall (refers to recombination mechanism)
STC	Standard Test Conditions
sq	'Square' for expressing sheet resistance (i.e. Ω/sq)
T	Temperature
TCO	Transparent Conductive Oxide
TFSC	Thin Film Solar Cell
w	depletion layer width
Wp	Maximum power from a solar cell under STC conditions
V	Externally applied bias
VB	Valence Band
VBE	Valence Band Edge (see E_V)
V_{bi}	Built-in potential
VBO	Valence Band Offset
V_{MP}	Voltage across solar cell at the Maximum Power Point
V_{OC}	Open-circuit Voltage
V_{OC}-T	Temperature-dependent open-circuit voltage measurements
$< x >$	Apparent depletion layer width in presence of defect response
x_N	N-side of the depletion region inside a P-N junction
x_P	P-side of the depletion region inside a P-N junction
α	absorption coefficient
α-Si	amorphous Silicon
ϵ	Dielectric constant
Φ	Photon flux (cm^{-2})
Φ_B^p	Recombination barrier to holes at CdS/CIGS interface
η	Conversion efficiency
λ	Wavelength
τ^{-1}	Emission/capture rate of traps
τ_E^{-1}	Emission rate of traps
$\mu(T)$	Chemical potential of electrons in a semiconductor
μ-Si	Microscrystalline Silicon
σ	Conductivity
ω	Angular frequency ($2\pi f$)

Abstract

Thin Film Solar Cells (TFSC's) with $Cu(In_{1-x},Ga_x)Se_2$ (CIGS)-absorber deposited by means of the novel Low Temperature Pulsed Electron Deposition (LTPED) technique developed at IMEM-CNR [1] were investigated with Admittance Spectroscopy (AS), Capacitance-Voltage profiling (C-V), temperature-dependent current voltage measurements (IV-T) and temperature dependent open-circuit voltage measurements (V_{OC}-T) to obtain information about doping densities, defect characteristics and recombination mechanisms. The novelty of the LTPED technique is the achievement of a single stage deposition at low substrate temperature (250°C as opposed to the >350°C used in other processes) by using a stoichiometric target in the Pulsed Electron Deposition (PED) technique. The characterizations performed during this thesis allowed a more detailed comparison of the behaviour of CIGS-based devices created using LTPED (LTPED devices) and CIGS-based devices produced using more conventional deposition techniques. A methodology was developed to minimize metastable effects often reported for CIGS-based devices [2] [3] [4] [5] from influencing the measurement results, and for each technique the most relevant frequency-, temperature- and bias- were determined.

The best performing LTPED devices were found to have doping densities in the range of $2\text{-}3\cdot10^{15}$ cm^{-3}, corresponding to depletion layer widths of $w\sim0.5\text{-}0.75$ μm [6]. Very often lower efficiencies could be attributed to insufficient doping. Although the AS-spectra varied significantly between investigated cells, in nearly each case a high defect density was observed and two separate steps in the capacitance similar to the 'N1' and 'N2' steps often reported in literature [7] [6] could be distinguished. For the step identified as the N1 step, the activation energy E_d of the trap-level was found to lie in the range of 40 meV $\leq E_d \leq$ 250 meV. From V_{OC}-T and IV-T measurements the activation energy E_a of the dominant recombination mechanism in the temperature range 200 K $\leq T \leq$ 350 K was found to lie close to the absorber bandgap E_G (1000-1200 meV) for nearly all cells, suggesting Shockly-Read-Hall (SRH) recombination in the bulk of the absorber layer. For $T <$ 200 K a lower activation energy was found, most likely indicating increased interface recombination or tunnelling enhanced interface recombination. For a small number of low efficiency cells ($\eta <$ 10%) values for $E_a < E_G$ were found for $T >$ 200 K, indicating alternative

recombination paths such as interface recombination limited the efficiency also at normal operating temperatures.

To test the feasibility of creating a homojunction device rather than the presumed P-N heterojunction between CdS and CIGS in standard devices, attempts were performed to deposit a layer of Ordered Defect Compound (ODC) phase of CIGS directly onto the surface of the P-type CIGS absorber using LTPED. Comparison of samples with expected ODC-layer thicknesses of $d = 0$, 10, 16, 40 and 800 nm only showed a significant loss in performance in the sample with the 800 nm ODC-layer, and an increase in the R_S and R_{Sh} values in the dark with increasing ODC-layer thickness. The increased R_S and R_{Sh} values in the dark were found to reduce to similar values as those observed on devices without ODC-layer upon illumination. These effects were attributed to a high photoconductivity in the ODC-layer due to a high concentration of defects, as also proposed in [8]. In this picture, the variations in the R_S values might be explained as a barrier for forward current being formed by the resistive ODC-layer in the dark, which reduces upon illumination as the conductivity of the ODC-layer increases. The variations in the R_{Sh} values would be explained by the additional ODC-layer covering shunting paths in the CIGS absorber, leading to reduced shunting in the dark. Under illumination, the increased conductivity of the ODC-layer would then explain the large reduction in R_{Sh}.

Accelerated lifetime tests (ALT's) in damp heat (DH, 85% relative humidity and 85°C) were performed on two LTPED devices with Ga/(Ga+In) ratio (GGI) of 0.375 and 0.3 for 60 and 80 hours respectively. As often reported in literature [9] [10] [11] [10] [12] the clearest effect of DH treatment was the degradation of the Mo and ZnO layers causing an increase in R_S. Corrosion and oxidation of the Mo might also explain the observed losses in EQE at longer wavelengths ($\lambda > 750$ nm) as discoloration of the Mo surface might cause a reduction in the amount of light reflected back into the CIGS absorber after reaching the back-contact. The generally observed decrease in R_{Sh} was attributed to degradation and gradual disappearance of the absorber layer resulting in short-circuits between TCO and Mo back-contact. The observed disappearance of CIGS and formation of 'craters' in the absorber layer is expected to be a problem more relevant

in LTPED devices, since in depositions by LTPED larger particulates/debris are known to be incorporated into the bulk of the CIGS film, which can eventually cause partial detachment [1].

In separate experiments the relevance of Na doping for formation of an ohmic contact in LTPED devices and the metastability and photoconductivity in CdS layers were investigated. Comparison of Mo/CIGS/Au and Mo/NaF/CIGS/Au samples strongly suggested that NaF can indeed allow a reduction of a back-contact barrier at the CIGS/Mo contact at temperatures for which no $MoSe_2$ is expected to form [13]. The underlying mechanism is thought to be formation of a thin, highly doped P^+-layer at the CIGS/Mo interface allowing tunnelling of charge carriers. However, significant non-uniformity of was observed in this effect in the investigated samples. Measurements performed on a $\sim$1 μm layer of CdS showed occurrence of photoconductivity with slow transients. This suggested a significant concentration of deep defects in the CdS buffer layers used in LTPED devices, which could have an important role in the metastability observed in LTPED devices.

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Introduction

GLOBAL ENERGY TRANSITION

The negative effects of the use of fossil fuels, such as air pollution and accelerated global warming, as well as the finite reserve of these fuels available on earth, have caused a rise in awareness that alternative and cleaner sources of energy are essential. The energy consumption has grown exponentially the past century, and can be expected to continue increasing at similar or higher rate the coming century.

The sharp increase in the global energy demand during the past century has caused an almost equal increase in fossil fuel consumption and hence an increase in emission of waste gases. The negative impacts on the environment due to these exhaust fumes have by now become clearly noticeable from the dangerous levels of air pollution in many industrialized areas and an accelerated rate of global warming. These effects in combination with the recent increase in oil and gas prices have caused a growing incentive for an energy transition during the past few decades. This is reflected in the increase of investments done worldwide in both research and installation of renewable energy sources, which have caused over a doubling of installed capacity during the past 10 years.

As also clear from Table 1**Error! Not a valid bookmark self-reference.**, the relative contribution from solar power to the total production of renewable energy is still small. However, this renewable energy resource has also been growing extremely fast. In 2012 the total capacity of solar power connected to the grid was estimated as slightly below 100 GW, while in 2016 it was estimated as 306.5 GW of which 76.6 GW was installed in 2016 alone [14]. This enormous growth was triggered in part by the aforementioned increase in investments in renewable energy research, but mostly by a steep drop in the costs of conventional solar cells at the start of the century. The lower cos of solar energy has allowed 'grid-parity' to be reached in many countries, meaning energy can be obtained from solar power at equal or lower cost as from the general grid. The current record for lowest sales-price of solar power is 2.4 US cents/kWh [14].

Table 1 Comparison of the contributions of solar power to the total power supply and total power capacity installed, as reported in [14]. Installed capacities refer to that installed at the end of 2007 and 2016.

	Total capacity installed (GW)			Total produced power (TWh)		
	2007	2016	Growth (%)	2007	2015	Growth (%)
Renewable energy	994.1	2,011.3	102.3	3,531	5,537	56.8
Solar power	9.26	295.9	3095	8.2	253.6	2992
Of which PV	*95%*	*99%*		*92%*	*96%*	

In light of the high energy density of the solar radiation falling onto the earth's surface, solar power is a promising technology that can allow to achieve the necessary transition to renewable energies.

INNOVATIONS IN PHOTOVOLTAICS

The most common and probably most convenient method of harvesting solar power for modern day purposes is by using solar cells. Solar cells are based on the application of semiconductor materials that allow direct conversion of incident photons into electricity through the photovoltaic effect (see sections 1.1 of Chapter 0).

From conventional to Thin Film Solar Cells (TFSC's)

The first commercial solar cells were based on Silicon (Si). This was an obvious material choice considering the suitable properties of Si for application in solar cells (see section 1.2 of Chapter 0), its' abundance on earth and the large amount of experience that was already available regarding its processing for electronics. The earliest Si-based solar cells used pure monocrystalline Si (c-Si) wafers, which require expensive and complicated production processes [15]. Later, also polycrystalline (poly) Si, microcrystalline (μ) Si and amorphous (α) Si were developed, offering a less expensive alternative but also with lower efficiency. In 2016 still 94% of the produced solar cells were based on Si, of which 70% of the solar cells was based on poly-,

μ- or α-Si category [16]. Most likely, also in the future Si will continue to dominate the market of photovoltaics.

The other ~6% of market share in photovoltaics is taken up by a more recent technology referred to as 'Thin Film Solar Cells' or TFSC's. The thickness of the absorbing layer ('absorber layer') in TFSC's is in the order of ~1 μm, while in typical c-Si solar cells a thickness in the order of ~100 μm is required for sufficient light absorption. The lower thickness of TFSC's is achieved by application of alternative materials with higher absorption efficiency than Si (also see section 1.2 of Chapter 0) and leads to significantly lower material costs. In addition, thinner solar cells can be made flexible or semi-transparent, allowing more innovative application in e.g. Building Integrated Photovoltaics (BIPV) where solar cells are incorporated into various parts of normal building architecture. This type of application which allows covering more of the available surface area with solar cell technology will become increasingly important as the contribution of solar power will continue to grow. Flexible TFSC's are also promising for 'roll-to-roll' processing which can lead to higher throughput [17].

The TFSC's that are currently available on the market are mainly based on α-Si, Cadmium Telluride (CdTe) and Cu(In,Ga)Se_2 (CIGS). Until now, TFSC's based on CdTe and CIGS have reached the highest efficiencies among this type of solar cell, with records of up to 15.7% on commercial modules. They were also found to have relatively high durability and stable in performance for such a novel technology (also see Chapter 2 and Chapter 5) [18]. For this thesis, CIGS-based devices were studied.

Developments in Cu(In,Ga)Se_2 deposition approach

Obtaining the suitable phase of CIGS for PV applications is quite challenging (see section 2.3.1 of Chapter 2). In most conventional deposition techniques this requires multiple processing steps, high substrate temperatures (≥ 400°C) and possibly toxic gases such as H_2Se (see section 2.4 of Chapter 2). The complexity of typical deposition techniques makes them difficult to scale up and obtain higher throughput. The high substrate temperature limits the range of substrate materials that can be used for the final devices.

At IMEM-CNR an approach to CIGS thin film deposition using Pulsed Electron beam Deposition (PED) was developed, in which a single stoichiometric CIGS target and a substrate temperature of only ~250°C are used. With this 'Low Temperature Pulsed Electron Deposition' (LTPED) technique, good quality CIGS films and functional PV devices with record efficiencies of 17% have been obtained [19]. The devices investigated during this thesis were deposited with this novel LTPED technique, and will be referred to as "LTPED-devices" in the following.

AIM AND SCOPE OF THIS THESIS

The aim of this thesis was to determine the electrical properties of LTPED devices, with a strong focus on aspects related to defect response, recombination mechanisms and doping and net free carrier densities. Defects (i.e. imperfections in the crystal lattice) are usually present in high concentrations in CIGS thin films and play an important role in determining the behaviour of CIGS-based TFSC's [20]. The different defects and their role in device behaviour will be treated in more detail in section 2.3.2. By studying the abovementioned properties indications of the limiting factors in the efficiency in LTPED-devices were obtained, and the doping levels of the devices were determined to verify the effectiveness of the preparation approach. A prerequisite for obtaining the results presented in this thesis was identifying the most suitable approach for performing the different characterization techniques, taking into account influences from metastability and transients in device operation (see 2.2.2.2). Hence, the first part of this thesis was focused on determining the best methodology to obtaining reproducible results from the electrical characterization of the LTPED devices. The most important results from this thesis were obtained using current-voltage (IV-T), open-circuit voltage versus temperature (V_{OC}-T), admittance spectroscopy (AS) and capacitance-voltage (C-V) measurements. Further background regarding the different measurement techniques and the established methodology are discussed in more detail in Chapter 3. The established methodology was applied to LTPED-devices with a number of different architectures.

A smaller part of this thesis concerned investigations of the photoconductivity and metastabilities in the buffer layer material (CdS), the influence of an NaF precursor layer on the formation of an

ohmic contact at the interface between the CIGS layer and the back-contact (Mo), and accelerated lifetime tests (ALT's) performed on LTPED devices. Although the investigations regarding the CdS and Mo/CIGSIn particular the investigations regarding the photoconductivity in CdS and the contact at the CIGS/Mo interface were relatively small and inconclusive, they were useful in the interpretation of the results from the main investigations.

THESIS OUTLINE

Chapters 1, 2 and 3 of this thesis contain some background theory. In Chapter 0 some basics regarding semiconductors and their application in PV devices are treated. In Chapter 2 a more detailed background is given regarding CIGS-based TFSC's and their typical behaviour. In Chapter 3 the basic theory regarding the IV-T, V_{OC}-T, C-V and AS characterization techniques is presented the applied methodology is described.

The main results of this thesis are presented in the Chapters 4 to 6. Chapter 4 contains both an introduction to the LTPED deposition technique and LTPED device preparation, and the results obtained for devices with standard architecture. In Chapter 5 the results obtained from the investigation of LTPED-devices in which an attempt was made to deposit an additional layer of an 'Ordered Defect Compound' or ODC-phase material are presented. Chapter 6 contains the results from Accelerated Lifetime Tests (ALT's) on a small number of LTPED devices, and some preliminary conclusions that could be obtained regarding limiting factors in the lifetime of this type of device. After a presentation of the results, the conclusions and perspectives are given. The appendices contain a list of the different measurement techniques that were used (Appendix A), the investigations regarding the formation of an ohmic contact at the CIGS/Mo interface (Appendix B) and the investigations regarding photoconductivity in the CdS buffer layer (Appendix C).

1 Background of solar cells

INTRODUCTION

This chapter contains some important theory about solar cells and their operation and introduces the terminology used to describe solar cell performance. In section 1.1 the photovoltaic effect, the fundamental functionality of a solar cell, is described in some detail. In section 1.2 the most important requirements that need to be met to achieve efficient photovoltaic conversion of solar energy are discussed, and the standard approach to analysing and describing the performance of solar cells is explained.

1.1 THE PHOTOVOLTAIC EFFECT

The photovoltaic effect refers to formation of an electric field and current following the excitation of charge carriers (electrons and holes) by photons incident on a material or device. In most solar cells this is achieved by implementing a P-N junction diode, a device formed from two layers of semiconductor material. Before arriving at the photovoltaic effect in P-N junctions in section 1.1.2, some relevant theory and terminology regarding semiconductor properties is introduced in section 1.1.1. A more complete and detailed description of semiconductor properties is given in, for example, references [21] and [22]

1.1.1 Intrinsic semiconductors and generation/recombination

Semiconductors are materials with a low intrinsic conductivity at room temperature, which can be changed by adding impurities (i.e. 'doping' the material). The low intrinsic conductivity is due to restrictions in the energies E and momenta $\mathbf{k}$ that electrons can attain inside the material**.** These restrictions follow from Bloch's theorem, which states that the dispersion relation $\mathrm{E}(\mathbf{k})$ between allowed energies and momenta needs to have periodicity in $\mathbf{k}$ corresponding to the spatial periodicity of the crystal lattice. The allowed combinations $\mathrm{E}(\mathbf{k})$ are usually visualized using a band-diagram, an example of which is shown in Figure 1. In the lowest energy configuration of a semiconductor the electrons will fill up the lowest available distinct states. This

results in a range of energies that would be occupied even at 0 K, which the Valence Band (VB) with highest energy (the Valence Band Edge or VBE) at $\mathrm{E_V}$. The allowed states that remain unoccupied in this configuration define the Conduction Band (CB) with lowest energy $\mathrm{E_C}$ (the Conduction Band Edge or CBE).The VBE and CBE are separated by an energy gap or bandgap $\mathrm{E_G} = \mathrm{E_C} - \mathrm{E_V}$ where no allowed electron states exist. Electrons can then be excited from the VBE to the CBE under excitations with energy satisfying $\mathrm{E} > \mathrm{E_G}$.

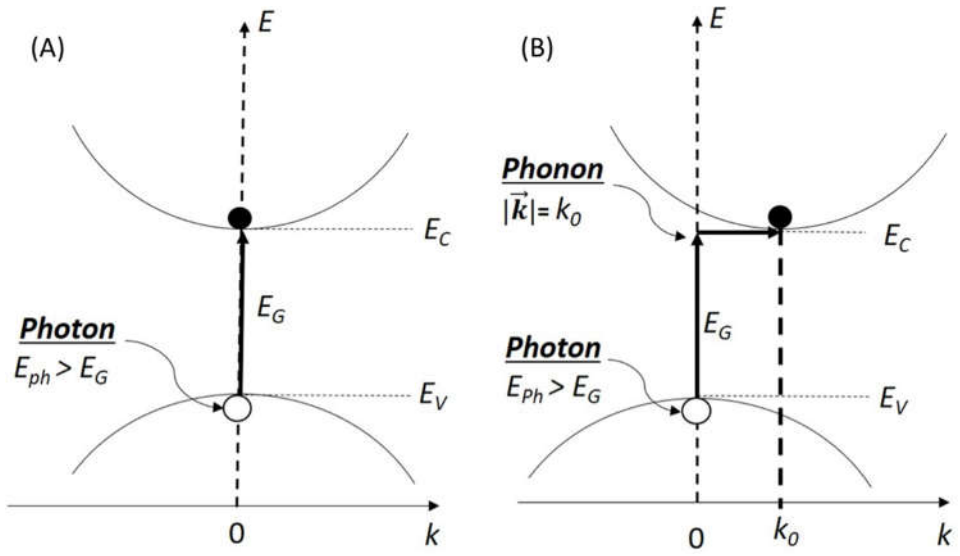


Figure 1 Examples of band-diagrams illustrating the difference between the absorption processes in a direct (A) and indirect (B) bandgap semiconductor. Open circles indicate holes (empty electron states) and filled circles indicate electrons.

Once an electron reaches the CB it can give rise to conduction by moving between the large number of unoccupied energy states. The corresponding equation of motion is similar to that of a free particle if an 'effective mass' $\mathrm{m_e}$ is introduced to take into account the forces due to the potential of the atoms forming the crystal lattice. Hence, an electron in the CB is often referred to as 'free charge carrier' or 'free carrier'. Empty electron states in the VB also give rise to electron transport by allowing electrons in the VB to move from occupied to unoccupied states. This type of conduction is most easily described by considering the empty electron state as a virtual positive charge carrier (hole) which also acts as free particle with effective mass $\mathrm{m_h}$ (much higher than $\mathrm{m_e}$ for electrons). In an intrinsic semiconductor, every free electron in the CB will

correspond to a free hole in the VB, so that the concentration of free electrons n will always equal the concentration of free holes p.

The probability of occupation of an electron state depends on the energy of the state E and the temperature of the system T, as given by the Fermi-Dirac distribution (Equation 1.1)

$$\mathrm{f(E,T)} = \frac{1}{1 + \exp\left(\frac{\mathrm{E} - \mu(\mathrm{T})}{\mathrm{kT}}\right)} \qquad 1.1$$

Here, $\mu(\mathrm{T})$ is the chemical potential for electrons in the material. Note that this probability distribution doesn't take into account whether the state is actually allowed in the semiconductor crystal. For the distribution of allowed states a different density of states function is used. At 0 K, $\mathrm{f(E)}$ forms a step function which gradually smooths out at higher temperatures, as shown in Figure 2.

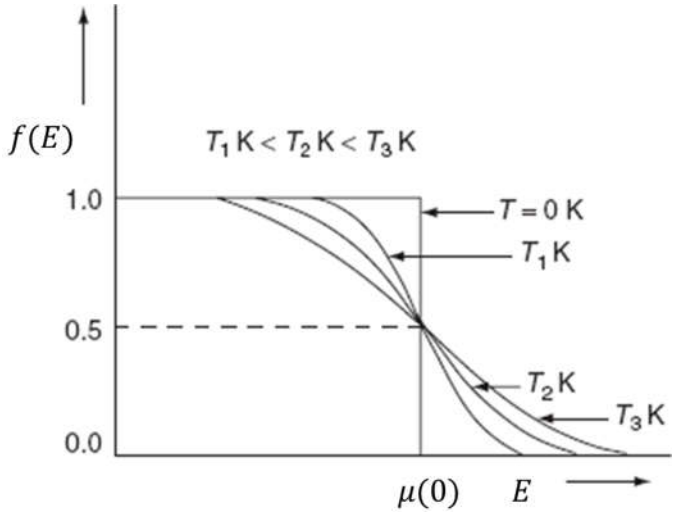


Figure 2 Fermi-Dirac distribution plotted for 0 K and three temperatures T $>$ 0 K [23]

The energy $\mathrm{E} = \mu(\mathrm{T})$ is referred to as the Fermi-level $\mathrm{E_F}$. From the given expression for $\mathrm{f(E)}$ it follows that $\mathrm{f}(\mu(\mathrm{T})) = \frac{1}{2}$, so that if an allowed electron state would exist at the Fermi-level it would have equal probability of being occupied and unoccupied.

For an intrinsic semiconductor, the condition $n = p$ results in a symmetric distribution around the centre of the bandgap, so that $E_F \sim \frac{E_G}{2}$ at all temperatures. For doped semiconductors the introduction of additional electron states leads to a shift in the probability distribution (and therefore E_F) toward either the VB band or CB. Hence, from the position of E_F a useful indication of the conductivity properties of a semiconductor is obtained.

The creation of free carriers in a semiconductor can occur through thermal, optical or electrical excitations and is referred to as free carrier *generation*. In stationary conditions free carrier generation is balanced by carrier *recombination*, the opposite process in which electrons from the CB drop to the VB and 'recombine' with holes. Different possible routes for carrier recombination exist in a semiconductor, as will be discussed specifically for Cu(In,Ga)Se_2-based devices in Chapter 4. Of course, for photovoltaics the process of free carrier generation by absorption of incident photons (i.e. band-to-band absorption) is particularly important. This process is illustrated in Figure 1 for a direct bandgap (where VBE and CBE occur at the same value of $\mathbf{k}$) and an indirect bandgap (where VBE and CBE occur at different values of $\mathbf{k}$). For a direct bandgap, a photon with energy $E_{ph} \geq E_G$ is sufficient to excite an electron to the CB. For an indirect bandgap an additional momentum $\mathbf{k_0}$ needs to be provided, which requires a phonon (lattice vibration) since the momentum of photons is usually negligible. This makes band-to-band absorption much less probable for indirect bandgap semiconductors than for direct bandgap semiconductors.

The amount of band-to-band absorption in a semiconductor follows the Lambert-Beer law, where upon incidence of light at intensity I_0 the amount of light remaining after passing through a thickness x of the semiconductor is given by

$$I = I_0 \exp(-\alpha x) \qquad 1.2$$

Here, α is the absorption coefficient and has units of inverse length. It depends on the photon energy E_{ph} (and hence photon wavelength according to $E_{ph} = \frac{hc}{\lambda}$) and the semiconductor bandgap E_G. The expression for α is quite different for direct and indirect bandgap

semiconductors due to the different mechanisms involved. For a direct bandgap, α the dependence of E_{ph} and E_G is given by:

$$\alpha \propto a\sqrt{E_{ph} - E_G} \qquad 1.3$$

Here a is a constant. For indirect semiconductors the dependence becomes quadratic:

$$\alpha \propto a(E_{ph} - E_G)^2 \qquad 1.4$$

The absorption coefficients are shown as function of wavelength for a number of direct and indirect bandgap semiconductors in Figure 3. The much higher absorption coefficients of direct bandgap semiconductors indicates they require much less material to achieve the same amount of absorption, which makes them advantageous for photovoltaic applications.

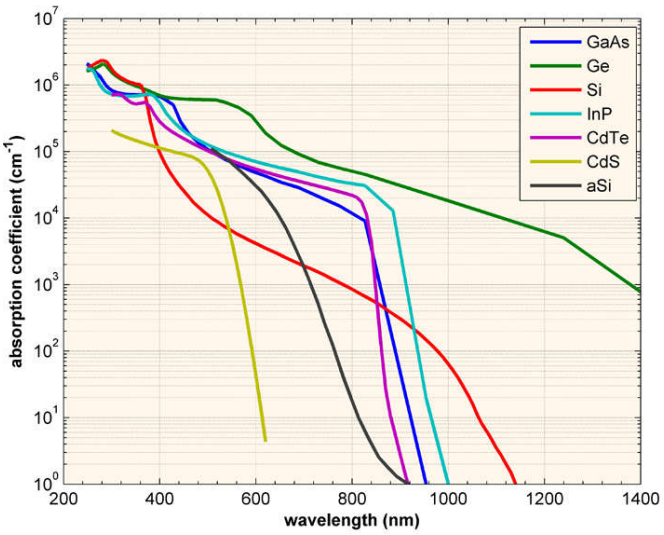


Figure 3 Absorption coefficient as function of wavelengths for a number of semiconductors often used in photovoltaics: Si (red curve, indirect bandgap), Ge (green curve, both direct and indirect bandgap), α-Si (black curve, large number of indirect bandgaps), and the direct bandgap semiconductors GaAs (dark blue curve), InP (light blue curve), CdTe (pink curve) and CdS (yellow curve) [24]

1.1.2 Semiconductor doping and P-N junctions

The conductivity of a semiconductor can be changed from intrinsic to P-type (conduction via holes in the VB) or N-type (conduction via electrons in the CB) by appropriate doping. P-type

conductivity is achieved by introducing impurities that can take-up electrons from the VB (acceptor impurities) resulting in the formation of an acceptor energy level at E_A, with ($E_A - E_V \leq kT$). Introduction of the acceptor level at E_A close to the VB results in a higher occupation probability of states in the energy range $E \leq \frac{E_G}{2}$ than in the intrinsic case, so that E_F shifts towards the VB. Analogously, to achieve N-type conductivity impurities that can give-off electrons to the CB (donor impurities) are introduced, resulting in the formation of a donor energy level at E_D with ($E_C - E_D \leq kT$). In case of presence of a donor level, the increased probability of states in the energy range $E > \frac{E_G}{2}$ causes a shift of E_F towards the CB.

Since $(E_A - E_V) < kT$ and $(E_C - E_D) < kT$, nearly all impurities can be expected to be ionized at room temperature. For a P-type semiconductor with acceptor concentration N_A the free hole concentration will be approximately given by $p_P \approx N_A + n_i$, with n_i the intrinsic carrier concentration. For a N-type semiconductor with donor concentration N_D the free electron concentration will be approximately given by $n_N \approx N_D + n_i$. The more abundant free carriers are referred to as 'majority carriers' while those at lower concentration are referred to as 'minority carriers'. The minority carriers generated in a semiconductor will have a high probability of recombining due to the much higher concentration of majority carriers. The average time it takes for minority carriers to recombine is referred to as the minority carrier lifetime, with the expected distance the minority carriers can travel without recombining referred to as the minority carrier diffusion length. Usually electrons have a longer minority carrier lifetime/diffusion length than holes due to their lower effective mass, which is an important consideration in the design of the P-N junction, as discussed in section 1.2.

To establish a photovoltaic effect, majority and minority carriers need to be separated after their generation by incident photons. One common way to achieve this carrier separation is by using a combination of a N-type and P-type semiconductor in a P-N junction, as illustrated in Figure 4.

At formation of the interface between the N-type and P-type material, the large gradient in charge carrier concentrations on both sides gives rise to a diffusion current of electrons from N-side to P-side and holes from P-side to N-side, as illustrated in Figure 4. Electrons arriving at the

P-side become minority carriers and quickly recombine with majority carrier holes, leaving behind positively charged donors on the N-side and negatively charged acceptors on the P-side.

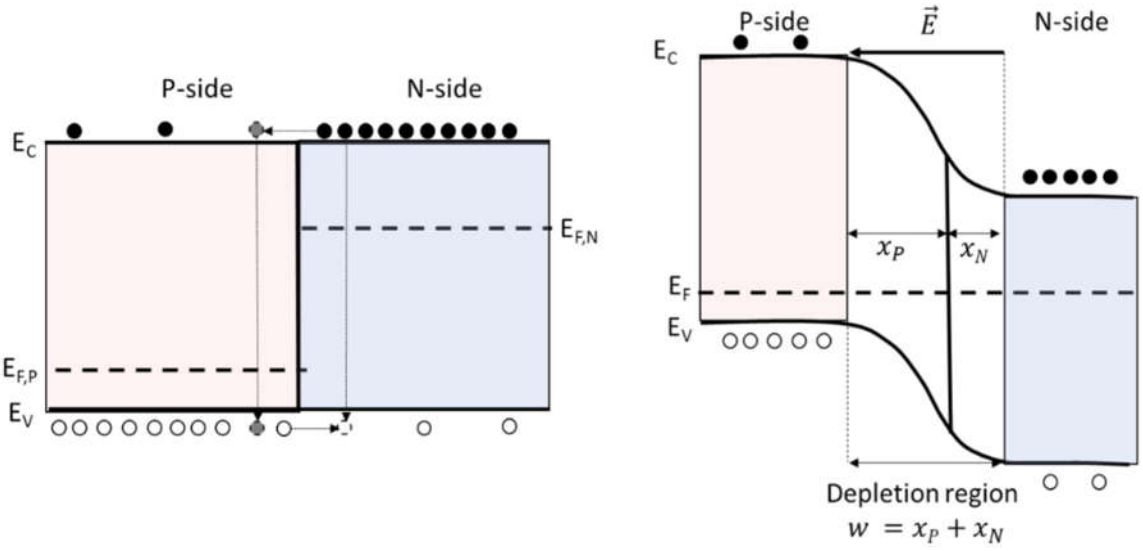


Figure 4 Band-diagram for a P-N junction near the interface before (left) and after (right) reaching equilibrium. $E_{F,P}$ and $E_{F,N}$ refer to the Fermi-level for electrons on the P-side and N-side of the junction respectively. Closed circles represent electrons, open circles represent holes.

Thin layers with thicknesses x_N and x_P and only positively charged donors and negatively charged acceptors remain on the N-side and P-side respectively. The entire region with thickness $w = x_N + x_P$ depleted of free carriers is referred to as the depletion region or 'space-charge region' (SCR).

The fixed charge inside the SCR in an electric field directed from the N-side to the P-side, as also indicated in Figure 4. This electric field gives rise to a 'drift current' in opposite direction of the diffusion current, as electrons are swept from P- to N-side, and holes are swept from N- to P-side. Equilibrium is reached once the diffusion current and drift current balance each other. In Figure 5 the charge carrier densities, charge distribution, electric field and electric potential in a symmetric P-N junction are shown under equilibrium conditions.

The built-in potential V_{bi} across the junction at equilibrium can be expressed in terms of the intrinsic carrier concentration n_i and majority carrier concentrations on both sides of the junction (i.e. n_N and p_P)

$$V_{bi} = \frac{kT}{q} \cdot \left(\frac{n_N p_P}{n_i^2}\right) \approx \frac{kT}{q} \cdot \left(\frac{N_D N_A}{n_i^2}\right) \qquad 1.5$$

The depletion layer width w can be expressed in terms of the V_{bi}, doping densities and external bias V according to

$$w = \sqrt{\left(\frac{2\epsilon(N_A + N_D)}{q(N_A N_D)}(V_{bi} - V)\right)} \qquad 1.6$$

Here, ϵ is the dielectric constant of the semiconductor material. The external bias V is considered as positive or forward bias if it opposes V_{bi} (with cathode at the P-side and the anode at the N-side) and as negative or reverse bias otherwise.

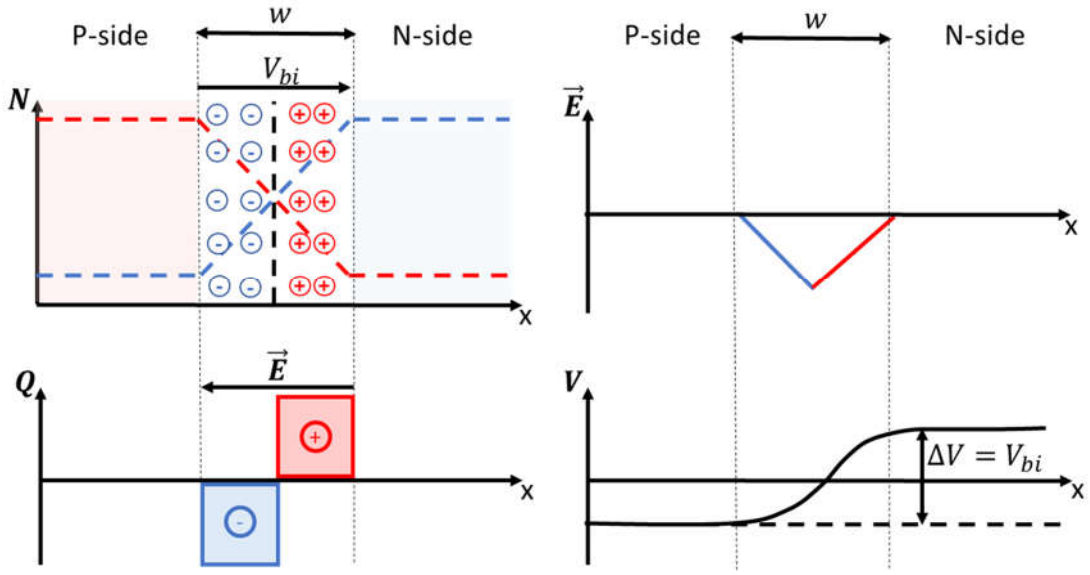


Figure 5 Schematic representation of the spatial distribution of charge carrier density N (red line = electrons, blue-line = holes), static charge Q, electric field $\vec{E}$ and electric potential V in a P-N junction with depletion layer width w in equilibrium.

At application of forward bias the depletion layer width will reduce as majority carriers are driven toward the depletion layer edges, and for high enough forward bias will become negligible. At application of reverse bias the depletion layer width will increase as majority carriers are pulled

away from the depletion layer edges. The current will only slightly increase due to an increase in the drift current of minority carriers across the depletion layer. At high enough reverse bias the junction breaks down and the depletion layer disappears, causing a much faster increase in reverse current. In short, the P-N junction acts as a diode and allows current to pass relatively easily in forward direction, while resisting reverse current up to the break-down voltage.

The above-described internal electric field of a P-N junction allow it to be applied to obtain a photovoltaic effect. After band-to-band absorption of incident photons satisfying $E_{ph} > E_G$, minority carriers formed within a diffusion length distance from the edges of the depletion region will be swept to the other side of the junction by the internal electric field and become majority carriers. This leads to an increase in the majority carrier density on both sides of the junction after photo-excitation, and the build-up of an electric field and a current that can be driven into an external circuit.

1.2 SOLAR CELL DEVICES AND EFFICIENCY

Whereas the previous part of this chapter was concerned mainly with the fundamental theory regarding semiconductors and P-N junctions, the current part concerns the description of complete solar cells based on P-N junction diodes. In section 1.2.1 the most important requirements to obtain functioning solar cells for terrestrial purposes will be discussed, still mainly regarding the properties of the P-N junction. Section 1.2.2 is focused on the description of the behaviour of complete solar cells.

1.2.1 From P-N junction to solar cell

From section 1.1.2 above, it will be clear that the efficiency of photo-absorption, carrier separation and carrier collection in a solar cells are mainly determined by the quality of the P-N junction. As already described in section 1.1.1, the absorption coefficient and hence efficiency of absorption for a given wavelength or spectrum depends on the bandgap of the absorbing layer ('absorber layer') in the P-N junction. From consideration of the 'detailed balance limit' or 'Shockley and Queisser limit' [25] the maximum theoretical efficiency of 33.2% for conversion of

the solar spectrum was found to be achievable when using an absorber bandgap of 1.34 eV [26]. Hence, absorber layer materials used for solar cells typically have a bandgap in the range of ~1.0-1.5 eV as shown in Figure 6. Silicon (Si), by far the most common material in commercial solar cells, has a bandgap reasonably close to this value ($E_{G,Si} \approx 1.17$ eV) but has a relatively low absorption coefficient due to its indirect bandgap, as shown Figure 3. Alternative direct bandgap semiconductors are InP (E_G = 1.34 eV), GaAs (E_G = 1.42 eV), CdTe (E_G = 1.5 eV) and the $Cu(In,Ga)Se_2$ (~ 1.2 eV).

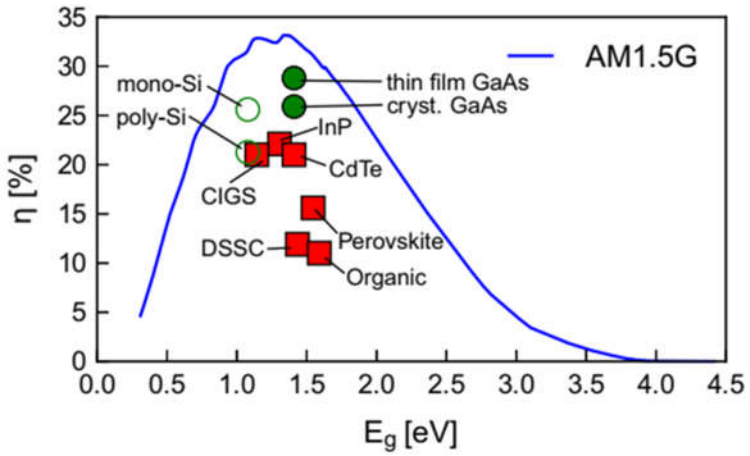


Figure 6 Plot of the theoretical limit in the photovoltaic conversion efficiency for a number of typical solar cell materials, as function of bandgap, calculated using the AM 1.5G standard reference spectrum for solar energy conversion on earth (see Figure 10) [26].

An important factor in limiting the charge carrier separation is the minority carrier diffusion length, since minority carriers need to be able to reach the depletion layer edge to be swept across the junction. Since electrons usually have a much larger minority carrier diffusion length than holes, most solar cells are designed to have the P-side of the junction as absorber layer where electrons form the minority carriers. This requires a much lower doping on the P-side than on the N-side so that $W \approx x_P$. The combination of materials used to form the P-N junction also has an important influence on the device efficiency. If the same semiconductor material is chosen for the N-side and P-side (a homojunction) the interface will be formed with the same crystal lattice on both sides, resulting in few interfacial defects and limited effects of interface recombination. When using two different semiconductors (forming a heterojunction) the lattice mismatch is likely to result in a much higher concentration of interfacial defects so that interface

recombination will be more likely to limit collection efficiency. Also, a difference in bandgap will lead to a difference between the CBE and/or the VBE on both sides of the junction which translates into a Conduction Band offset (CBO) and/or Valence Band Offset (VBO). The presence of a CBO and VBO can form a barrier for photogenerated charge carriers.

At the same time, in a heterojunction the equal bandgap on both sides results in comparable absorption coefficients, while from the consideration of the lower minority diffusion length of holes absorption on the N-side is less desirable. Hence in this case a very thin layer of N-type material is more important to optimize carrier collection. An advantage of heterojunctions is that absorption in the N-type material can be prevented by using a high bandgap material that doesn't absorb in the spectrum relevant for absorption on the P-side.

Typical components present in solar cells in addition to the P-N junction and front-/back-contacts are window layers, buffer layers, and Anti-Reflection (AR) coatings. The presence of these additional materials is intended to increase efficiency of carrier transfer to front- and back-contacts, act as diffusion barriers, increasing the absorption (by e.g. limiting reflection losses or increasing reflection back into the absorber layer), reduce shunting effects and interface recombination [6]. A few examples of such components relevant for CIGS based devices are discussed in more detail in Chapter 2.

1.2.2 Description and analysis of solar cell behaviour

From the electrical behaviour of a P-N junction given in section 1.1.2, a single-junction solar cell can be modelled with the circuit shown in Figure 7. The diode with current density J_D (Equation 1.10) describes the behaviour of the P-N junction in the dark, and an ideal current source is used to model the current density J_L produced under illumination. The current density J_L depends on the intensity of incident light (with $J_L = 0$ mA/cm^2 in the dark) and is usually assumed to be independent of bias. The series resistance losses occurring throughout the various components of the a solar cell are modelled with a single ('lumped') series resistance R_S, and shunting losses are modelled with a single parallel or shunt resistance R_{Sh}. The total current density J through a solar cell can then be expressed as

$$J = J_D + \left(\frac{V - JR_S}{R_{Sh}}\right) - J_L \qquad 1.7$$

In Equation 1.8 the diode current J_D given by

$$J_D = J_0 \left(\exp\left(\frac{q(V - JR_S)}{AkT}\right) - 1\right) \qquad 1.8$$

With A the ideality factor and J_0 the reverse saturation current density. An ideal solar cell without series resistance and shunting losses would have R_S = 0 $\Omega \cdot cm^2$ and R_{Sh} = ∞ $\Omega \cdot cm^2$. The effects of illumination, R_S and R_{Sh} are illustrated in Figure 8.

It should be noted that in actual devices care needs to be taken as to the range of bias, current and illumination intensities that is used for estimating values of R_S and R_{Sh}. These variations are caused by the different possible origins to both series and shunt resistance in actual devices. Also J_L typically has some bias-dependence [6] [27] [28] [29].

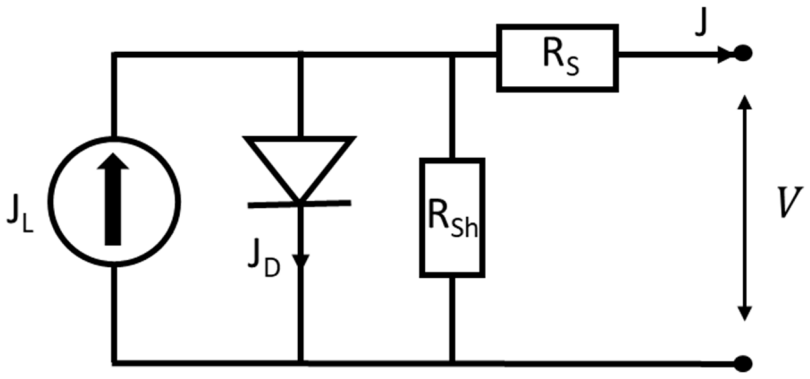


Figure 7 Model circuit of a simple solar cell

In the expression of the diode current J_D shown in Figure 7, the ideality factor A and reverse saturation current density J_0 can also contain non-idealities in the diode behaviour, related to recombination mechanisms other than standard band-to-band recombination. In Chapter 3 a more detailed description will be given about how these parameters can be used to distinguish the different recombination mechanisms.

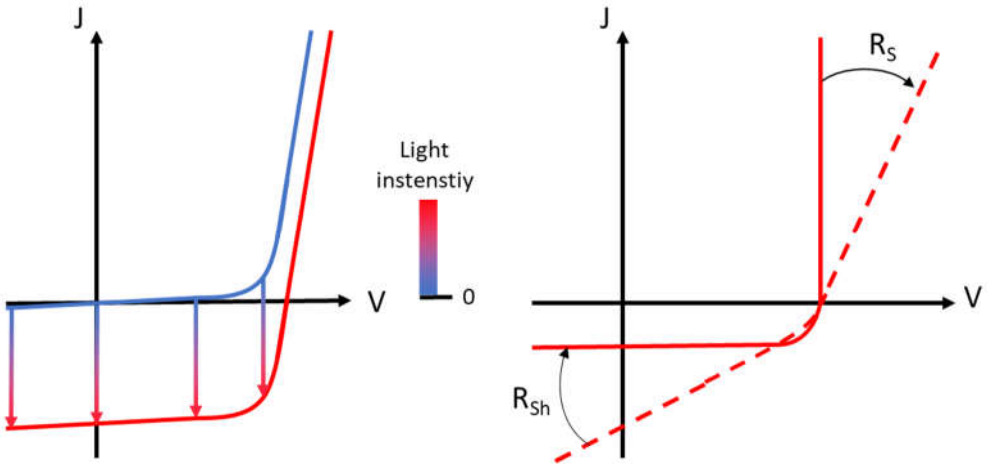
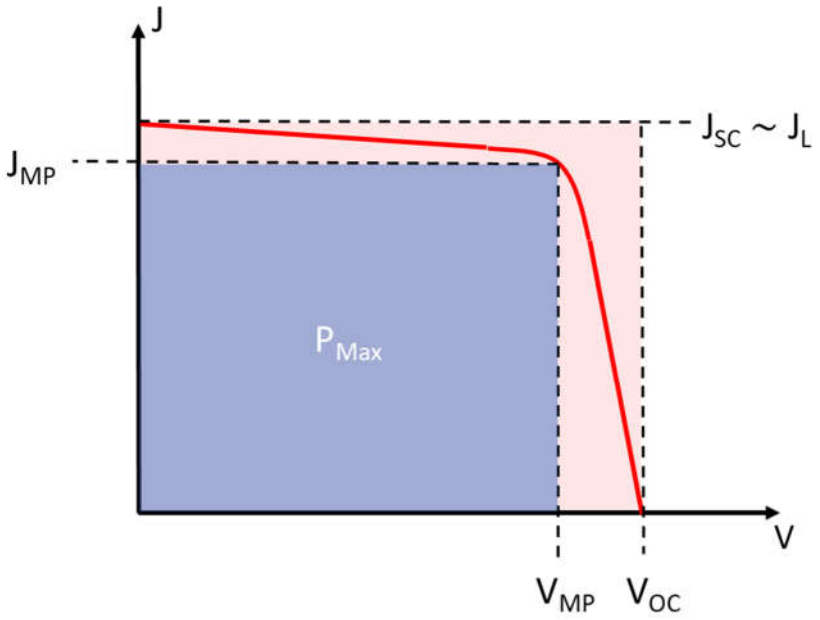


Figure 8 Current-voltage (IV) characteristics of a solar cell, with effects of illumination, series resistance and shunt resistance. Left: IV-curve in the dark (blue line) and under illumination (red curve), arrows indicate curve shift with increasing light intensity. Right: Illuminated IV-curve in the ideal case where $R_{Sh} = \infty$, $R_S = 0$ (full-line) and for lower R_{Sh} and higher R_{Sh} (dashed line)

In the dark $J_L = 0$ and the solar cell acts as a normal diode in presence of the resistances R_S and R_{Sh} in the circuit. Approximate values of R_S and R_{Sh} can be obtained from the dark IV characteristics from the inverse slope $\left(\frac{dJ}{dV}\right)^{-1}$ at the bias regions where the respective resistances are expected to dominate. Typically, R_S is fitted at high forward biases where linear (Ohmic) behaviour is observed and R_{Sh} is derived from the region close to 0 V.

Under illumination, the shape of the IV-curve would ideally remain unchanged with respect to the dark curve, with the total current resulting from the sum of the dark current J_D and light generated current J_L, i.e. $J = J_D + J_L$. The power that can be produced by the solar cell is then given by the product of the current and voltage in the fourth quadrant if IV-characteristics are plotted as shown in Figure 8. Often, to obtain positive values of generated power the IV-curve is plotted as shown in Figure 9 with opposite sign of the current.



$$\eta = \frac{V_{MP} \cdot J_{MP}}{P_{In}} = FF \cdot \left(\frac{V_{OC} \cdot J_{SC}}{P_{In}}\right) \qquad FF = \frac{V_{MP} \cdot J_{MP}}{V_{OC} \cdot J_{SC}} =$$

Figure 9 IV-curve of an illuminated solar cell (corresponding to the fourth quadrant of Figure 8 with indications of the open-circuit voltage V_{OC}, short-circuit current J_{SC}, and maximum power-point (MPP) with corresponding current J_{MP} and voltage V_{MP}. The expressions of the Fill Factor (FF) and solar cell efficiency (η) are also shown, with P_{In} referring to the total power density of incident light.

Under illumination, the open-circuit voltage or V_{OC}, short-circuit current or J_{SC}, and the current density J_{MP} and voltage V_{MP} at the point at which maximum power is produced (MPP, with power density P_{Max}) are important parameters to analyse the solar cell performance. The power P_{Max} measured under standard testing conditions (see below) is often expressed in the special unit 'Watt peak' (W_P). By comparing V_{OC}, J_{SC}, V_{MP} and J_{MP} the Fill Factor (FF) can be calculated according to

$$FF = \frac{V_{MP} \cdot J_{MP}}{V_{OC} \cdot J_{SC}} \qquad 1.9$$

As shown in Figure 8, in the ideal case where $R_S = 0$ and $R_{Sh} = \infty$, the illuminated IV-curve would be rectangular, with maximum power P_{Max} given by $P_{Max} = V_{OC} \cdot I_{SC}$ (I_{SC} the short-circuit current) in which case $FF = 100\%$. For a real device $V_{MP} < V_{OC}$ and $J_{MP} < J_{SC}$, so that $0\% < FF < 100\%$ and the deviation of FF from 100% gives an indication of device quality.

The most complete indication of solar cell performance is given by the conversion efficiency η, defined as the ratio of the maximum power P_{Max} and total power of incident photons P_{In}, as show in Figure 9:

$$\eta = \frac{(V_{MP} \cdot I_{MP})}{P_{In}} = FF \cdot \frac{(V_{OC} \cdot I_{SC})}{\Phi_{In} \cdot (area)} \qquad 1.10$$

with Φ_{In} the flux of incident power (W/m^2). This expression indicates the sensitivity of the calculated efficiency to the illumination intensity and the actual area of the device used during measurement. The efficiency η also depends on the exact spectrum used for measurement since the conversion efficiency of a solar cell usually varies strongly with wavelength (this is referred to as the spectral response or 'Quantum Efficiency' (QE) as described in Appendix A. Measurement techniques. In consideration of the sensitivity of obtained results to measurement conditions, well-defined standard test conditions (STC) have been established. The current international standards are measurement at 25°C cell temperature and 1000 W/m^2 illumination with the 'air-mass' 1.5G (AM 1.5G) spectrum as shown in Figure 10. This spectrum is calculated assuming solar insolation at 41.8° above the horizon and taking into account absorption in the earth's atmosphere as well as diffuse light [26] [30]. In addition to measurement conditions, also the area that can be used for defining the efficiency follows strict guidelines [18].

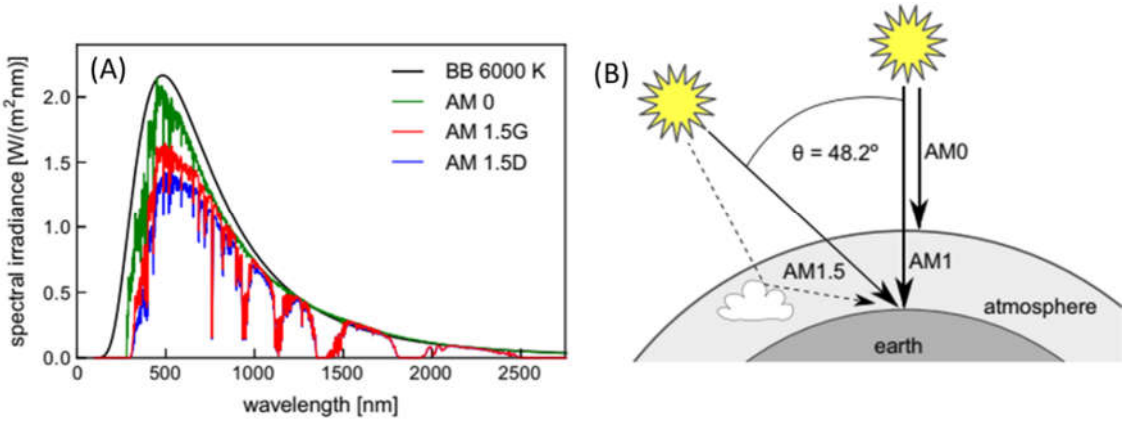


Figure 10 A: Standard reference spectra used to model the solar spectrum outside of the earth's atmosphere (AM 0, green), at the earth's surface only considering light at direct incidence (AM 1.5D, blue), at the earth's surface considering both direct and diffuse light (AM 1.5G, red), radiation from a black-body at 6000 K (BB 6000 K, black line). B: Corresponding insolation assumed for each spectrum [26]. The AM 1.5G spectrum is considered as the standard in the remainder of this thesis.

2 $Cu(In,Ga)Se_2$-based Thin Film Solar Cells

INTRODUCTION

As treated in the introduction of this thesis, TFSC's are a relatively new technology in PV allowing a much smaller amount of material per unit of produced power (i.e. lower g/W_P ratio) and a much wider range of applications than the more conventional Si-based devices. The wider range of applicability in e.g. Building Integrated Photovoltaics (BIPV) will become increasingly important considering the continued growth of the photovoltaic industry predicted for the next decade [14] [31] [32]. The quaternary semiconductor $Cu(In,Ga)Se_2$ (CIGS) is one of the most promising materials for TFSC's. It has a direct bandgap in the ideal energy range for solar energy conversion (1.04-1.68 eV), which results in an absorption coefficient of $\sim 10^5$ cm^{-1}, sufficient to absorb most incident light within a few μm's [33] [34]. The possibility to apply CIGS for PV was already realized in the early 1970's, when the first solar cells based on bulk single crystal $CuInSe_2$ (CIS) quickly reached conversion efficiencies exceeding 10% [35] [36]. The first thin-film devices followed shortly after and had initial efficiencies limited to ~5-6% [34], but owing to much research and development currently with CIGS the 20% efficiency record has been exceeded by various groups. In Figure 11 the progress in CIGS-based devices over the past 30 years is shown, with a number of sudden jumps in record efficiencies reflecting different discoveries in best preparation approach and architecture. Since the improvements don't show a sign of saturation yet it is expected that it will be possible to get closer to the theoretical limit of 30%.

On the laboratory scale, the verified efficiency record is currently at 22.6% [37] [18], which already exceeds the current record efficiency of 22.0% on the same scale devices based on multi-crystalline Si. Transferring the high efficiencies of CIGS lab-scale cells to the modular scale has been a challenge due to issues in scaling up the most successful deposition techniques. Nevertheless, the 19.2% efficiency record currently reached on CIGS modules is only slightly lower than the 19.9% record for comparable poly-Si modules and proves CIGS technology can be

highly competitive with conventional c-Si. Significant cost reduction in CIGS TFSC's are to be expected once further upscaling of production is achieved [38].

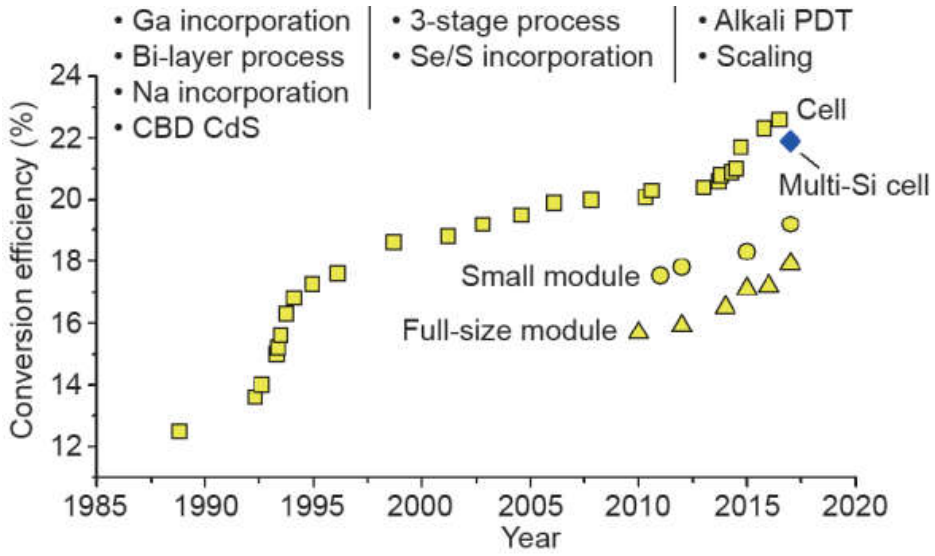


Figure 11 Graph showing the progress in conversion efficiency in laboratory scale (squares), small modules (circles) and full-size modules (triangles) CIGS-based TFSC's([38]

2.1 TYPICAL ARCHITECTURE FOR CIGS DEVICES

The conventional architecture for CIGS-based TFSC's shown in Figure 12 is based on a structure invented in 1987 at Arco Solar [6]: a Soda Lime Glass (SLG) substrate/Molybdenum (Mo) back contact/CIGS absorber layer/Cadmium Sulfide (CdS) buffer layer/thin intrinsic Zinc-Oxide (i-ZnO) high resistive window (HRW) layer/and an aluminium doped Zinc-Oxide (Al-ZnO) low resistance window (LRW) layer. In this architecture the P-N junction is formed close to the CIGS/CdS interface, by P-type CIGS and N-type CdS. Below, the function, deposition approach and material choice are explained and motivated for each layer. A more detailed description of the different deposition techniques for the CIGS absorber will follow in section 2.4.

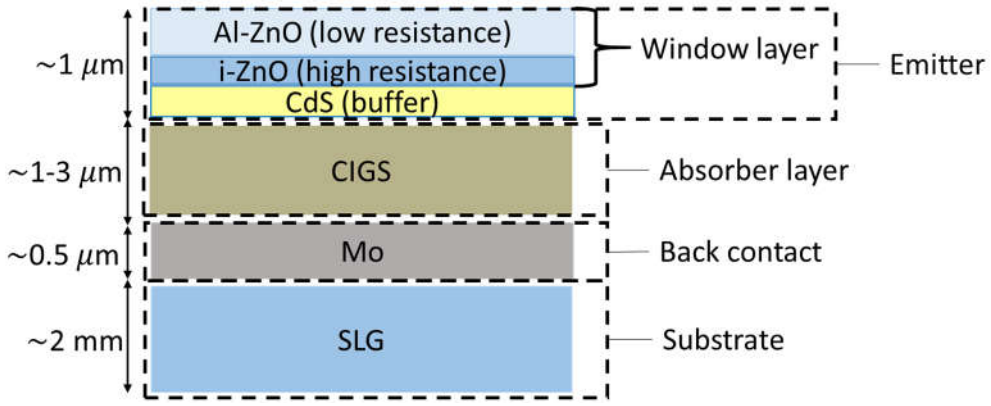


Figure 12 Schematic representation of the conventional architecture used for CIGS-based TFSC's. The active part of the solar cell can be roughly divided into an emitter, absorber and back-contact, where the emitter consists of three layers: buffer-layer, high resistance window (HRW) layer and low resistance window (LRW) layer. The materials in this figure indicate the most common choice of materials for CIGS-based solar cells. In the text some alternatives are also described.

Substrate: Soda Lime Glass (SLG)

For thin film devices a substrate material is essential to offer mechanical support to the solar cell. The choice for SLG in CIGS-based devices was initially made in consideration of its wide availability, high durability to both the CIGS deposition conditions and normal operating conditions, and low cost. The later realization that sodium (Na) diffusion from the SLG substrate into the absorber layer during CIGS deposition leads to improved device performance made SLG the standard choice for substrates in CIGS-based devices [39, 40].

The numerous investigations performed during the past decade (see e.g. [6, 41] [42] [43] [44] [45] [46] [47, 48]) have increased the understanding of effects of Na-doping device performance, but at the same time much is still unclear or topic of discussion. Alternative approaches to supplying Na during the CIGS deposition [6, 49, 50, 41] have allowed SLG to become successfully substituted by other materials, mainly flexible metallic foils and polymers (polyimides). Metallic foils have the advantage of good resistance to temperatures well above the typical ~500 °C used for CIGS deposition, but the disadvantage of a relatively high diffusivity into the absorber layer. To prevent diffusion of metals into the CIGS absorber, a diffusion barrier (typically SiO_2 or Si_3N_4) can be placed between the metallic substrate and the Mo-back contact. The most suitable metals

for application as substrate for CIGS were found to be aluminium (Al), tin (Ti), nickel (Ni) alloys and stainless steel. Highest efficiencies, in the range of ∼17.7-17.9%, have been reached on Ti substrates [51]. Polyimides have the advantage of being electrically insulating, allowing easier monolithic interconnection on large areas. They also don't contain impurities that could diffuse into the absorber layer. However, their inability to withstand temperatures above 500°C makes them unsuitable for application in the deposition approaches that until now allow reaching highest efficiencies. They also typically bend after deposition of the Mo-back contact, but this can be prevented by applying an insulating material on the back. The record efficiency reached on polyimides is currently at 20.4% [51, 52].

Back-contact: Molybdenum (Mo)

The choice for Mo as back-contact in CIGS-based devices was made in consideration of its low contact resistance with the CIGS absorber, low diffusivity in the CIGS absorber, relatively low cost and high melting point (∼2700 °C) [6, 53, 54]. A layer of ∼300-1000 nm Mo is usually DC-sputtered directly onto the substrate at room temperature or deposited by electron beam evaporation at 300-400 °C [6]. To achieve good adhesion to the substrate and low resistivity at the Mo/CIGS a 'bilayer' structure is usually deposited: a first deposition at high pressure results in a layer with good adhesion to the substrate, a second deposition at lower pressure results in a layer with low resistivity [53].

The low resistivity at the CIGS/Mo interface has been correlated to formation of a $MoSe_2$ layer between CIGS and Mo at sufficiently high CIGS deposition temperatures [55] [56] [57]. The layered structure of $MoSe_2$ allows diffusion of Cu, In, Ga and Se from the absorber into the Mo, resulting in chemical intermixing at the Mo/CIGS interface and formation of either an Ohmic contact or a Schottky barrier [58]. The band-alignment between CIGS/$MoSe_2$/Mo was found to limit electron recombination at the back contact, thus improving carrier collection [58]. The thickness of $MoSe_2$ layers formed during the CIGS deposition strongly depends on substrate temperature, Ga-grading and presence of Na in the absorber. While the highest observed thicknesses were ∼100 nm, in samples without Na no $MoSe_2$ could be detected [6].

As will be discussed in Chapter 4, the low deposition temperature of 250°C used in LTPED doesn't allow formation of a $MoSe_2$ layer. Nevertheless, by supplying sufficient Na ohmic- or near-ohmic contacts have been obtained (see [54] and Appendix B).

Absorber layer: $Cu(In_{1-x}Ga_x)Se_2$ (CIGS)

In addition to having a suitable bandgap for photovoltaic applications, CIS and CIGS have also shown a relatively high tolerance to compositional variations and good durability under normal operating conditions. This allows some tunability in important electrical properties such as bandgap and conductivity type without loss of absorber quality. This section contains a description of the most common compositions of CIGS used for photovoltaic applications, while a more general description of CIGS material properties follows in section 2.2.

The thickness of CIGS absorber layers usually lies in the range of 1-3 μm. Although good light absorption would already be achieved using only 0.1-1 μm of CIGS, a thickness of at least 1 μm was found necessary to prevent openings occurring in the absorber layer which would form shunting paths [59]. Upper limits to the absorber layer follow from the maximum diffusion length of minority carriers, which should be able to reach the space charge region (SCR) from the bulk or neutral region of the absorber, and the diffusivity of dopants such as Na, which should be able to diffuse throughout the entire absorber to result in homogeneous doping.

The most important variables in CIGS composition are the relative Cu-content, expressed as Cu/(In+Ga) or CGI, and the relative Ga-content, expressed as Ga/(Ga+In) or GGI. Variation of the CGI leads to variations in the phase and conductivity type of CIGS (see section 2.3). For good absorber layer quality, the bulk conductivity needs to be P-type which is achieved for CGI ~0.9, i.e. slightly Cu-poor compared to stoichiometric composition. Variation of the GGI leads to variations in the bandgap, where GGI = 0 corresponds to ~ 1.04 eV and GGI = 1 corresponds to ~1.68 eV. The best device efficiencies have been reached using GGI ~ 0.3, corresponding to a bandgap of ~ 1.2 eV. Although this is slightly lower than the theoretically ideal bandgap of ~1.4 eV for conversion of solar light as treated in Chapter 0 [25] [26], increasing the GGI beyond ~0.3

leads to only limited increase in V_{OC} and reduced device performance, most likely due to increased interface recombination (see section 2.3.1) [60] [61] [62].

A common approach to optimizing collection efficiency in CIGS-based devices is by implementing a variation of the GGI along the depth of the absorber layer to obtain a 'bandgap-grading'. Highest efficiencies have been reached with this approach using the 'notch'-profile', which has a bandgap reducing from the CIGS/Mo interface towards the absorber bulk, where it reaches a minimum before it increases again towards the CIGS/CdS interface. The increased bandgap close to the CIGS/CdS interface results in a higher electric field at the SCR, which results in a larger electron drift diffusion length and thus improves the collection of photo-generated minority charge carriers. Similarly, the increased bandgap and corresponding increased electric field toward the CIGS/Mo interface leads to partial compensation of the typically high recombination velocity at the back-contact [63].

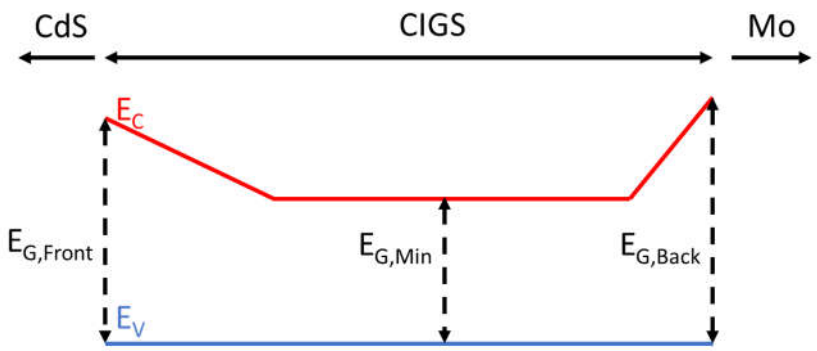


Figure 13 Example of a band-diagram for a CIGS absorber layer with a 'notch' profile

During the past decades of research and development of CIGS thin films for solar cells, sequential processing and co-evaporation have proven to be the techniques allowing highest control of the most relevant deposition parameters to obtain good compositions. These are still the techniques with which the highest efficiencies are obtained in CIGS devices, and will be described in more detail in section 2.4. Devices prepared using other deposition techniques used on smaller scale such as closed space sublimation, reactive sputtering, chemical bath deposition and electrodeposition usually still lag behind in efficiency [63].

The samples investigated for this thesis were deposited using the Low Temperature Pulsed Electron Deposition technique (LTPED) developed at IMEM-CNR. This technique and the specific preparation approach for LTPED-devices is discussed separately in Chapter 4.

Buffer layer: Cadmium Sulfide (CdS)

The bandgap of Cadmium Sulfide (CdS) (∼2.4 eV) makes it transparent to most of the light absorbed by CIGS, while the small lattice mismatch between the CdS and CIGS crystal lattices allow formation of a hetero-interface which suffers relatively little from interfacial states. Mainly these two points make CdS a suitable choice for buffer layer material in CIGS-based devices. Originally, CdS was also expected to form the N-side of the P-N junction in CIGS based devices. However, in more detailed investigations of the structure of good performing CIGS-based devices the N-side of the junction was found to be formed by a thin layer of type-inverted CIGS (i.e. with N-type rather than P-type conductivity) located at the interface between the CIGS absorber and the CdS buffer layer (see section 2.3.1) [64]. The CdS layer has been suggested to play an important role in inducing the type inversion at the CIGS surface.

The introduction of the Chemical Bath Deposition (CBD) for CdS in the 1980's, which is still the standard approach to CdS deposition, was an important step for improving efficiency of CIGS-based TFSC's. In earlier deposition techniques ∼5-10 μm of CdS was evaporated onto the absorber surface [36] [35]. With CBD a better coverage of the absorber layer was obtained with much thinner layers of CdS (∼50 nm), resulting in both reduced shunting effects and much lower absorption losses [6].

In the attempt to eliminate the toxic element Cd from the standard architecture of CIGS devices alternative buffer layer materials are being sought. The most promising materials at the moment appear to be compositions of (Zn,Mg)(O,S). The higher bandgap in these materials (> 3.3 eV) leads to less parasitic absorption than in CdS. An additional advantage of alternative buffer layers is the possibility to change the deposition technique from CBD to a vacuum technique (e.g. sputtering) which might be performed directly after the CIGS deposition without having to remove the sample from vacuum. This would reduce the risk of surface contamination and

possibly improve the quality of the absorber/buffer interface. The current record efficiency of Cd-free CIGS based devices is at 22.3% [65]. Alternative buffer layer materials have also been investigated for LTPED devices [54].

Window layer: Zinc-Oxide (i-ZnO) and Aluminum doped Zinc-Oxide (Al-ZnO)

The window layer of a solar cell device has the contradictory requirements of a high optical transparency and a high conductivity to act as efficient front contact. The choice for ZnO in CIGS-based devices is made in consideration of the high bandgap, $E_G \geq 3.3$ eV, making it sufficiently transparent for light absorbed by CIGS. By Al-doping the ZnO (to obtain Al-ZnO) it's possible to achieve a material with both good transparency and good conductivity, that can therefore act as a low resistive window layer (LRW layer) for CIGS-based devices. However, finding the suitable doping and thickness for the LRW is difficult due to the trade-off between conductivity and transparency. Increasing layer thickness reduces resistance but also transparency. Similarly, increasing the doping level increases conductivity but reduces transparency since the free carriers absorb light in the infrared range. The best compromise is usually found to be a thickness of $\sim$200 nm and doping level of < 2% Al, which typically corresponds to a sheet resistance of $\sim$ 5-10 Ω/sq and transmittance of $\sim$90%. The LRW layers are usually deposited either by DC-sputtering in larger scale production, or RF-sputtering in laboratory scale devices [6].

Although reasonable efficiencies can be obtained using only an Al-ZnO LRW layer [66] [67], device performance can be improved by adding a thin highly resistive window layer (HRW layer) of i-ZnO onto the CdS buffer, usually deposited by RF-sputtering. This HRW layer can cover parts of the CIGS film where cracks occur or that haven't been completely covered by the CdS buffer layer. These zones would otherwise lead to shunting as the Al-ZnO can reach the Mo back-contact. Implementation of a HRW layer was also found to improve homogeneity of the device performance [40] [66]. There exists a critical thickness of the HRW layer below which shunting effects dominate, and above which the increased series resistance starts to have a negative impact on device performance [68] [69], which was found to be $\sim$50 nm and sheet resistance of $\sim$ 1 MΩ/sq.

Another important aspect in the choice of the window- and buffer layers in the CIGS architectures is the matching of their dielectric constants. In the standard architecture presented here, each successive layer deeper in the device (i.e. starting from the ZnO-layers) has a higher dielectric constant: the respective dielectric constants of the layers are ∼8 (ZnO), ∼10 (CdS) and 13.6 (CIGS) to. This limits the amount of reflectivity of the solar cell and allows reaching relatively high device efficiencies without AR-coatings [6].

Energy band diagram

To understand the efficiency with which charge carriers are collected in a solar cell, the line-up of the energy bands at the different interfaces ('band-alignments') in the device needs to be considered. For the interface between two semiconductors, the difference in bandgap ΔE_G and the requirement of a constant Fermi-level in equilibrium lead to a conduction band offset (CBO) and valence band offset (VBO), which to first approximation will be the same for any specific pair of semiconductor materials. Usually this allows obtaining an accurate approximation of the band-alignment by determining the VBO experimentally and calculating the CBO from ΔE_G as VBO = ΔE_G − CBO [6]. The resulting band-alignment throughout the device can be visualized in the energy band-diagram, shown in Figure 14 for a typical CIGS-based device (with constant bandgap in the CIGS absorber of E_G∼1.2 eV) [52]. In this diagram, the alignment at the CIGS/CdS and Mo/CIGS interfaces are particularly important in determining the final device performance. The CBE of CdS ($E_{C,CdS}$) is higher than that of CIGS ($E_{C,CIGS}$) resulting in a positive CBO or 'spike'. This forms a barrier for minority carrier electrons that need to be collected from the absorber. The VBE of the CIGS increases toward the CIGS/$MoSe_2$ interface and sharply decreases again at the $MoSe_2$/Mo interface. While the increased VBE between CIGS and $MoSe_2$ is favourable for hole transport, the sharp decrease at the $MoSe_2$/Mo interface forms a barrier for minority carrier holes.

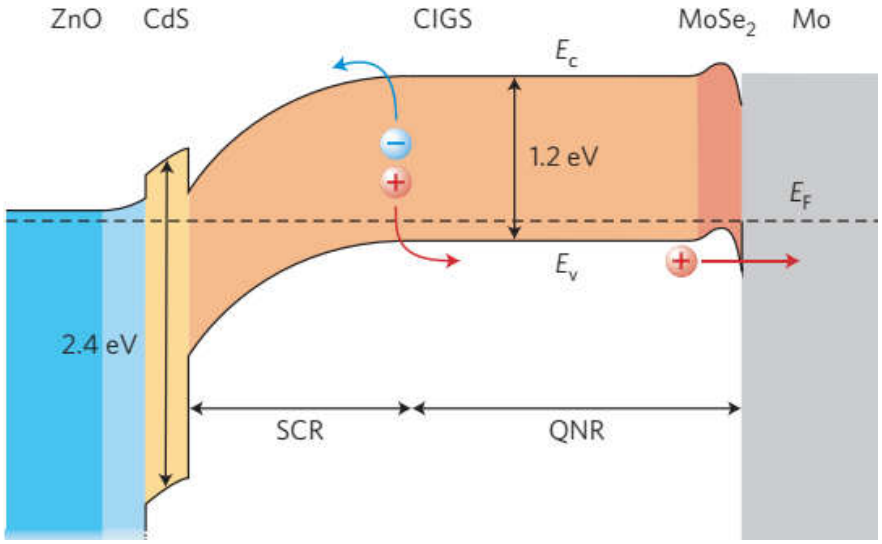


Figure 14 Schematic representation of the expected band-alignment in a typical CIGS-based device at 0 V bias [52], for constant GGI, and hence constant bandgap (E_G~1.2 eV). The upper and lower black-lines indicate the conduction band edge (E_C) and valence band edge (E_V) respectively. The bandgap of the ZnO layer is assumed to be in the range >3 eV. 'SCR' refers to the Space Charge Region (depletion region), while 'QNR' refers to the 'Quasi Neutral Region', i.e. the bulk of the absorber layer where no internal electric field is present.

In the band diagram shown in Figure 14 presence of a type-inverted CIGS layer close to the CIGS/CdS heterointerface [70] hasn't been taken into account. As will become clear in section 2.2 below, the N-type CIGS layer corresponds to a different phase which is often referred to as the 'Ordered Defect Compound'(ODC). The ODC-phase has a slightly higher bandgap than P-type CIGS (~1.45 eV for GGI = 0.3) and a VBO with CdS of ~0.65 eV which is independent of GGI. Presence of the ODC-phase layer is thought to reduce the CBO between the absorber and buffer [71] [8].

2.2 TYPICAL DEVICE BEHAVIOUR AND ANOMALIES

2.2.1 Record and baseline devices

To compare record efficiencies for any type of solar cell technology a clear distinction needs to be made between the laboratory scale and module scale. Higher efficiencies can always be obtained on the laboratory scale, as the smaller area ($\leq$ 1 cm^2) and the experimental nature of these devices allow more complex and expensive preparation approaches as proof of concept.

Modules consist of larger area cells connected in series, with at least 800 cm^2 total area taken into consideration in official comparisons [18]. Deposition on these larger areas inevitably leads to less homogeneity than on laboratory scale devices causing significantly lower performance on the module scale. In addition, the interconnections between the separate cells in the module lead to relatively large inactive areas, significant series resistance losses, and an output current which is limited to that of the lowest single-cell current [38].

The highest efficiency reached for CIGS-based on the laboratory scale is currently at 22.6% [37] [18], using a multi-stage thermal co-evaporation deposition process. The performance parameters of this cell were V_{OC} = 741 mV, J_{SC} = 37.8 mA/cm^2 and FF = 80.6%. The reported device had a slightly thicker absorber layer than the standard (~2.5-3 μm), was prepared with a post-deposition treatment in which Rubidium Fluoride was evaporated onto the CIGS surface in a Se atmosphere, and had a (Zn,Mg)O layer as HRW layer instead of i-ZnO. The most recent important step to achieve higher efficiencies (exceeding 21%) has been the implementation of a post-deposition treatment with alkali-fluorides in Se atmosphere to induce surface modification of the CIGS absorber.

The record efficiency on the module scale is limited to 18.7% on aperture areas of ~9400 cm^2 [72]. On commercial modules the nominal efficiency is currently ~15%. The module efficiencies can be expected to increase further, as the most recent laboratory scale discoveries (e.g. large scale incorporation of post-deposition treatments and substitution of i-ZnO with (Zn,Mg)O) will gradually be incorporated on the industrial scale [38].

2.2.2 Anomalies of CIGS-based devices

Non-ideal performance in CIGS-based devices is often visible in anomalies in the electrical characteristics. In the current section the most commonly observed ones related to metastability's and deformations in the IV-curves are described.

2.2.2.1 Deformations in IV-curves

The most important types of deformations usually observed in IV-curves of CIGS-based devices are i) the 'roll-over effect', ii) the 'cross-over' effect, iii) a 'kink' in illuminated IV-curve and iv) the violation of the shifting approximation. In Figure 15 an example is given for each effect.

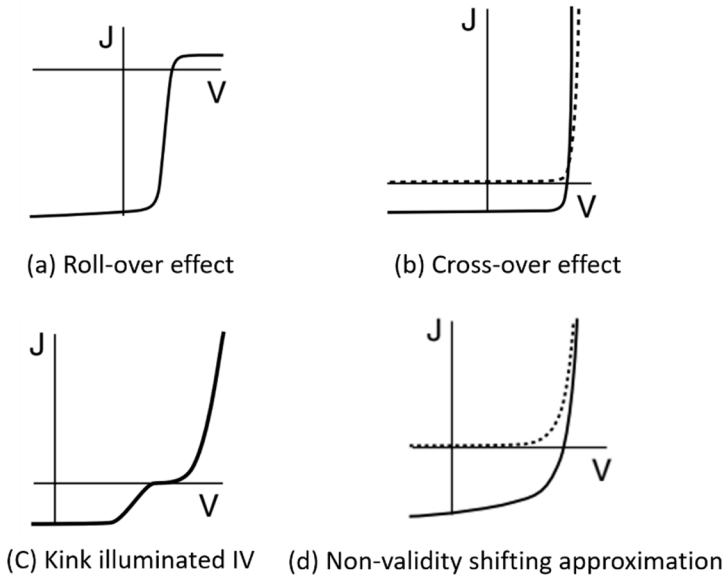


Figure 15 Typical deformations observed in non-ideal performing CIGS-based devices [6]

a) **Roll-over effect:** starting from a certain bias, the forward current saturates. This effect can be observed both in the dark and under illumination. It indicates a barrier to the forward current at the absorber/back, absorber/buffer or buffer/window layer interfaces.

b) **Cross-over**: The illuminated curve crosses the dark IV-curve due to a higher R_S in the dark than under illumination. This has been attributed to an electron barrier at the CdS/CIGS-

interface that is lowered under illumination, and/or minority carrier recombination at the back contact.

c) **Kink in illuminated IV-curve**: A strong bias-dependence of the photocurrent is observed, indicating a barrier. It can originate from a CBO at one of the absorber/buffer/window interfaces, a P^+-layer, or a conduction band gradient at the absorber surface.

d) **Violation of shifting approximation:** In the shifting approximation it is assumed that the dark and light IV-curves differ only by a constant current $\Delta J \sim J_{SC}$. This assumption can be inaccurate for significant variations in the illuminated R_{Sh} or R_S due to bias-dependent photocurrent, photoconductive shunting paths, or a change in the diode current between dark and illuminated conditions at low bias.

2.2.2.2 METASTABILITY AND TRANSIENT EFFECTS

In CIGS-based devices application of bias and/or illumination can induce changes in the electrical characteristics of the sample, most notably the open-circuit voltage (V_{OC}), fill factor (FF), capacitance (C), conductivity (σ), free carrier density (N) and net ionized charge concentration in the SCR. These changes can persist for several minutes or hours after removal of the excitation. Metastable states following excitation can be distinguished from the 'relaxed state', usually obtained by storing the sample in the dark at ~330 K for several hours [6] [5]. In the relaxed state CIGS-based devices demonstrate a low apparent acceptor density ($N_A \sim 10^{15}$ cm^{-3}), below optimal V_{OC} and FF, and significant differences between dark and illuminated IV-curves. Application of red-light illumination in the relaxed state can induce a 'kink' in the forward current, resulting from an electron barrier at the CdS/CIGS interface (see Figure 14 in section 2.1 above).

The performance of CIGS-based devices usually improves when exposed to white light for extended periods of time (i.e. 'light-soaking'). This results in an increased V_{OC}, FF, C and σ. The state of improved performance obtained after light-soaking is expected to be caused by the removal or lowering of current barriers in the device induced by the illumination. Investigations in which the effects of red light ($\lambda > 680$ nm, mainly absorbed in CIGS-layer) and blue light ($\lambda <$

480 nm, mainly absorbed in the buffer-layer) were studied separately, showed the two types of illumination had different effects.

Light-soaking with only red-light results in an increase in hole density p, mobility μ and apparent acceptor density $\mathrm{N_A}$, causing occurrence of persistent photoconductivity with time-constants in the order of hours, both at application and removal of the illumination [6]. The $\mathrm{V_{OC}}$ also often increases after red light treatment. For relaxed samples cooled to below 250 K red light showed no effect, while samples that had been soaked with red light and cooled to below 250 K didn't show relaxation. The effect of red light anneals out at 300 K. Light-soaking with only blue light leads to an increased FF and reduction of the cross-over effect. For samples demonstrating a 'kink' in the IV-curve due to red light illumination in relaxed conditions, blue light soaking removes the kink. Effects of blue light illumination reduce at low temperature, but don't disappear.

The effects of reverse and forward bias treatment have also been studied separately by various authors [73]. In this case the samples were usually kept at reverse bias (~ -1 V) or forward bias ($\sim +0.7$ V) for 1 hour at 300 K. The reverse bias treatment leads to a higher concentration of ionized states in the SCR at $\sim$0.35 eV from the VBE, a low FF, increased C and increased $\mathrm{N_A}$ with respect to the relaxed state. It can also result in hysteresis in the IV-characteristics, where measurements performed under decreasing bias result in a higher FF than those performed under an increasing bias. Below 300 K reverse bias treatment has no effect. Forward bias treatment results in an increased capacitance (and hence in $\mathrm{N_A}$ as explained in Chapter 3), and increased $\mathrm{V_{OC}}$. This state has also been found to lead to a reduction in the activation energy of a trap often observed in admittance spectroscopy ('N1', see Chapter 3) [74]. Both reverse- and forward-bias effects can be annealed out at temperatures of 340-360 K.

These metastable effects have been attributed to changes in the configuration of imperfections in the crystal lattice (defects) to applied excitations, as will be discussed in more detail in section 2.3.2 below. Although they can have a positive influence on device performance, the dependence of the performance of a device on its history makes interpretation of results from even the most

basic characterization technique non-trivial [75] [76]. In order to obtain reproducible results in the investigation of CIGS-based devices, well-defined initial conditions need to be established. The approach chosen to achieve this during this thesis is described in more detail in Chapter 3.

2.3 CIGS MATERIAL PROPERTIES

The presence of four different elements in CIGS leads to many possible compositions and corresponding phases, as explained in section 2.3.1 below. The differences in the electrical properties between each phase are partly due to differences in the concentration of imperfections in the crystal lattice (intrinsic defects). The intrinsic defects that are most important in determining the electrical behaviour in CIGS are described in more detail in section 2.3.2.

2.3.1 Phases and compositions

The phase of CIGS used as absorber layer material in solar cells is obtained by adding Ga to the ternary system Cu-In-Se. Partial substitution of In-atoms by Ga-atoms in the crystal lattice leads to formation of a solid-state solution between the two ternary compounds $CuInSe_2$ and $CuGaSe_2$, resulting in the composition $Cu(In_{1-x}Ga_x)Se_2$. Since the introduction of Ga has little effect on the equilibrium phases of the final compounds for temperatures below 800°C [43] [77] the equilibrium phases of CIGS can be derived from those of CIS, a material that has been topic of investigation since the 1950's [35] [36]. The most relevant phases of CIS for application in TFSC's are those on the connection line between the Cu_2Se and In_2Se_3 phases: the α- and the β-phase, the high temperature δ-phase, and Cu_2Se impurity phases. This is shown in the pseudo-binary equilibrium phase diagram in Figure 16.

The α-phase is the phase corresponding to the composition $Cu(In_{1-x}Ga_x)Se_2$ mentioned above, and has a tetragonal chalcopyrite crystal lattice (see Figure 17). It is also referred to as the 'photovoltaic quality phase'. Since it is the only phase in the CIGS system with P-type conductivity, it is ideally present in pure form in the absorber layer of CIGS based TFSC's. It exists in stable form for only a narrow range of Cu-poor compositions, with formation of the β-phase starting with Cu-

contents below 24 at%, and precipitation of Cu_2Se phases starting with Cu-contents above 24.5 at% [9] [78]. Complicated preparation techniques are required with accurate control of the Cu-content to obtain compositions in which pure α-phase CIGS is formed, as explained in section 2.4 below.

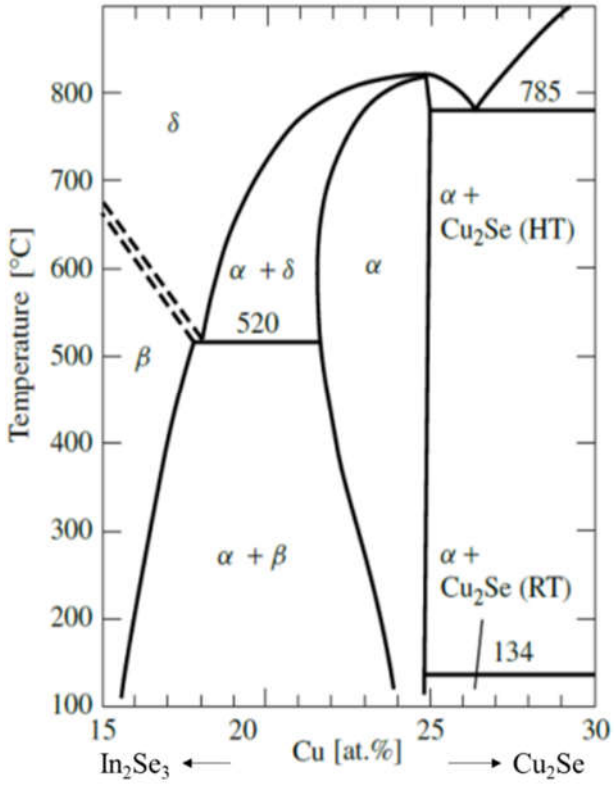


Figure 16 Pseudo-binary phase diagram on connection line between In_2Se_3 and Cu_2Se, for Cu-content close to the stability range of pure chalcopyrite $CuInSe_2$. [54] [79]

The formation of the N-type β-phase follows from the ordered insertion of Cu-related crystal defects with decreasing Cu-content (also see section 2.3.2). This results in a very similar crystal lattice as that for the α-phase (see Figure 17) but with off-stoichiometric compositions such as $Cu(In,Ga)_3Se_5$, $Cu_3(In,Ga)_5Se_9$, $Cu_2(In,Ga)_4Se_7$, $Cu_2(In,Ga)_4Se_7$ and $Cu(In,Ga)_5Se$ [59] [80] [20]. In consideration of the high concentration of ordered defects in the β-phase, it is commonly referred to as 'Ordered Defect Compound' (ODC), 'Ordered Vacancy Compound' (OVC) and 'defect chalcopyrite'. In the remainder of this thesis the terms β-phase or ODC-phase will be used.

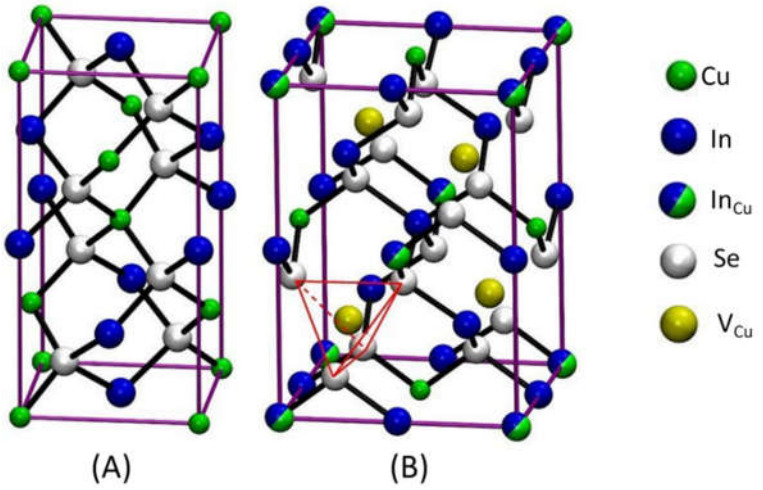


Figure 17 Two crystal structures corresponding to the dominant two phases of CIS: (a) the α-phase or photovoltaic quality phase with chalcopyrite crystal structure. With Ga addition, blue lattice sites will become occupied by either In or Ga atoms (b) the β-phase with defect chalcopyrite structure, formed at ordered insertion of Cu-related defect complexes (i.e. ($2V_{Cu}$-In_{Cu}), see section 2.3.2) [81]

While the absorber bulk is ideally free of any N-type phases such as the β-phase, a thin 'ODC-layer' has been found at the CdS/CIGS interface in various investigations (see section 2.1). This thin layer of N-type material has been found beneficial for device performance, possibly because it allows formation of a P-N homojunction with low interface roughness and limited effects of interface recombination and promotes good band-alignment between the absorber surface and the CdS buffer layer [70] [64] [82]. The origin of the thin N-type layer was suggested to be a type-inversion at the absorber surface induced during the CBD of CdS. Presence of the thin ODC-layer was also found as possible explanation for the metastable behaviour described in section 2.2 [82] [8]. However, it should be noted that there is still much discussion regarding the formation of the ODC-layer, its exact composition and its role in the behaviour of good quality CIGS devices. Also during this thesis a number of LTPED samples has been investigated in which it was attempted to add an ODC-layer with LTPED. The results of these investigations are presented in Chapter 5.

The stability of the different phases of CIGS strongly depends on the composition. As more Ga is added to the system, the stability range of the α-phase increases while that of the β-phase decreases. For compositions with GGI < 0.3 the P-type α-phase can still be converted to the N-

type β-phase, while for GGI > 0.3 the β-phase becomes unstable, and even when introducing extrinsic dopants highly resistive or slightly P-type material is usually obtained instead of N-type material [60] [82] [54] [62] [83]. The lattice mismatch between the α- and β-phase was also found to increase with higher Ga-content, so that a possible explanation of the disappointing increase in V_{OC} with higher Ga devices mentioned in section 2.1 might be a higher concentration of interfacial states resulting in increased recombination [71] [83] [62].

The formation of the 'high-temperature' δ-phase occurs at temperatures above 800 °C as the chalcopyrite structure changes to a disordered zinc-blende crystal structure [20]. Formation of the δ-phase is prevented relatively easily by controlling the deposition temperature. The Cu_2Se impurity phases precipitate from the chalcopyrite crystal lattice at high Cu-content, forming a 'quasi-liquid'. As explained in section 2.4, the Cu_2Se phases can help improve the quality of the final CIGS film during growth [60] [84].

2.3.2 Intrinsic defects

As mentioned above, the native defects in CIGS strongly influence the phase, conductivity type and crystal structure of the material [85] [84] [86] [63] [87] [88] [89] [90] [91]. Hence, considering the different type of native defects typically present in CIGS and how they influence these important material properties is important to understand the behaviour observed in a CIGS-based device.

An imperfection at a single lattice point of any of the four species composing CIGS leads to formation of a *point defect*. Three types of point defects can be distinguished:

- **Vacancies (V_A):** empty lattice sites ('V') that in the perfect crystal would be occupied by species 'A'. Vacancies can usually diffuse through the crystal, as atoms can move between neighbouring lattice sites
- **Antisite defects (A_B):** lattice sites occupied by species 'A' which in the perfect crystal would be taken up by species 'B'.
- **Interstitials** (A_i): spaces in between lattice sites ('i') occupied by species 'A' that would be unoccupied in the perfect crystal

Each of the four elements composing CIGS can form one vacancy, one interstitial and three antisite defects, giving a total of 20 different possible point defects in the CIGS crystal lattice. The likelihood of formation of each defect will increase with reducing formation energy. Generally, only a few defects will have low enough formation energies to be present in significant concentrations. Mainly V_{Cu}, (V_{In},V_{Ga}), V_{Se}, (Cu_{In},Cu_{Ga}), (In_{Cu},Ga_{Cu}) and Cu_i are expected to be present in CIGS (here In and Ga can be interchanged in the defect types). In Table 2 the different formation energies of the most important defects in CIS are shown, together with an indication of the defect type (deep/shallow donor/acceptor) [20]. For the typical Cu-poor/In-rich composition with P-type conductivity, the order of formation energies was calculated as $V_{Cu} < In_{Cu} < V_{In} < Cu_{In} < Cu_i$ [20].

Table 2 Range of formation energies and average formation energy as obtained by first princuple calculations presented in [20]. The V_{In}, Cu_{In} and In_{Cu} defect states can have different charge configurations with different energy levels inside the CIS bandgap.

Defect	Range of formation energies	Average	Type
V_{Cu}	$-2.41 \leq \Delta E \leq 0.63$	-0.89	Shallow acceptor
V_{In}	$-0.83 \leq \Delta E \leq 4.29$	1.73	Deep acceptor
Cu_{In}	$-1.67 \leq \Delta E \leq 4.41$	1.37	Deep acceptor
In_{Cu}	$-0.15 \leq \Delta E \leq 5.93$	2.89	Deep donor
Cu_i	$2.04 \leq \Delta E \leq 5.08$	3.56	Shallow donor

Figure 18 also shows a comparison between experimentally observed acceptor and donor levels in CIGS, and the energy in the CIGS bandgap calculated for the different intrinsic defects [6] [92]. Combining the results from first principle calculations and experimental observations, it was concluded that the electrical properties in CIGS absorber layers are mainly determined by variations in the relative concentration of In_{Cu} and V_{Cu} defects. The intrinsic P-type doping in the α-phase is attributed to presence of V_{Cu} defects forming a shallow acceptor level $\sim$30 meV above the VBE.

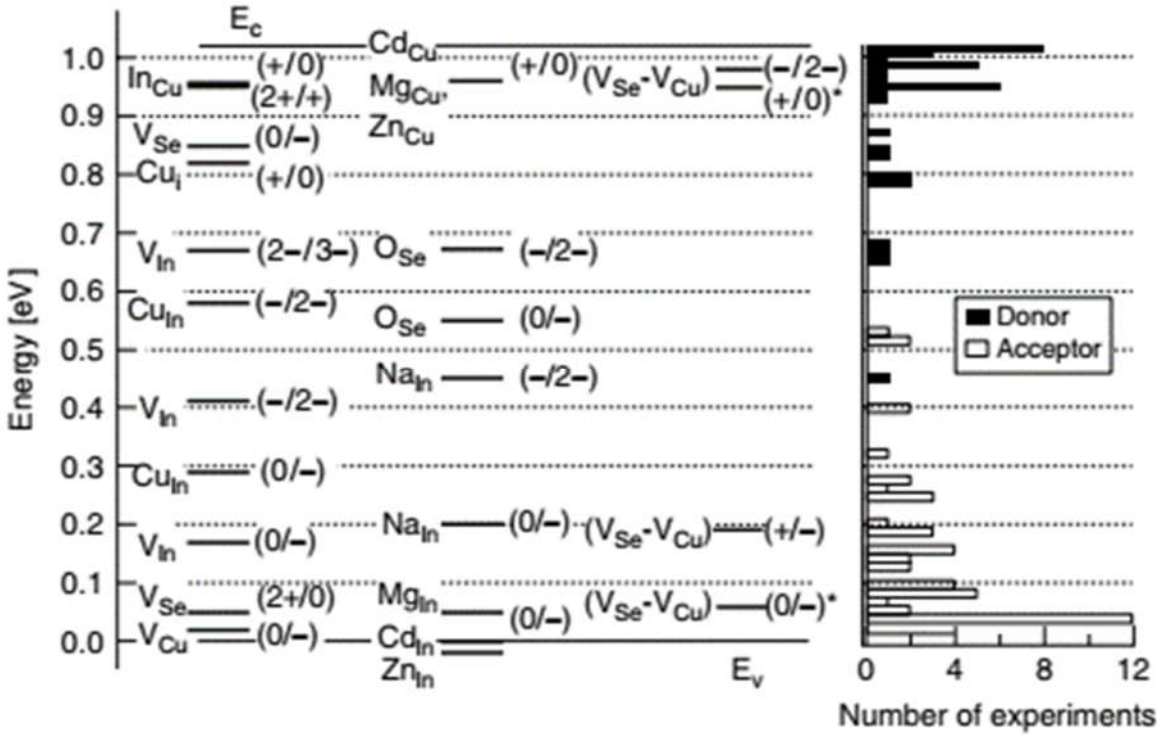


Figure 18 Theoretically calculated energy levels of defects in $CuInSe_2$ compared to experimentally determined energy levels. White bars correspond to donor levels, black bars correspond to acceptor levels [6]

Formation of In_{Cu} defects is expected to result in formation of deep donor levels ~340 meV below the CBE which compensate the intrinsic P-type doping [20].

The stability of the α-phase for moderately Cu-poor CIGS compositions is due to the favourable formation energy of electrically neutral ($2V_{cu}^{-} + In_{Cu}^{2+}$) defect complexes from V_{Cu} and In_{Cu} defects. At low concentrations, presence of these neutral defect complexes doesn't affect the phase or electrical behaviour of the material. As the Cu-content is reduced (below 24.0 at% for CIS, see Figure 16) formation of 'defect arrays' becomes energetically favourable and a transition from the α- to the β-phase takes place.

The influence of Ga on the stability of the α- and β-phase mentioned in section 2.3.1 above follows from the higher formation energy of Ga_{Cu} defects than that of In_{Cu} defects. This causes a decrease in the total concentration of compensating $(In,Ga)_{Cu}$ donors and ($2V_{Cu} + (In,Ga)_{Cu}$) defect complexes at similar Cu-contents and increasing Ga-content. Lower compensation and a lower

concentration of defect complexes results in in the larger stability range of P-type conductivity (α-phase) and a smaller stability range of the ODC-phase or β-phase [62].

Due to their very low formation energies V_{Se} defects are also expected to be present in high concentrations, and play an important role in device behaviour. However, the precise effect of these V_{Se} defects isn't widely agreed upon. Since the defect can occur in charge states from +2 to -2, it can act as both electron or hole trap. Most of the V_{Se} defects are expected to be present in defect complexes ($V_{Se} + V_{Cu}$), which can act as donors in the $(V_{Se} + V_{Cu})^{+}$ state or as acceptors in the $(V_{Se}+V_{Cu})^{-}$ or $(V_{Se}+V_{Cu})^{-2}$ states. These defect complexes can't lead to stable N-type or P-type conductivity, but transitions between their different charge states have been proposed as explanation for the metastable effects induced by external excitations described in section 2.2.2.2 [6] [93].

Another important defect type in addition to the point defects and defect complexes mentioned above are 'grain boundaries', i.e. the boundaries between zones with differences in crystal orientation, crystal structure and/or phase. These two dimensional defects are inherently present in any polycrystalline materials and usually severely limit the performance in thin film solar cells. However, in CIGS the negative effect of grain boundaries is known to be relatively small [6], which is possibly explained by a high Cu-depletion and hence a high density of V_{Cu} defects at these boundaries. This would result in the formation of a neutral hole barrier which limits recombination [92, 94]. Also, certain extrinsic dopants such as Na that are used for CIGS thin film absorber have been proposed to reduce the negative effects of grain boundaries, as explained in more detail in the following section 2.3.3.

2.3.3 Extrinsic dopants

In addition to the dominant role of intrinsic defects discussed above, a number of extrinsic dopants are commonly used in CIGS absorbers since they are known to be important to achieve good absorber quality and device performance. The most important ones described below are alkali elements (Na, K, Cs and Rb) and Cd.

As mentioned in section 2.1, doping the CIGS absorber with Na or other alkaline materials has become recognized as an essential step to obtain good electrical quality in CIGS-based devices. The most important effect of Na doping appears to be an increase in the acceptor concentration N_A, which is usually explained by a passivation of In-related defects by Na atoms at the grain boundaries [47]. Passivation of In-related defects refers to formation of Na_{Cu} and Na_{In} rather than In_{Cu} interstitials and V_{In} vacancies, resulting in a lower concentration of compensating donors. Doping with Na was also found to significantly improve the quality of Se-poor CIGS [42], and improve the surface composition of the CIGS absorber leading to a reduction of interface recombination at the CIGS/CdS heterointerface [41].

Treatment with K was found to lead to a strong Cu and Ga depletion in a thin (~30 nm) layer at the CIGS absorber surface due to the replacement of Na ions by K ions. These changes in composition at the absorber layer surface were found to allow a thinner CdS layer without leading in an increase in surface recombination. This leads to a reduction in absorption losses in the CdS buffer layer without losses in V_{OC} [95] [96]. In addition to Na and K, very good results have been obtained with the heavy alkali elements Caesium (Cs) and Rubidium (Rb) [37]

The addition of Cd to the CIGS absorber is expected to play in important role in the type-conversion at the absorber surface. In the standard architecture of CIGS TFSC's this Cd-doping occurs automatically during the CBD of the CdS buffer layer, as mentioned in sections 2.1 and 2.3.1. Presence of Cd is expected to result in the formation of Cd_{Cu} defects thus reducing the concentration of V_{Cu} defects and hence the P-type conductivity.

2.4 DEPOSITION OF CIGS ABSORBER LAYERS

The first approach to the deposition of $CuIn(Se,S)_2$ thin-films was based on evaporation from a single $CuIn(Se,S)_2$ source under simultaneous evaporation from separate source of (Se,S) [34] [97]. During these first investigations the importance of a higher accuracy in the Cu/In ratio became clear, so that new deposition techniques were developed that allowed separate control of the Cu and In deposition rates. Two important requirements for obtaining high quality CIGS

films were identified: i) the final composition should be Cu-poor (Cu/In < 1) and ii) preferably, part of the growth occurs in Cu-rich conditions. The most favourable range of Cu-contents was found to be $0.8 < CGI < 0.9$, but good device efficiencies (>14%) have been obtained using compositions in the range $0.56 < CGI < 0.92$ as long as Na is provided to the absorber. The effect of implementing a Cu-rich growth stage was found to be an increase in grain-size (>1 μm), and improved morphological and electrical properties. Increased grain size is suggested to result from the crystal growth in presence of the 'quasi-liquid' formed by the Cu_XSe phases present in Cu-rich conditions. Presence of these Cu_XSe phases should be avoided since they show metallic behaviour. The final growth step in any process should be a Cu-poor growth step to convert any remaining Cu_XSe into $Cu(In,Ga)Se_2$ [6] [98].

Mainly two deposition techniques have consistently resulted in highest device efficiencies the past 30 years: *sequential processing* and *co-evaporation*. The material obtained using both processes can be quite similar as long as i) a substrate temperature of at least 500 °C is used, ii) the final film has overall Cu-poor composition, iii) there is an oversupply of Se during deposition, iv) the GGI of the final film is in the range of ~0.2-0.3 and v) Na-doping is applied at some stage in the deposition [6]. This is also reflected in the rather similar efficiencies, although in recent years three-stage co-evaporation (see-below) has given best results.

In the sequential processing or 'deposition-reaction' approach two separate steps are necessary to form the final CIGS film: the *deposition* step in which the metallic (Cu, In, Ga) precursors are deposited onto the substrate, and the *reaction* step in which the precursors are annealed in a Se atmosphere (typically H_2Se gas) at high temperature (>500°C) to finalize the CIGS film. The precursor deposition can be formed in various ways but sputtering from metallic targets is the most common approach. The deposition-reaction approach has the advantages that it doesn't necessarily require vacuum methods for deposition, and it is more easily used for larger area depositions. However, the H_2Se gases used for the reaction step are highly toxic and lead to the requirement of more complicated setups for safe depositions.

In co-evaporation each element (Cu, In, Ga, Se) is evaporated from a separate source directly onto the substrate. By applying high temperatures at the elemental sources (from 350°C for Se up to 1300° C for Cu) as well as at the substrate (∼350-650 °C) a CIGS film is formed instantaneously at the substrate from the vapour mixture [6] [63]. The biggest advantage of co-evaporation is that the composition of deposited material can be regulated with very high accuracy by varying the relative elemental fluxes. Different strategies have been developed for co-evaporation during the past decades. The simplest is the 'single-step' approach in which the relative fluxes are fixed during the deposition to obtain a Cu-poor composition. For implementing a Cu-rich growth phase two alternative approaches have been developed: the 'bilayer' approach [99] and the 'three-stage' approach [98]. As the name suggests, the bilayer approach consists out of deposition of two layers: an initial Cu-rich layer deposited at substrate temperature of 350-500°C, and a second Cu-poor layer deposited at temperatures of 450-600°C. Introduction of the bilayer approach was an important step that allowed the large jump in efficiencies CIGS-based devices in the 1980's (see Figure 11). The more recently established three-stage approach consists out of three separate growth steps: first In, Ga and Se are evaporated at ∼250 -300 °C, followed by Cu and Se at substrate temperatures $>$ 540°C, and finally In, Ga and Se are evaporated again, at substrate temperatures $>$ 540 °C [6] [98]. The most recent efficiency records above 20% were reached with the three-stage process. The most important drawback of co-evaporation is the relatively energy-intensive and complicated setup, making it more difficult to scale-up than sequential processing. In the standard configuration, each source covers a relatively small area of the substrate, as shown in Figure 19(A). Alternatives have been developed for larger area depositions, as shown in Figure 19(B) and Figure 19(C). Here, the sample is moved during deposition while the material fluxes are fixed, leading to lower flexibility in the composition profile.

The LTPED technique that was used for the samples studied during this thesis is described in more detail in the following chapter. The motivation for developing this LTPED technique was the promise of a single step deposition, at much lower temperatures (∼ 250°C) than co-evaporation or sequential processing.

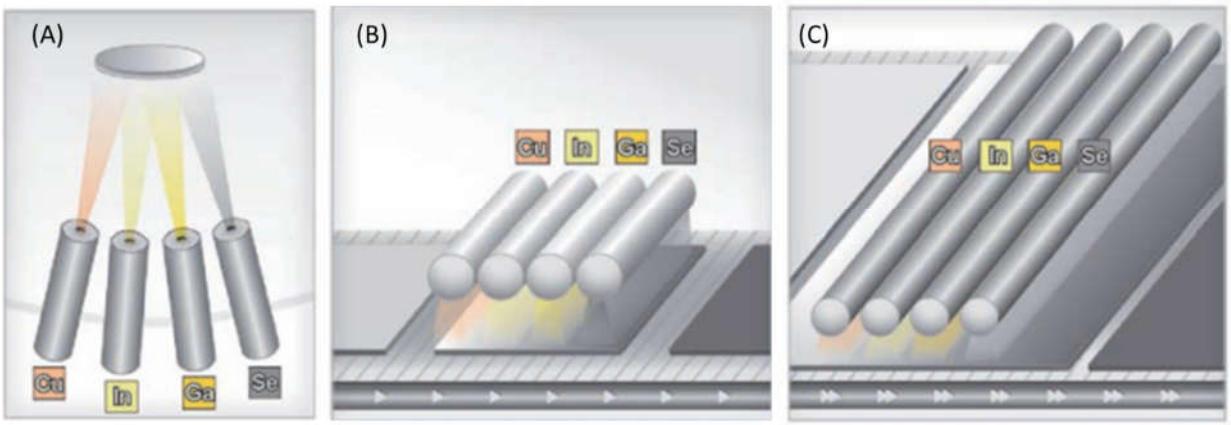


Figure 19 Different approaches to co-evaporation for laboratory scale (A) in which evaporation sources and substrate are fixed, 'sub-modular' scale (B), for which evaporation onto each module is performed separately with variation of the fluxes over time and (C) 'full-modular' scale, for which the substrate moves underneath evaporation sources depositing at fixed rates [49]

3 Electrical characterization techniques

This chapter contains the theoretical background of the most important electrical characterization techniques used during this thesis (section 3.1) and the instrumental setup and methodology that were used (section 3.2). The electrical characterization techniques that will be presented are Admittance Spectroscopy (AS), Capacitance-Voltage profiling (C-V), temperature dependent current-voltage measurements (IV-T) and temperature dependent open-circuit voltage (V_{OC}-T).

3.1 THEORETICAL BACKGROUND

The electrical behaviour of a solar cell can be modelled using different model circuits, depending on the range of operation of the device. The AS spectroscopy and C-V profiling techniques are based on application of AC-bias, in which case the solar cell acts as an RC-circuit. By analysing the dependence of the capacitance C on the bias V, frequency f and temperature T, the apparent free carrier density and defect response in a device can be determined. The relevant background regarding the AC-circuit model, limitations in the accuracy of the model, and the more detailed theory behind AS-spectroscopy and C-V profiling are treated in section 3.1.1.

For IV-T and V_{OC}-T measurements DC-biases are used, in which case the solar cell behaves as a diode with series and shunt resistance (also see section 1.2). The temperature dependence of the IV-T and V_{OC}-T characteristics give an indication of the main recombination mechanisms that limit device performance. The relevant background for these techniques is treated separately in section 3.1.2.

3.1.1 Capacitive investigation techniques (AS and C-V)

3.1.1.1 AC EQUIVALENT CIRCUIT AND JUNCTION CAPACITANCE

As discussed in section 1.2, application of a bias voltage ΔV to a solar cell will induce a charge variation ΔQ at both sides of the depletion layer and a variation Δw in the depletion layer width. For ΔQ sufficiently small, the cell can be associated to a parallel plate capacitor formed

by plates with separation distance equal to the depletion layer width (w) and area equal to the junction area (A_J) with the semiconductor as dielectric medium between the plates. For a dielectric constant ϵ of the semiconductor, the 'junction capacitance' is then defined as

$$C \equiv \frac{\Delta Q}{\Delta V} = \frac{\epsilon A_J}{w} \qquad 3.1$$

The circuit corresponding to this model is shown in Figure 20, where the shunt resistance R_{Sh} accounts for shunting paths in the solar cell.

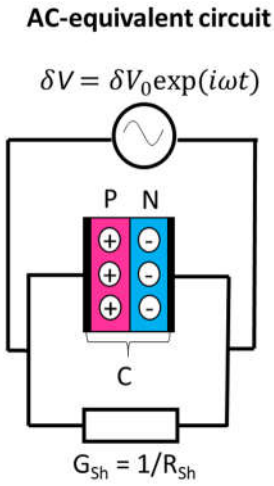


Figure 20 Schematic representation of the equivalent circuit and measurement of the principle behind the measurement of the junction capacitance for a P-N junction

The junction capacitance can be determined by considering the admittance Y of the circuit, given by Equation 3.2, under application of a small-amplitude AC-bias $\delta V(t) = \delta V \cdot \exp(i\omega t)$ (where the angular frequency $\omega = 2\pi f$ needs to be low enough to allow free charge carriers to respond to the signal).

$$Y = \frac{1}{R_{Sh}} + i\omega C \qquad 3.2$$

From the imaginary part of Equation 3.2 the capacitance can be derived, which can in turn be used to calculate the depletion layer width w using Equation 3.1. In CIGS-based devices nearly the entire depletion region is expected to lie on the P-side of the P-N junction, as discussed in Chapter 2. From Equation 1.6 shown in Chapter 0, with $N_D = 0$ the ionized acceptor density N_A

on the P-side can then be extracted from the depletion layer width (see section 3.1.1.3). The accuracy of the extracted values for C, w and $\mathrm{N_A}$ can be strongly limited due to the contribution of electrically active defects, which are usually present in high concentrations in CIGS-based devices as discussed in Chapter 2.

In Figure 21(A) the band-diagram on the P-side of a P-N junction is show in the region between the P-N interface at $\mathrm{x} = 0$ and the depletion layer edge at $\mathrm{x} = \mathrm{w}$. Presence of a defect state acting as a majority carrier trap leads to formation of an additional energy level at energy $\mathrm{E_d}$ above the VBE, on the P-side of a P-N junction.

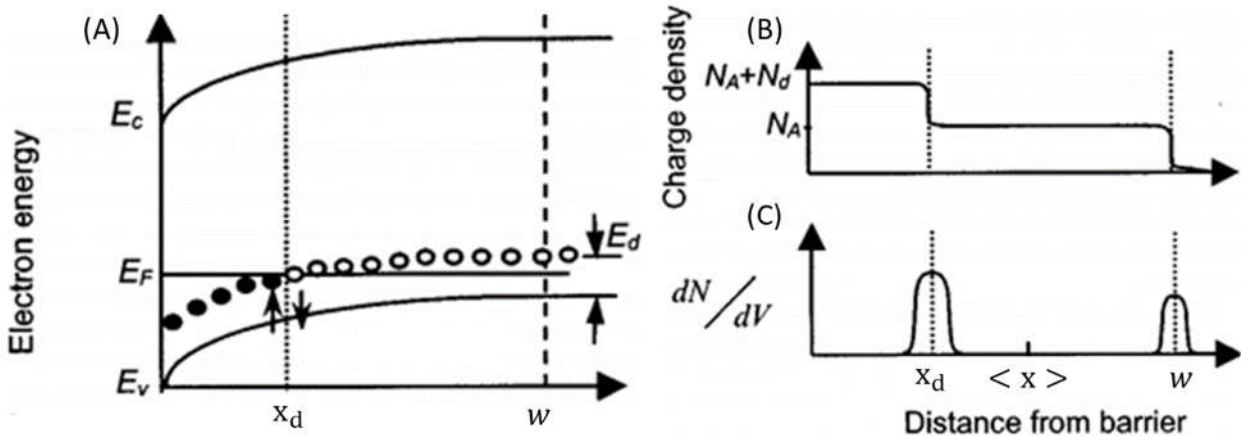


Figure 21 The influence of a defect inducing a single majority carrier trap in the bandgap of the P-type semiconductor forming a P-N junction, adapted from [100] (A): Band-diagram of the depletion region ($0 \leq \mathrm{x} \leq \mathrm{w}$) on the P-side of the junction, with $\mathrm{E_d}$ the energy corresponding to the trap level. For $\mathrm{E_d} < \mathrm{E_F}$ negatively charged traps contribute to the total charge density, while for $\mathrm{E_d} > \mathrm{E_F}$ the traps have neutralized by hole capture. At application of an AC-bias the point $\mathrm{x_d}$ where $\mathrm{E_d} = \mathrm{E_F}$ oscillates, giving rise to hole capture/emission close to $\mathrm{x_d}$ (B): The total charge density in the depletion layer as function of distance x from the interface. Traps in the region $\mathrm{E_d} < \mathrm{E_F}$ contribute a charge density $\mathrm{N_d}$ to the total charge density, while for $\mathrm{E_d} > \mathrm{E_F}$ only the ionized acceptor density $\mathrm{N_A}$ remains (C): Variation in charge density under application of an AC-bias. The charge variation $\mathrm{x_d}$ due to hole capture/emission of the traps results in a higher measured capacitance and lower apparent depletion layer width ($< \mathrm{x} >$)

Due to the band-bending in the region $0 \leq \mathrm{x} \leq \mathrm{w}$, $\mathrm{E_d}$ lies below $\mathrm{E_F}$ for $\mathrm{x} < \mathrm{x_d}$ and above $\mathrm{E_F}$ for $\mathrm{x} > \mathrm{x_d}$, with the intersection point $\mathrm{E_d} = \mathrm{E_F}$ at $\mathrm{x} = \mathrm{x_d}$. For high enough temperatures, all traps for which $\mathrm{E_d} > \mathrm{E_F}$ will be able to capture holes and neutralize, while those for which $\mathrm{E_d} < \mathrm{E_F}$ will remain ionized (in this case, negatively charge). As a result, in the region $\mathrm{x} < \mathrm{x_d}$ a charge density $\mathrm{N_d}$ in addition to the ionized acceptor density $\mathrm{N_A}$ exists so that the total charge density

becomes $N = N_d + N_A$, as illustrated in Figure 21(B). From Equations 1.6 and 3.1, the contribution N_d causes a smaller w and higher C than in absence of the ionized traps. This can be considered a 'static' contribution of majority carrier traps and is also present without external bias.

At application of an AC-bias the variations induced in the band-bending result in oscillation of the point $x = x_d$ around its equilibrium position. This causes traps close to $x = x_d$ to continuously be swept above and below the Fermi-level. If the capture/emission rate τ^{-1} of the traps is high enough to follow the frequency of the AC-signal (see the following section 3.1.1.2) the traps will periodically ionize and de-ionize during measurement. This gives rise to a charge variation $\delta Q'$ centred at $x = x_d$ in addition to the charge variation δQ at $x = w$. From Equation 3.1 a higher total charge variation leads to a higher C and a smaller 'apparent' depletion layer width ($< x >$ in Figure 21(C)) than the actual (w). This 'dynamic' contribution from majority carrier traps will disappear at high frequencies of the AC-bias for which τ^{-1} is too low to allow capture/emission by majority carrier traps. Since τ^{-1} reduces exponentially with temperature (see Equation 3.3) the contribution of defects to the measured capacitance can be significantly reduced by cooling the sample and increasing the frequency of the AC-bias. This allows obtaining accurate values of C, w and N_A by appropriate choice of frequency and temperature used for C-V measurements. The AS-spectroscopy technique treated in the section below gives a good indication of the appropriate ranges.

3.1.1.2 Admittance Spectroscopy (AS)

In AS-spectroscopy the frequency and temperature dependence of the junction capacitance are analysed to obtain more information about the energy distribution of majority carrier trap-levels in the depletion region. This approach takes advantage of the temperature and frequency dependence of the trap emission rate τ_E^{-1}, which for a single trap level at energy E_d on the P-side of a P-N junction is given by [100] [101]

$$\tau_E^{-1} = aT^2 \exp\left(-\frac{E_d}{kT}\right) \qquad 3.3$$

In this expression a can be considered a constant if the capture cross section is assumed to be temperature independent. If the capacitance is measured as function of the frequency f of the AC-bias, the present trap level can be expected to respond in the range for which $2\pi f = \omega \leq \tau_E^{-1}$. By choosing the amplitude of the AC-bias small enough, only traps close to $x = x_d$ with emission rate τ_E^{-1} equal to the capture rate τ_C^{-1} will emit and capture majority carriers. For a homogeneous distribution of traps in the depletion region the shape of the C-f profile will then be given by:

$$C(f) = C_\infty + \frac{C_0 - C_\infty}{1 + (f/f^*)} \qquad 3.4$$

In this expression C_0 and C_∞ are the asymptotic capacitance in the low and high frequency limits respectively (i.e. $C_0 = \lim_{f\to 0} C(f)$ and $C_\infty = \lim_{f\to\infty} C(f)$) and f^* is the frequency at which the trap level stops responding, satisfying $2\pi f^* = \omega^* = \tau_E^{-1}$ [102]. The disappearance of the defect response is visible in the curve given by Equation 3.4 as a clear step in the capacitance with an inflection point at f^*. In Figure 22 this is shown for the case of two distinct trap levels. From Equation 3.3, ω^* will be temperature dependent with a variation depending on E_d, where trap levels closer to the centre of the bandgap ('deeper' levels) will have a stronger temperature dependence. The inflection point in the C-f curves is observable as a peak in the derivative of the capacitance, which is usually analysed in the scaled form $\left[-\omega\left(\frac{dC}{d\omega}\right)\right]$. From equation 3.3, it follows that E_d can be expressed in terms of $\omega^*(T)$ as

$$-\frac{E_d}{kT} = \ln\left(\frac{\omega^*(T)}{T^2}\right) \qquad 3.5$$

From an Arrhenius plot of the right hand side of equation 3.5, the slope of the linear region of the plot will give an estimate of E_d.

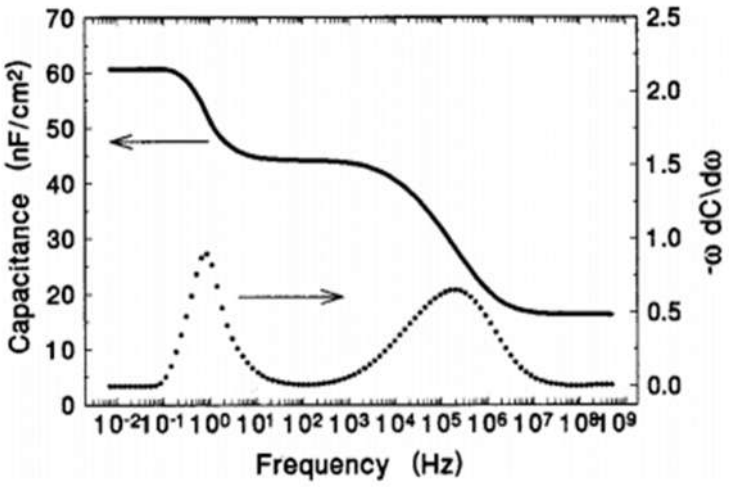


Figure 22 Picture of C-f profile (full black-line, left axis) showing two steps in capacitance with corresponding -$\left[-\omega \frac{dC}{d\omega}\right]$ curve (dotted line, right axis) as reported in [100].

The above description is valid for a single isolated trap level. However, in general there will be a distribution of closely spaced defect levels inside the bandgap of the depletion region, typically presumed Gaussian or exponential [103] [104]. In this case the defect response will disappear more gradually as the *C*-f profile becomes a convolution of curves as the one given by Equation 3.4. For distribution of trap levels, the energy level extracted from the Arrhenius plot will correspond to the energy at which the trap concentration in the distribution is highest.

The defect response observable in AS-spectroscopy is limited to that from majority carrier traps, as the minority carrier concentration is too small to allow significant capture/emission by minority carrier traps. A second limitation is the limited frequency and temperature ranges for which accurate capacitance measurements are possible, as discussed in section 3.1.1.1. On CIGS-based devices, typically accurate capacitance measurements can be performed using frequency and temperature ranges of 1 kHz $\leq f \leq$ 1 MHz and 100 K $\leq$ T $\leq$ 400 K. This allows detection of trap levels at up to ~0.5-0.6 eV from the VBE. Due to the limited frequency range accessible and the reduction in accuracy of the measured capacitance at high and low frequency, estimates of C_0 and C_∞ extracted from actual C-f profiles will always suffer significant inaccuracy. Nevertheless, the ratio of C_0/C_∞ can give a rough indication of the relative contribution from defects to the capacitance (see Chapter 4). Also, C_∞ can give an indication of the accuracy of the

high frequency capacitance in the case the absorber layer is fully depleted (see section 3.1.1.3 below). In a completely depleted layer, the capacitance without response from trap levels should correspond to the 'geometric capacitance' $C_{\mathrm{Geo}} = \frac{\epsilon A_{\mathrm{J}}}{\mathrm{d}}$, with d the thickness of the depleted layer. Hence, at high frequencies $C_{\infty} \geq C_{\mathrm{Geo}}$ should always be satisfied. For a CIGS absorber with of ~1.8 µm thick and an absolute dielectric constant ϵ_{CIGS} = $1.2 \cdot 10^{-12}$ F/cm^2, the geometric capacitance would be approximately 6.7 nF/cm^2.

3.1.1.2.1 Typical AS-spectra for CIGS-based devices

In the already published work regarding AS-spectroscopy on CIGS-based solar cells quite similar shapes are usually reported for C-f profiles. A sharp step in capacitance at low temperatures is typically observed and commonly referred to as 'N1', while at higher temperatures a more gradual reduction in capacitance is often reported commonly referred to as 'N2'. The corresponding activation energy of the two signatures are usually found to be~100 meV for N1 and 250-300 meV for N2 (see Figure 23) [101]. For N1 a slight variation in the activation energy was found after light-soaking and forward bias application, while for N2 usually no variation was observed after device treatment [101] [74].

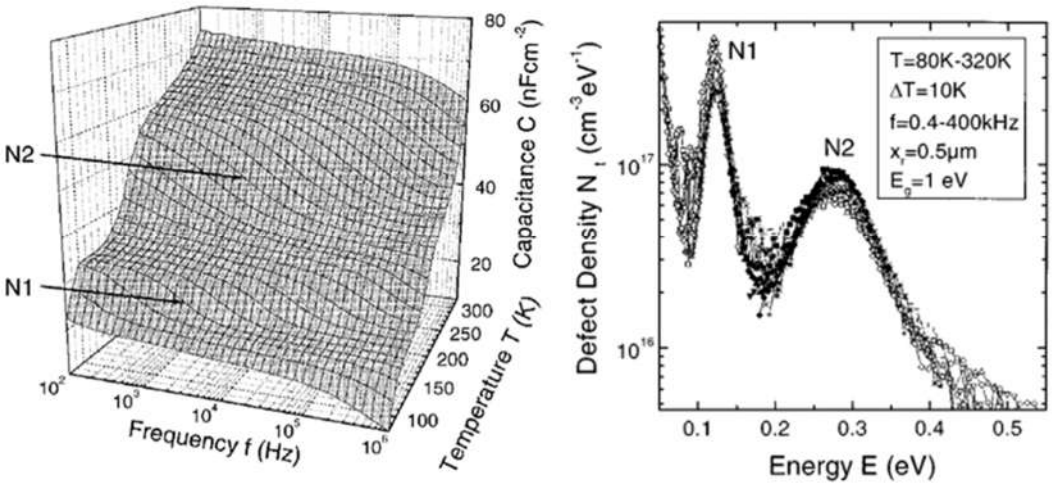


Figure 23 Left: Three-dimensional representation of typically observed AS-spectra on $CuInSe_2$-based devices. Right: energy distribution of N1 and N2 levels derived from observed defect response with AS-spectroscopy (both figures from [105]). The N1 defect level is observed at lower temperatures indicating a shallower defect energy (typically ~40-160 meV), while N2 is observed at higher temperatures, indicating a deeper defect energy (~250-400 meV).

The origin of both steps is still a matter of discussion. Some authors report both steps show characteristics of a barrier at the buffer/absorber interface or at the absorber/back-contact interface [101] [74] while other authors suggest the steps to be related to intrinsic defects [106]. The intrinsic defects to which the N1 step is typically attributed are $(In,Ga)_{Cu}$ defects inside an N-type inverted layer at the absorber surface [87]. The N2 response has been attributed to V_{Se} defects, $Cu_{(In,Ga)}$ antisite defects and more generally to effects of Cu-migration.

In $CuGaSe_2$ (CGS)-based devices the AS-spectra were found to depend on the Cu-content. At high Cu-content, two acceptor levels were found at ~240 meV and 350 meV from the VBE. At high Ga-content a tail-like distribution of levels with maximum energy at ~250 meV from the VBE was observed [103].

3.1.1.3 Capacitance voltage profiling (C-V)

In C-V profiling the doping density inside the depletion layer is analysed at different depletion layer widths. In this measurement approach the capacitance is measured by application of an AC-bias as described in the previous sections with different DC-bias superimposed to change the depletion layer width. In absence of deep level response the doping density $\mathrm{N_A}$ follows from the variation in capacitance C with DC-bias according to

$$\mathrm{w} = \frac{\epsilon \mathrm{A_J}}{C} = \sqrt{\frac{\frac{2\epsilon}{\mathrm{q}}(\mathrm{V_{bi}} - V)}{\mathrm{N_A}}} \qquad 3.6$$

Here, $\mathrm{V_{bi}}$ is the built-in potential and q is the elemental charge. In the Mott-Schottky approach this is usually rewritten as

$$\frac{1}{C^2} = \left(\frac{2}{\mathrm{q}\epsilon \mathrm{N_A}}(\mathrm{V_{bi}} - V)\right) \qquad 3.7$$

so that

$$N_A = -\frac{2}{q\epsilon} \cdot \left[\frac{d}{dV}\left(\frac{1}{C^2}\right)\right]^{-1} \qquad 3.8$$

Hence, the slope of $\frac{1}{C^2}$ against V will give an indication of the doping density N_A. A straight line indicates a constant doping density with depletion layer width, as shown in Figure 24. The intercept $\frac{1}{C^2}$ with the horizontal axis can give a rough indication of the V_{bi}, but will also depend on the voltage drop across the buffer-layer and present interface charges [6].

Typically, the DC-bias is swept in the range of +0.5 V $\leq V \leq$ -1 V in steps of ~10-50 mV, i.e. from forward to reverse bias according to increasing depletion layer width. The suitable frequency and temperature range for C-V measurements can then be determined from the AS-spectra as mentioned above. In most cases at f ~1 MHz and T~120 K defect response is absent. To prevent the contribution of constant charge in a possible region where $E_d < E_F$ illustrated in Figure 21, a moderate forward bias can be applied to sweep present traps above the Fermi-level and allow them to neutralize. Even taking the above-mentioned precautions, various authors suggest the typical N-w profiles obtained on CIGS-based devices remain influenced by deep defect levels able to capture charge carriers during the slow DC-bias sweet at low temperatures, as explained below.

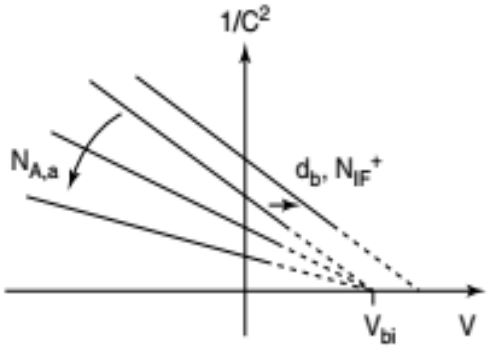


Figure 24 Typical results of a 'Mott-Schottky' plot. The slope of ($1/C^2$) vs V gives an indication of the doping density of the absorber layer. For a buffer layer with interface charge N_{IF}, the profile is shifted towards higher bias [6].

In most cases the N-w profiles of CIGS-based devices show a 'U'-shape, with an apparent increase toward both CIGS/CdS interface and the absorber bulk (see Figure 25). The profile minimum is considered to give the most accurate estimate of the net free carrier density in the sample, while the origins of the increase toward the interface and bulk aren't entirely agreed upon. Both have been explained as an actual increase of the charge carrier density. However, the accuracy of the increase toward the heterointerface is questioned as it is only observed at high temperature and relatively high forward bias conditions ($V \geq 0.4$ V) for which the forward current density can expected to be too high to allow accurate measurement of the capacitance. The increase toward the back-contact might also be related to the capture/emission of electrons/holes by deep defects during the longer DC-bias sweep, causing an increase in negative charge in the depletion layer [101].

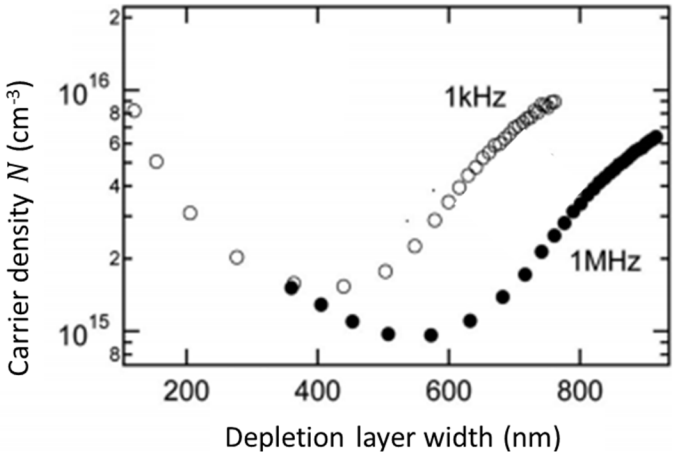


Figure 25 Typical 'U'-shaped profiles, as measured for CIGS-based devices reported in [101]

3.1.2 Temperature dependent current-voltage techniques (IV-T and V_{OC}-T)

3.1.2.1 Single diode model and recombination paths

At application of DC-bias and illumination, the behaviour of a solar cell can be modelled according to the model shown in section 1.2.2 of Chapter 0 (see Figure 7). In Chapter 0 the diode current J_D was expressed as the product of a single saturation current density J_0 and a single exponential term containing the ideality factor A. In reality the more complete expression would contain a sum of saturation currents J_0^i and exponential terms with different ideality factors A^i for each of the possible contributions to recombination, as shown in Equation 3.10 [6]

From analysis of the circuit and by using the standard diode equation, the current through the solar cell can be expressed as

$$\mathrm{J} = \mathrm{J_D}(V) + \frac{(V - \mathrm{JR_S})}{\mathrm{R_{Sh}}} + \mathrm{J_{Ph}}(V) \qquad 3.9$$

$$\mathrm{J_D}(V) = \sum_{\mathrm{i}=1}^{\mathrm{N}} \mathrm{J_0^i} \exp\left(\frac{\mathrm{q}V}{A^i \mathrm{kT}}\right) \qquad 3.10$$

Each of the $\mathrm{J_0^i}$ terms can in turn be expressed in terms of an activation energy $\mathrm{E_a^i}$ of the recombination mechanism and a corresponding reference current density $\mathrm{J_{00}^i}$ usually assumed to be temperature independent:

$$\mathrm{J_0^i} = \mathrm{J_{00}^i} \exp\left(\frac{\mathrm{E_a^i}}{A^i \mathrm{kT}}\right) \qquad 3.11$$

Although in TFSC's the number of different possible recombination mechanisms is quite large, one is usually expected to dominate. The principle of both IV-T and V_{OC}-T measurements is to take advantage of the temperature dependence of the diode current $\mathrm{J_D}$ to isolate the recombination dependent parameters, $\mathrm{J_0}$, A and $\mathrm{E_a}$. From the temperature dependence and values of these parameters the corresponding recombination mechanism can be derived.

A useful model for the description of recombination in CIGS-based devices was developed by Rau, Jasenek et al. [104] where two different regions and two different mechanisms for recombination are distinguished, as shown in Figure 26. In this model, recombination is assumed to take place either in the bulk of the absorber, or at the CIGS/CdS interface. In both regions, the possibility of different degrees of tunnelling enhanced recombination are considered.

In the bulk of the absorber tunnelling enhanced recombination can occur as electrons tunnel from the conduction band (CB) of the CdS layer to the CB of the CIGS absorber, where they recombine with the majority carrier holes. At the interface between CdS and CIGS holes can tunnel from the valence band (VB) of the CIGS absorber to the VB of the CdS buffer layer, where they recombine with the majority carrier electrons.

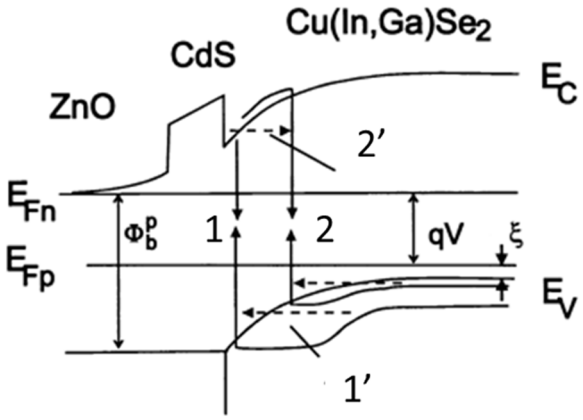


Figure 26 Illustration of expected dominant recombination paths in typical CIGS-based TFSC's according to [104]. 1) Recombination at CdS/CIGS interface, 1') Tunnelling enhanced interface recombination: holes tunnel from the CIGS VB to the CdS VB. (TE-IR) 2) Bulk recombination in the CIGS absorber 2') Tunnelling enhanced bulk recombination: electrons tunnel from the CdS CB into the CIGS CB

Each recombination mechanism corresponds to a different expression for the current density. Using these expressions, the distinction between interface and bulk recombination can be made directly from the value of the activation energy $\mathrm{E_a}$ occurring in the exponential term. In the case of bulk recombination, it was found that $\mathrm{E_a} \sim \mathrm{E_G}$, i.e. the activaiton energy equals the bandgap of the absorber layer. In the case of interface recombination, $\mathrm{E_a} \sim \Phi_{\mathrm{B}}^{\mathrm{P}}$, i.e. the hole-barrier at the interface [107]. The distinction between tunnelling enhanced bulk or interface recombination could be made from analysis of the temperature dependence of the ideality factors in the expression for the current density. In the case of interface recombination, tunnelling was associated with a temperature dependence according to

$$\frac{1}{A} = 1 - \frac{(\mathrm{E_{00}})^2}{3(\mathrm{kT})^2} \qquad 3.12$$

Where $\mathrm{E_{00}}$ is referred to as the characteristic tunnelling energy which expresses the energy barrier for a specific tunnelling mechanism [108].

Classical recombination (by thermionic emission) corresponds to a temperature dependence given by:

$$A = \frac{\mathrm{E_{00}}}{\mathrm{kT}} \coth\left(\frac{\mathrm{E_{00}}}{\mathrm{kT}}\right) \qquad 3.13$$

The description of recombination in the bulk of the absorber ('bulk recombination') are slightly more complicated due to the influence of the defect distribution in the bandgap (see section 3.1.1). In [104] and [4] the assumption of an exponential trap distribution with a maximum at the edge of the VB was made, resulting in a temperature dependence of the ideality factor for bulk SRH recombination (i.e., without tunnelling contribution) of

$$A = \frac{1}{2}\left(1 + \frac{\mathrm{T}}{\mathrm{T^*}}\right) \qquad 3.14$$

In this expression $\mathrm{T^*}$ refers to the temperature corresponding to the characteristic energy $\mathrm{kT^*}$ of the defect distribution [109]. This relationship has been found to be valid in well behaving CIGS-based devices for temperatures in the range 200 K $< \mathrm{T} <$ 350 K, with lower temperatures leading to a higher contribution from tunnelling. For the higher bandgap compounds $CuGaSe_2$, tunnelling has also been confirmed to play a more significant role [109]. In the case of pure tunnelling, the ideality factor was found to satisfy

$$\frac{1}{A} = \frac{1}{2}\left(1 + \frac{\mathrm{T}}{\mathrm{T^*}} - \frac{\mathrm{E_{00}^2}}{3(\mathrm{kT})^2}\right) \qquad 3.15$$

3.1.2.2 Temperature dependent Current-Voltage spectroscopy (IV-T)

By analysing of IV measurements performed as function of temperature, the above described theory can be applied to deduce the dominant recombination mechanism limiting the performance in a solar cell. The ideality factor A and saturation current density $\mathrm{J_0}$ can be fitted at each temperature, and used with the known expression for the dark current in a device to obtain the activation energy $\mathrm{E_a}$ of the dominant recombination mechanism:

$$A \cdot \ln\left(\frac{J_0}{J_{00}}\right) = -\frac{E_a}{kT} \qquad 3.16$$

Often the temperature dependence of $A \cdot \ln(J_{00})$ is disregarded, so that $A \cdot \ln(J_0) \approx -\frac{E_a}{kT}$. Although this approach was found to give some deviation from the actual value of E_a obtained when determining J_{00}, especially for lower efficiency cells, it is useful to obtain at least a rough indication of E_a while being much less cumbersome [107].

Hence, an approximate value of E_a is obtained from the slope of the linear region of an Arrhenius plot of $A \cdot \ln(J_0)$. As mentioned above, for values of $E_a \sim E_G$ recombination is considered to take place mainly in the bulk of the absorber layer, while for very different values (usually $E_a < E_G$) interface recombination can be considered to play an important role.

3.1.2.3 Temperature dependent open-circuit voltage (V_{OC}-T)

Under open-circuit conditions (i.e. V = V_{OC} and $J = 0$) and assuming $R_{Sh} \gg R_S$ the diode current can be rewritten to give an expression of the temperature dependence of the V_{OC} [29]

$$V_{OC} = \frac{E_a}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_L}\right) \qquad 3.17$$

Here J_L refers to the illumination current, as defined in Chapter 1. It follows that mainly at high temperatures for which $A \cdot \ln(J_{00})$ has little temperature dependence, the temperature dependence of the V_{OC} is linear with temperature and gives an intercept with the vertical axis corresponding to E_a. For CIGS-based devices the linear region for V_{OC}-T characteristics is usually observed for temperatures of up to ~200 K. For lower temperatures tunnelling becomes increasingly important and carrier freeze out occurs, leading to saturation of the V_{OC}.

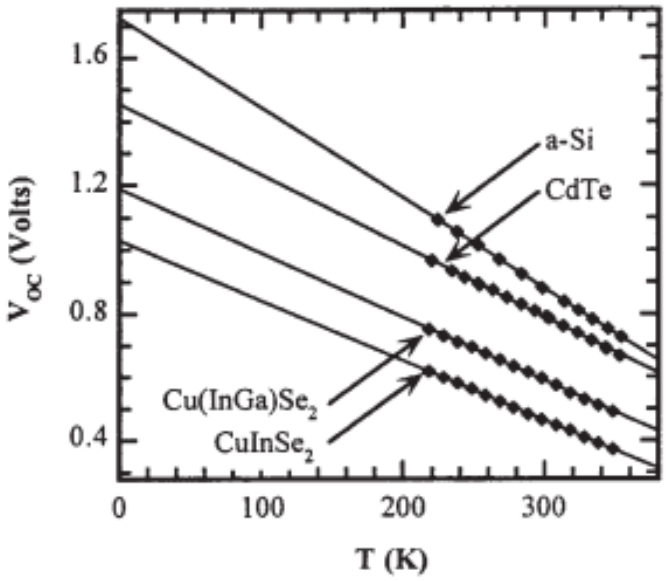


Figure 27 Example of V_{OC}-T curves measured for thin film solar cells with absorber layer of a number of different absorber materials. The Intercept with the vertical axis indicates $E_a \sim E_G$ for each case, indicating the V_{OC} is limited by bulk recombination [29].

3.1.2.3.1 LIMITATIONS TO ON-DIODE MODEL

The accuracy of the results obtained from V_{OC}-T and IV-T techniques will depend on the extent to which the investigated devices can be correctly described by the one-diode model. Especially for TFSC's parasitic losses are usually present in the diode current that aren't well described by the presented circuit with a single diode, R_S and R_{Sh}, but would require a more complicated model in which different contributions to current and current losses are taken into account explicitly [28] [110]. In IV-T measurements, correction of the IV-curves for the contribution from R_S and R_{Sh} can give an indication of how well the solar cell is described by the ideal diode model and allow easier determination of the recombination parameters A, J_0 and E_a [29]. However, since for lower quality solar cells the contributions from series resistance and shunt losses are higher, obtained values for the recombination parameters will also be less accurate [107].

3.2 EXPERIMENTAL SETUP AND METHODOLOGY

In the current section a description is given of how the AS, C-V, IV-T and V_{OC}-T measurements were performed on LTPED-devices at IMEM-CNR during this thesis. The approach was optimized

to achieve high reproducibility of obtained results by minimizing contributions from defect response and metastability described in section 2.2.2. Measurement parameters such as the oscillation frequency of the AC-bias in AS and C-V measurements, ranges of DC-bias and temperature, the approach to illumination for V_{OC}-T measurements, the order in which the measurements should be performed, and the definition of appropriate initial conditions of the device were varied to this end. Special care was taken in the choice of the investigated cells to limit effects from R_S and R_{Sh} on the accuracy of measured IV-characteristics and capacitance described in sections 3.1.1 and 3.1.2.3.1. Cells with low reverse current density and small area ($\leq$ 0.1 cm^2) were used to obtain reliable capacitance values and limit shunting effects.

3.2.1 Temperature regulation

For each of the four measurement techniques the same cryostat setup shown in Figure 28 and Figure 29 was used.

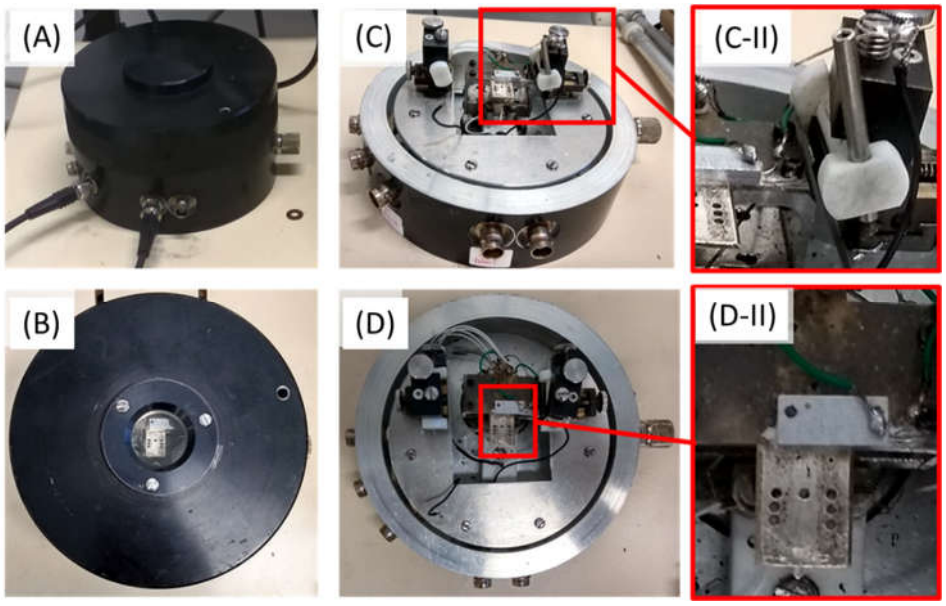


Figure 28 Cryostat chamber used for performing temperature dependent characterisations (AS, C-V, IV-T and V_{OC}-T). (A) Side-view, with top cover and window cap applied to keep sample in darkness. (B) Top-view, with window cap removed for allowing illumination of the sample. (C) Side-view without top-cover, with indication of pin (C-II) used for contacting the cell concerned. (D) Top-view without top-cover with indication of the cold-finger (D-II) onto which the 1-inch by 1-inch sample is mounted during measurements.

The setup consisted of the cryostat chamber (Figure 28), a DLTS temperature controller, a BIO-RAD control unit to regulate pressure and liquid nitrogen flow inside the cryostat chamber.

The sample was mounted inside the cryostat chamber such that the substrate was in direct contact with the cold finger that was used to control the temperature (Figure 28 D-II). For contacting the metallic pins in the cryostat were either placed in direct contact with the front/back contact with a dot of silver paste to reduce resistance, or Cu-wires were glued to the front/back contact with silver paste.

The chamber pressure was maintained in the range of $\sim 10^{-1}$-10^{-2} mbar using a membrane pump controlled by the BIO-RAD control-unit (Figure 29). The cold-finger was attached to a resistive thermocouple in contact with the DLTS temperature control unit. The desired temperature and heating rate could be set with an accuracy of 0.1 K and up to 0.01 K/s respectively. For the measurements performed during this thesis a heating rate of 0.9 K/s was used. Cooling below room temperature was achieved using a liquid nitrogen flow controlled by the BIO-RAD control unit via a rotary pump.

Figure 29 BIO-RAD control unit used to monitor the pressure inside the cryo-chamber and regulate the rotation speed of the rotary pump, which was used to control the liquid nitrogen flow into the cryostat. During temperature dependent measurements, , settings 'Auto' and 'Fast' were used for the cryo-pump.

As discussed in the previous sections, well-defined initial conditions were established before each measurement series. These were based on the typical preparations performed by various other groups for similar investigations [6] [4]. Before the start of a measurement series, the sample was left in complete darkness inside the cryo-chamber at a temperature of 320 K for ∼1.5-2 hours ('relaxation'). Care was taken to observe a stable capacitance value as function of time before starting a measurement series (stable meaning without significant variations in capacitance within ∼30 minutes).

The sequence of the different measurement techniques was chosen with the intention to minimize the influence between measurements due to metastable effects. Also, between nearly each separate measurement in the sequence additional relaxation steps were performed. From these consideration, all measurement series were performed in the order i) AS-spectroscopy, ii) C-V profiling, iii) second relaxation step, iv) IV-T measurements, v) third relaxation step vi) V_{OC}-T measurements. The AS-spectroscopy was expected to induce little to no metastable effects, considering the dark conditions and low amplitude of the AC-bias used (∼25 mV). It was found that C-V measurements could be performed directly afterwards without influence from the performance of the AS-measurements. In contrast, the higher bias range used for C-V and IV measurements and the illumination used for V_{OC}-T measurements usually induced persistent photoconductivity and influenced device performance, so that intermediate relaxation steps were considered to be required. The sequence of measurements was performed cooling down from 320 K after relaxation while performing AS-measurements, performing the C-V profiling at low temperature directly afterwards, and performing IV-T and V_{OC}-T measurements heating up after relaxation. The choice of performing IV-T and V_{OC}-T measurements heating up was made in consideration of the lower expected metastable effects at low temperature. However, in performance of V_{OC}-T measurements the difference between heating up and cooling down was found to be limited.

3.2.2 AS and C-V setups and approach

The capacitance measurements for both techniques were performed using an HP 4192A LF impedance analyser assuming the circuit to be modelled by a parallel plate capacitor with parallel shunt resistance as described in section 3.1.1.

For AS-spectroscopy an AC-signal with amplitude δV of 25 mV was usually used. Variation of this oscillation voltage showed relatively small differences between results obtained in the range of $\sim$ 15-35 mV. However, for $\delta V < 15$ mV a large loss in accuracy was observed in the measured capacitance while for $\delta V > 35$ mV the measured capacitance started to deviate, most likely due to violation of the requirement that $\tau_C^{-1} = \tau_e^{-1}$ for the excited traps as discussed in section 3.1.1.2. The frequency range of 1 kHz $\leq f \leq$ 1 MHz often reported in literature was usually found to be appropriate in most cases. For $f <$ 1 kHz the accuracy of the measured capacitance became extremely low due to the small number of cycles per unit time in combination with a reduction phase-angle θ between the real and imaginary part of the admittance Y. For $f >$ 1 MHz the capacitance was found to demonstrate artefacts similar to those reported in by Scofield et al. [111], where they were attributed to the influence of series resistance and inductance. The largest temperature range used for these measurements was 85 K $\leq T \leq$ 320 K, where the maximum was chosen to prevent damage by excessive heating. Reducing the temperature to below 120 K on the other hand showed little or no change in the C-f profile, which was ascribed to the freeze-out of free carriers that has been shown to be induced at such low temperatures. The step size in temperature was chosen in consideration of the amount of variation in the C-f profiles with the aim to achieve a sufficient resolution for constructing an Arrhenius plot from the obtained results. In each case steps of 10-20 K were found sufficient, and often lower step sizes could be used.

For C-V profiling most often a 1 MHz oscillation frequency was used at 120 K. However in a few cases artefacts were observed in the measured capacitance under these conditions, so that higher frequency/temperature were considered more suitable. The DC-bias voltage was always chosen within the range of -0.7 V $\leq V \leq$ 0.7 V, and most often the range -0.4 $\leq V \leq$ 0.3 V was found to give the most accurate results.

3.2.3 IV-T and V_{OC}-T setups and approach

For both IV-T and V_{OC}-T measurements a Keithley 236 unit was used. The 'Sense-high' output of the Keithley was contacted with the BNC-connector from the cryo-chamber, while the front-contact of the sample was kept at ground.

For IV-T measurements the bias was usually swept in the range of -0.5$\leq V \leq$ 1 V. In some cases the forward current at low temperature became so low that biases of up to 2.5 V could be applied (see Chapter 4). A step-size of 10-20 K was usually used for these measurements to obtain sufficient resolution to construct the Arrhenius plots.

For V_{OC}-T measurements a Tungsten-wire lamp fixed above the window of the cryostat was used for illumination. Before applying the relaxation treatment, the distance and orientation of the lamp were adjusted such that the measured I_{SC} under illumination at room temperature was as close as possible to the value obtained under standard condition illuminated IV measurements.

As for the other measurement techniques, some variations were applied in the approach to performing V_{OC}-T measurements over the course of this thesis. Results from V_{OC}-T measurements usually were found most suitable in the 200-320 K range as discussed in section 3.1.2.3. In some cases it was necessary to perform measurements with temperature steps in the 5-10 K range for sufficient resolution to obtain a good fit. An increased resolution in temperature was also useful as determining the V_{OC} in many cases was not straightforward. Different strategies have been attempted for illuminating the sample, firstly illuminating continuously during measurement or by applying and removing the illumination. In both cases the lamp was kept turned on to prevent variation of the intensity at switching on/off. Continuous application of illumination was attempted in some cases but was found to reduce the accuracy of the temperature regulation due to sample heating.

4 Standard CIGS by LTPED

INTRODUCTION

The aim of this chapter is to give an overview of the standard architecture, preparation approach and electrical characteristics of the CIGS-based devices investigated during this thesis. All devices for which results are reported here were prepared at IMEM-CNR using the novel low-temperature pulsed electron beam deposition (LTPED) technique, and will be referred to as 'LTPED-devices' in the following. First the LTPED technique for CIGS deposition is described in more detail in section 4.1, after which the specific architecture and preparation approach are treated in section 4.2. In section 4.3 some of the results obtained during this thesis are presented to give an impression of the typical electrical characteristics of LTPED devices.

4.1 LOW TEMPERATURE PULSED ELECTRON DEPOSITION

In the LTPED technique used at IMEM-CNR pulsed electron-beam deposition (PED) was applied to deposit good quality CIGS thin films. In comparison to conventional deposition techniques presented in Chapter 3, LTPED offers the advantages of a much lower substrate temperature during deposition (~250 °C as opposed to temperatures >450 °C) and only a single deposition step for the CIGS absorber. The PED technique had already been used for other materials at IMEM-CNR (mainly superconductors) before it started to be applied for low temperature depositions of CIGS in 2009. Within two years it was confirmed that good quality CIGS thin films suitable for application as absorber layers in solar cells could be obtained using LTPED [19]. Further optimization of the LTPED technique and the architecture used for LTPED-devices has since resulted in record efficiencies of 17% [1]

4.1.1 Experimental setup: Pulsed Electron Deposition

As in pulsed laser deposition (PLD), in PED a high-energy beam is used to achieve stoichiometric material transfer from a single target. However, the application of an electron beam rather than a laser beam has a number of advantages: lower cost, higher efficiency, smaller deviations in

stoichiometry of deposited material and simpler handling [112]. The scheme of the LTPED setup used at IMEM-CNR shown in Figure 30 also gives a good overview of the general principle behind PED: electrons are emitted from the electron gun at high energies and guided toward the target by a dielectric tube. The acceleration voltage and pulse rate of the electron beam can be varied according to the requirements for deposition.

Incidence of the high energy electrons onto the target surface results in formation of a plasma plume consisting of two components: a plasma plume of 'ablated' material (ablation plume) and a plasma plume of 'evaporated' material (evaporation plume), each having a different angular distribution (see Figure 30). Ablation is the mechanism that results in stoichiometric material transfer and hence the mechanism aimed for with PED. It's a result of higher energy electrons (kinetic energies $\geq$ 10 keV) which give rise to vaporization of the target material outside of thermodynamic equilibrium as their energy is dissipated within a small volume. Evaporation from the target occurs at thermodynamic equilibrium and gives rise to non-stoichiometric material transfer making it an undesirable component in PED. It results from lower energetic electrons (kinetic energies $\leq$ 1 keV) which gradually heat the target surface during deposition, thus forming a melt from which incongruent evaporation occurs. The evaporation plume is off-stoichiometric since the more volatile elements will be present at higher concentrations. In the case of CIGS this causes high concentrations of Se and much lower concentrations of Cu in the evaporation plume [19]. Following the discussion of the CIGS phase-diagram in Chapter 3, Cu-poor material forms an ordered defect compound (ODC) phase, typically $CuIn_3Se_5$ [1] [19], instead of the desired chalcopyrite phase. In a separate series of experiments this effect was used intentionally for deposition of the ODC-phase by LTPED. These samples were also investigated during this thesis, with results reported in Chapter 5.

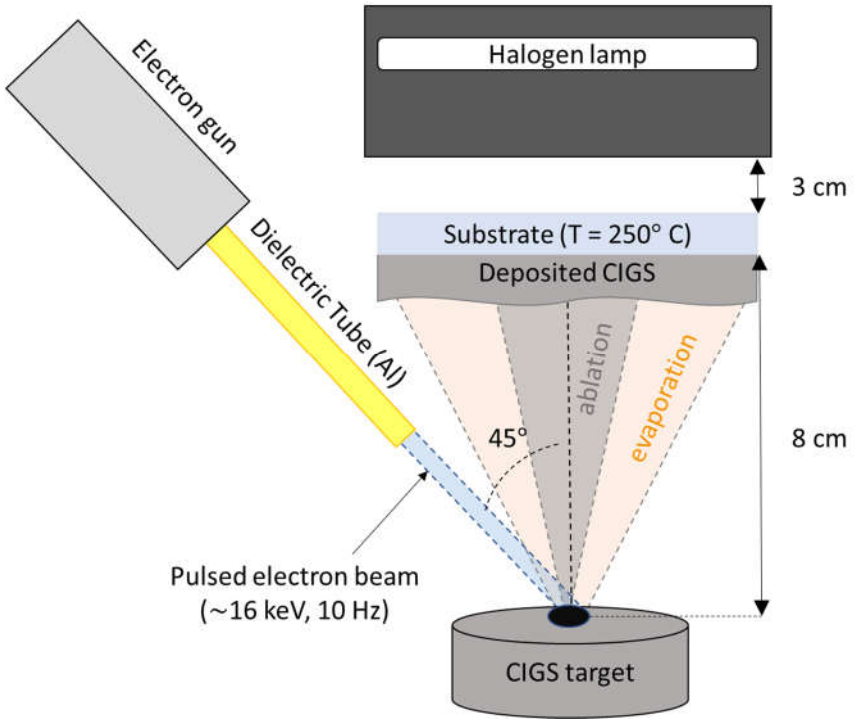


Figure 30 Schematic representation of the LTPED setup used at IMEM-CNR. The plasma plume formed during deposition consists of a plume of ablated material (grey cone) and a plume of evaporated material (orange cone) with different angular distribution and composition.

The LTPED setup at IMEM-CNR consists of a commercial PEBS-20 produced by Neocora Inc PED source, mounted inside a vacuum chamber. The setup is kept at 10^{-7} mbar on standby and filled with Argon (Ar) gas at 5N purity and $5 \cdot 10^{-3}$ mbar during depositions. The optimal deposition parameters for achieving good quality CIGS films at low temperature were found to be 16 kV acceleration voltage, a pulse repetition rate of 9 Hz and a substrate temperature of ~250 °C [54] [113]. The resulting electron beam has a pulse duration of ~200 ns pulse and a power density exceeding 10^8 W/cm^2. The conditions depend on the characteristics of the electron beam source, the CIGS target and the growth chamber.

Establishing the appropriate substrate temperature and acceleration voltage required careful analysis of their effects on the dominant mechanism for material transfer and crystallinity and composition of the deposited film [114] [115]. The substrate temperature mainly influences the crystallinity and composition of the deposited film. To obtain good crystallinity and compensate

for the Cu-poor material evaporated from the target by re-evaporation of Se-, In and Ga from the substrate, a temperature of at least 200 °C is required for LTPED deposition. Crystallinity and Na-diffusion into the absorber layer (see section 4.2) in principle only improve with increasing temperatures, but for temperatures above 300 °C evaporation of Se from the substrate results in excessive Se-loss (see Figure 31). The temperature of ~250°C was found as a good compromise. The acceleration voltage mainly influences the relative contributions from ablation and evaporation, the deposition rate and the film morphology. Acceleration voltages $V > 11.5$ kV are required to give rise to ablation from the target, while for $V > 14$ kV the contribution of evaporation is negligible. Increasing the acceleration voltage above 14 kV is desirable to achieve a higher deposition rate but also leads to a higher density and average size of particulates ablated from the target. Incorporation of these particulates in the bulk and surface of the deposited film leads to a negative effects on the film quality (see Chapter 6). At an acceleration voltage of 16 kV the best trade-off was found between a high deposition rate of ablated material and good film morphology (see Figure 31 and Figure 32).

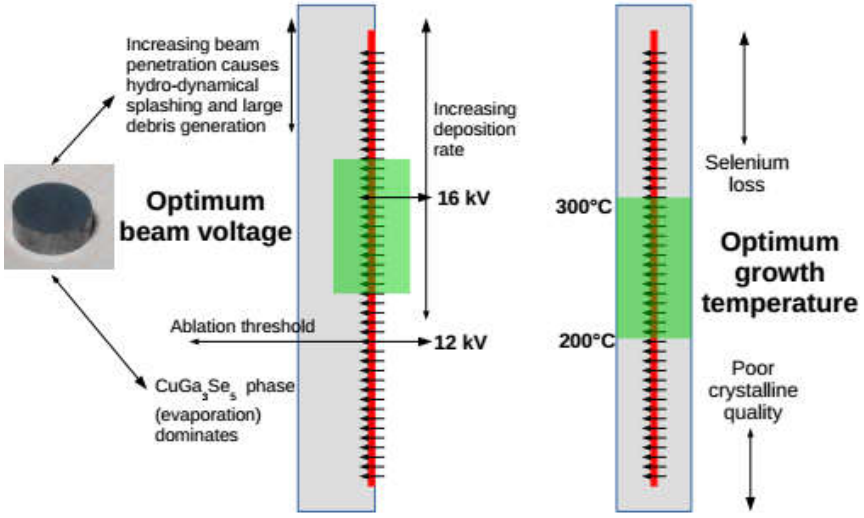


Figure 31 Indication of optimum values for the acceleration voltage for the LTPED and optimum substrate temperature to obtain good quality CIGS thin films [1]

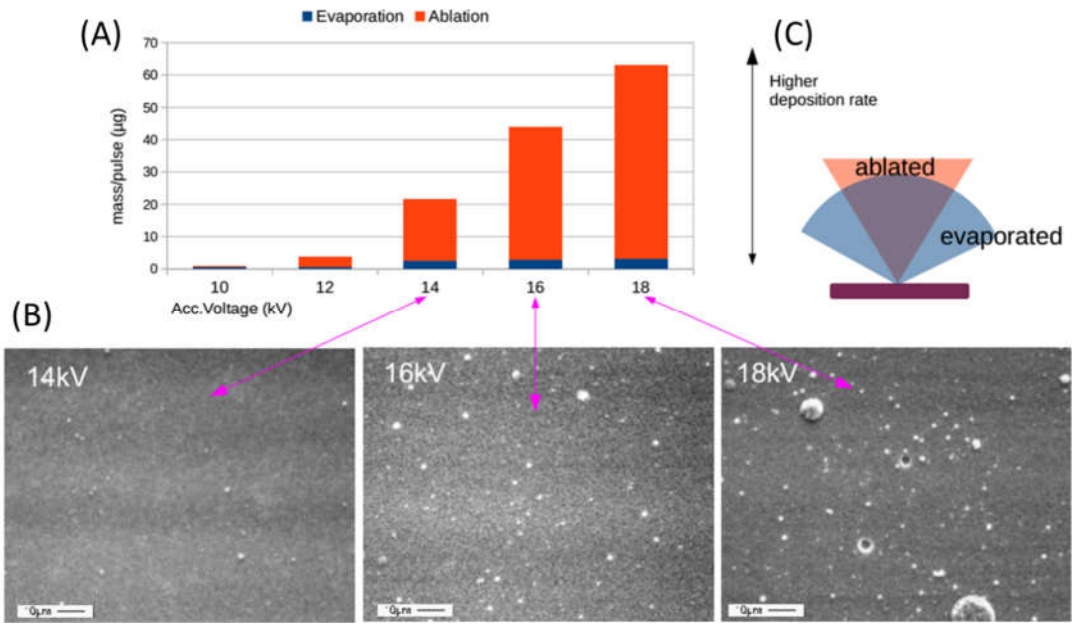


Figure 32 (A) Graph of deposition rate in µg/pulse as function of acceleration voltage in kV, with the contributions from evaporation and ablation indicated in orange and blue respectively. (B) Scanning Electron Microscopy (SEM) pictures of the surfaces for samples deposited at (from left to right) 14, 16 and 18 kV acceleration voltage. (C) Schematic indication of the different angular distributions of the ablation (orange) and evaporation (blue) plume [1].

4.1.2 Target preparation

The targets used for LTPED deposition of the CIGS absorber layer and the NaF precursor layer (see section 4.2) were also grown at IMEM-CNR. The CIGS targets were 1 cm thick disks with 2.5 cm diameter, grown by a modified liquid encapsulated Czochralski method. The different elements were added at 5N purity in the ratio corresponding to the desired stoichiometry and melted together at 897 °C under pressure in a semi-closed system in a quartz tube. The resulting melt was left to cool down to room temperature for two days resulting in the formation of the chalcopyrite phase. The NaF targets were 0.5 cm thick and 40 mm in diameter, created by cold pressing NaF powders with 5N purity at 200 bar for 10 minutes. The resulting pellets were then sintered at 900 °C for 12 hours to form the final target [54].

Usually, at the end of a deposition the surface layer of the target was found to have changed phase due to continuous heating. Before each new deposition 2000 electron beam pulses were

used to remove this layer. Uniform erosion of the targets was guaranteed by rotating the targets during deposition.

4.2 LTPED DEVICE ARCHITECTURE AND PREPARATION

The architecture and preparation approach used for LTPED devices went through some slight modifications during this thesis. Figure 33 shows the most recently established architecture on which the record efficiency of 17% was obtained and indicates the different deposition techniques used for each layer. Earlier architectures used during this thesis lacked a i-ZnO layer and had a thicker CdS buffer layer (~180-200 nm rather than 90 nm). Reduction of the CdS buffer layer thickness was possible after identification of a different approach to the chemical bath deposition (CBD) leading to more uniform CdS layers. In the remainder of this section the preparation of each layer will be briefly discussed.

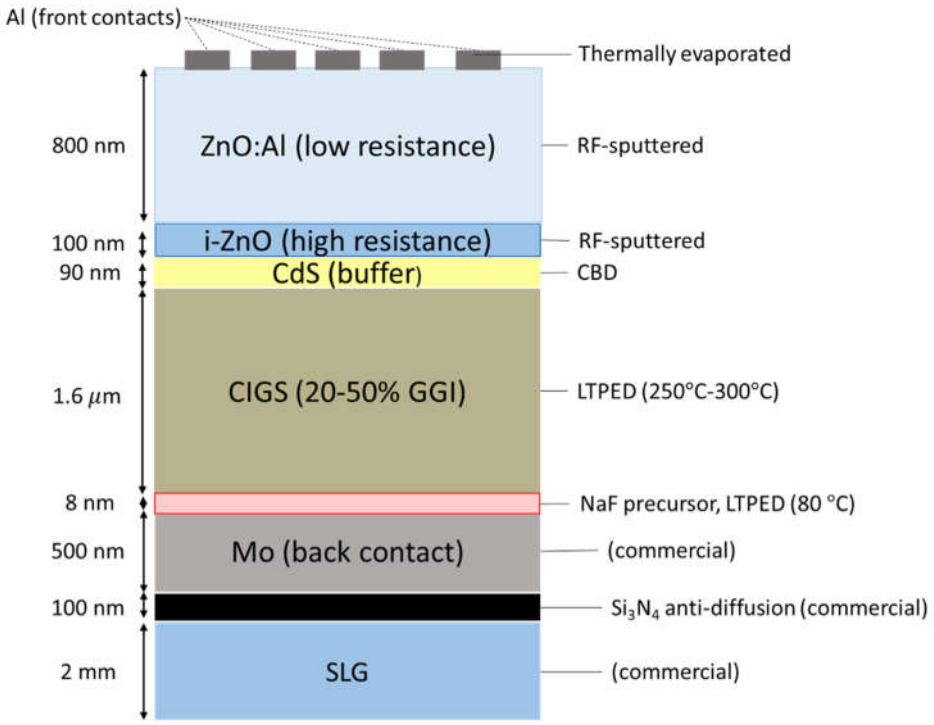


Figure 33 Architecture of typical LTPED-device. Substrates are 2.5 cm x 2.5 cm in size (see text).

Substrate: commercial SLG/Mo/Si_3N_4

The substrates used in LTPED-devices were 2 mm thick, 2.5 cm x 2.5 cm Soda Lime Glass (SLG) commercial substrates covered with 100 nm of Si_3N_4 and 700 nm DC-sputtered Mo, supplied directly by Singulus Technologies. The diffusion barrier was included to prevent Na diffusing from the SLG substrate, thus allowing a more controlled Na-doping using the NaF precursor (see below). Before use the substrates were cleaned in HNO_3 and HCl in ultrasound to remove any possible oxidation on the Mo back-contact.

Glass substrates with alternative back-contact materials were also investigated (see Table 3). Bifacial LTPED devices were obtained by using various transparent conducting oxides (TCO's) Until now, the most successful results have been obtained using fluoride-doped tin oxide (FTO), indium tin oxide (ITO) and aluminium-doped Zinc-Oxide (Al-ZnO) [116, 117].

NaF Precursor and CIGS absorber

Before deposition of the CIGS absorber layer a precursor layer of NaF was deposited by LTPED. The precursor was require since the low substrate temperature used for LTPED doesn't allow sufficient and homogeneous Na-diffusion from the SLG substrate. The LTPED deposition of the NaF layer was performed at an acceleration voltage of 14 kV a repetition rate of 10 Hz, and a substrate temperature of 80°C.

Even with inclusion of the NaF precursor layer, achieving sufficient Na-diffusion through the entire CIGS absorber layer at only 250 °C proved to be challenging. In this approach the thickness of the precursor layer is used to control the Na doping in the absorber. If a critical thickness of the NaF layer is exceeded, bad adhesion of the CIGS layer to the Mo-back follows, and eventually detachment of the CIGS absorber results. By tuning the thickness of the NaF precursor layer to the CIGS-absorber layer thickness and performing a post-deposition annealing step, a reasonable doping level was found to be achievable throughout the absorber layer while preventing problems of bad adhesion. For the standard architecture the optimal thicknesses were found to be 8-10 nm for the NaF precursor and ~1.6 μm for the CIGS absorber layer, as indicated in Figure 33. The post-deposition annealing is performed at 250 °C for 80 minutes.

Another important role of the NaF precursor layer in LTPED devices is to achieve an Ohmic or near-Ohmic back-contact at the CIGS/Mo interface. While in standard CIGS deposition approaches an ohmic contact is achieved by the formation of a $MoSe_2$ layer (see Chapter 3), this requires higher substrate temperatures than those used LTPED. The high Na-doping resulting from presence of the Na precursor layer is thought to result in formation of a thin highly doped (P^+) layer at the Mo/CIGS interface, allowing charge carriers to tunnel through the barrier at the back contact.

The deposition of the CIGS absorber layer was performed directly following the NaF precursor layer deposition, at 250 °C substrate temperature, 16 kV acceleration voltage and 9 Hz repetition rate. Most CIGS depositions were performed using a single CIGS target with the GGI desired for the absorber layer ($0.2 \leq GGI \leq 0.5$). For absorber layers with Ga-grading a rotatable target holder allowing up to four different targets was used. By rotating the target holder during deposition, CIGS layers with varying GGI could be achieved. Results from one sample deposited with two CIGS layers with different GGI are also reported in section 4.3.

Buffer layer: CdS

Chemical Bath Deposition (CBD) of the buffer layer was performed as soon as the sample was extracted from the vacuum chamber of the LTPED setup to minimize contamination of the absorber surface. The CIGS sample was first kept in a beaker containing double-distilled water and ammonia (NH_3) at room temperature for 5 minutes, after which $CdCl_2$ was added, followed by thiourea ($CS(NH_2)_2$) 2 minutes later. The beaker with sample and mixture were then placed in a bath of 80 °C, under continuous stirring of the mixture in the beaker. To remove the large clusters that were formed in the solution with time, each 10 minutes the solution is refreshed until the desired thickness of the CdS-layer has been achieved. The standard thickness of ~90-100 nm shown in Figure 33 is normally achieved in two steps. This thickness was found to give the best compromise between low absorption losses and sufficient shunt reduction by the CdS buffer layer.

Window layer (i-ZnO and Al-ZnO) and metallic front contacts (Al)

The architecture of the window layers used in LTPED-devices followed that discussed in Chapter 2: 100 nm undoped Zinc-Oxide (i-ZnO) was used to cover the CdS buffer layer to limit effects of shunting paths, and 800 nm aluminium-doped zinc-oxide (Al-ZnO) was used as final transparent front contact. Both layers were deposited by RF-sputtering at room temperature, using commercial 5 cm diameter targets from Testbourne Ltd. The targets underwent a cleaning process before deposition, which was performed at $5 \cdot 10^3$ mbar pressure of Ar-gas at room temperature. Sheet-resistances of $\geq 2 \cdot 10^6$ Ω/sq and 10-22 Ω/sq were found for the i-ZnO and Al-ZnO layers respectively, with transmittance of ~85% (±3%).

As front contact material usually 2 µm aluminium (Al) was deposited by thermal evaporation. In the most typical scheme for LTPED-devices a 4x4 grid of Al-contacts was used, each contact formed out of a single 1 mm dot connected to a 3 mm long finger (see Figure 34). Mechanical scribing was performed manually around the entire perimeter of the sample ~1 mm from the side, and small area cells of ~0.5-0.2 cm^2 are formed around each contact. The Mo-back contact is exposed at the bottom of the sample, also by mechanical scribing, and covered with some silver (Ag) paste to reduce series resistance.

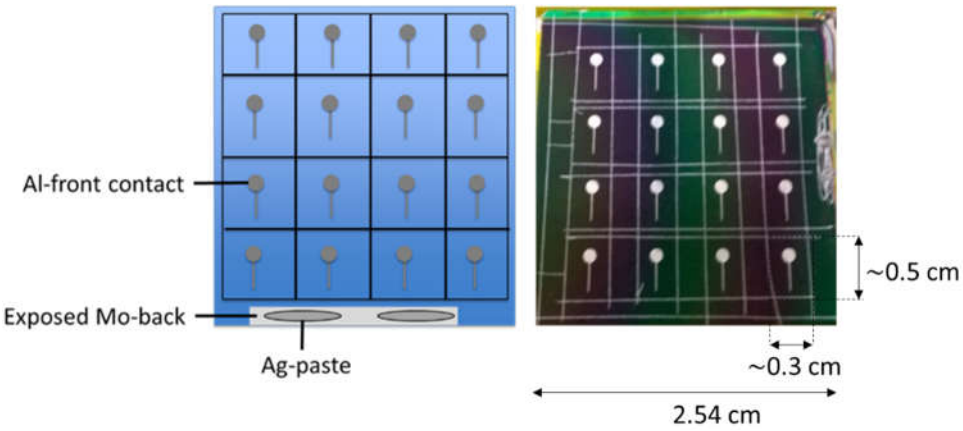


Figure 34 Typical contacting and scribing used for LTPED-devices

In some cases, it was preferred to perform contacting and scribing more ad-hoc, especially for samples demonstrating low uniformity. In this case smaller cells (~0.01 cm^2) were scribed and contacted with a Ag-paste.

Record efficiencies and current goals

As shown in Table 3, the record efficiency of 17.0% was reached on a laboratory scale device in the standard architecture discussed above, with a CIGS composition of GGI = 0.37. The corresponding J-V curve and external quantum efficiency (EQE) characteristics of the record efficiency sample are shown in Figure 35. Also shown in Table 3 are the record efficiencies reached on alternative architectures experimented with at IMEM-CNR. The highest efficiency reached on an alternative architecture was 14.7%, using a fluoride-doped tin oxide (FTO) substrate, also in this case using a composition of GGI = 0.37.

Table 3 Performance parameters of record cells obtained in four different architectures varying the back-contact materials. Adapted from [1]

Architecture	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)
CIGS/Mo/SLG	674	33.6	75.5	17.0
CIGS/FTO/SLG	652	30.8	73.3	14.7
CIGS/ITO/SLG	641	29.9	61.5	11.8
CIGS/ZnO:Al/SLG	635	26.6	54.5	9.3

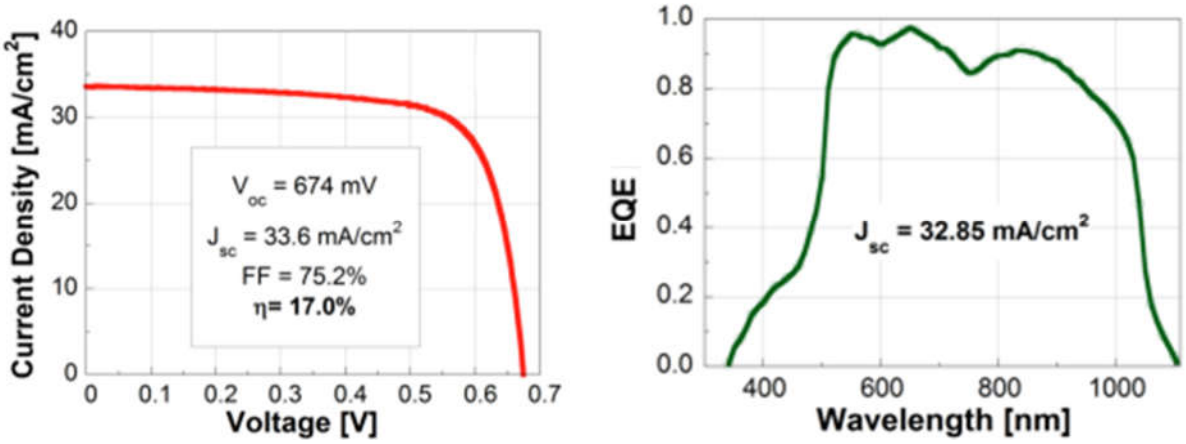


Figure 35 IV-characteristics (left) and spectral response (EQE) of the record-efficiency lab-scale solar cell (η = 17.0%) produced at IMEM-CNR in 2016, using the standard LTPED devices architecture [1]

The current limitations in LTPED devices mainly concern the reproducibility between samples and uniformity on single samples. The low processing temperatures make the quality of the deposited absorber layer highly sensitive to variations in other deposition parameters and limit the uniformity of Na-diffusion through the absorber. Nevertheless, the feasibility of the LTPED deposition technique has been proven with the achievement of good performing solar cells in both standard and innovative architectures [1] [116] [113]. After further optimization of sample reproducibility, LTPED might be a promising alternative to conventional deposition techniques.

4.3 TYPICAL ELECTRICAL CHARACTERISTICS OF LTPED DEVICES

In the current section results obtained from five LTPED devices are presented to illustrate the typical characteristics observed during this thesis. Reported are the standard performance (section 4.3.1) determined from IV-measurements (in the dark and under illumination) and external quantum efficiency (EQE) measurements, defect response and apparent free carrier densities (section 4.3.2) extracted using AS and C-V profiling and recombination parameters (section 4.3.3) extracted from IV-T and V_{OC}-T measurements. Nearly all results reported in this section were obtained on five different samples, for reference labelled A, B, C, D and E. Sample A was prepared according to the standard architecture and preparation of LTPED devices presented in section 4.2 of this chapter with CIGS composition GGI = 0.2. Samples B, C, D and E were all prepared without the highly resistive i-ZnO layer and with a CdS layer thickness of ~180-200 nm. Sample B, C and D were prepared with CIGS composition GGI = 0.3 while in sample E a bilayer structure was used for the CIGS absorber. Starting from the Mo-back contact, approximately 0.3-0.4 μm of CIGS with composition GGI = 0.5 was deposited, followed by ~1.2-1.3 μm of CIGS with composition GGI = 0.3. Different cells on each sample are distinguished by numerics (see Table 4).

4.3.1 Standard performance

The results of IV measurements in the dark and under illumination obtained on each cell are shown in **Error! Reference source not found.**, with basic performance parameters shown in Table 4. The efficiencies range from 6.4% (cell C-2) to 13.5% (cell E-1). For cell C-2 both the efficiency and V_{OC} (387 mV) lie outside of the typical range observed in LTPED devices: the range of efficiencies and V_{OC}'s usually lie in the range of $10\% \leq \eta \leq 15\%$ and $500\ mV \leq V_{OC} \leq 600\ mV$ respectively. The higher V_{OC} in cell E-1 is most likely due to the application of bandgap grading in the device. The results from cells C-2 and E-1 aren't considered in the mean and standard deviations of the performance parameters in

Table 5. Instead, they are used as examples of low efficiency and bandgap-graded LTPED devices in the following.

Upon comparing the performance parameters η, J_{SC}, V_{OC} and FF of cells A-1, B-1, C-1, D-1 and D-2 a relatively low variation is observed ($\leq$ 10%, see

Table 5). The average values of the VOC (~ 574 mV) and FF (~70%) also correspond well with typical values observed in LTPED-devices. The average J_{SC} (~27 mA/cm2) for these samples is somewhat low, as usually ~28-32 mA/cm2 would be expected. The R_S and R_{Sh} show very high variations between cells both in dark and illuminated conditions. Average values of R_S ~1.3 $\Omega \cdot$cm2 ($\pm$ 58 rel. %) and R_{Sh} ~ 9157 $\Omega \cdot$ cm2 ($\pm$ 79 rel. %) are observed in the dark. The large variations in R_S and R_{Sh} indicate variation in the amount of shunting (possibly due to the mechanical scribing) and series resistance (possibly due to variations in the ohmicity of the front/back-contact, the interface between CIGS and the CdS buffer layer, and in the free carrier density in the absorber) have an important contribution to limiting uniformity and reproducibility of the device quality.

Table 4.

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Table 4 Composition, architecture and standard performance parameters of LTPED-devices for which results are presented in the current section. Letters indicate different samples and numbers indicate different cells on each sample. Apart from the specified properties (GGI, CdS-layer thickness, presence of i-ZnO) the architecture and preparation as described in section 4.2 was used. The value of ΔR_S and ΔR_{Sh} give the relative variation between the R_S and R_{Sh} under illumination and in the dark. *Cell C-2 showed a clear red-kink effect and therefore bias-dependent R_S. The reported value of 0.8 $\Omega \cdot cm^2$ was measured for $V > 0.7$ V, while for lower bias a resistance of 1.8 $\Omega \cdot cm^2$ was measured. 'Dark' refers to dark conditions at 25°C, while 'STC' refers to illumination with AM1.5 at 1 sun, at a sample temperature of 25°C.

	Standard	Without i-ZnO					
Cell	**A-1**	**B-1**	**C-1**	**C-2**	**D-1**	**D-2**	**E-1**
CdS (nm)	90-100	180-200					
GGI (%)	20	30					30/50
STC							
η (%)	12.0	10.2	10.7	6.4	12.1	10.7	13.5
V_{OC} (mV)	575.8	541.3	577.0	386.9	590.9	584.8	619.9
J_{SC} (mA/cm^2)	28.0	29.3	23.7	26.2	27.2	24.7	28.6
FF (%)	75.0	60.7	74.2	59.9	71.3	70.3	76.0

R_S ($\Omega \cdot cm^2$)	0.24	0.88	1.2	*0.8**	2.0	1.9	0.9
R_{Sh}($\Omega \cdot cm^2$)	870	476	16670	300	606	385	833
Dark							
R_S ($\Omega \cdot cm^2$)	0.45	0.8	1.2	1.0	2.0	1.8	1.4
R_{Sh}($\Omega \cdot cm^2$)	1266	16670	16670	180	11000	180	1000
ΔR_S (%)	**-47%**	**+10%**	0%	**-20%***	0%	**+6%**	**-36%**
ΔR_{Sh} (%)	**-31%**	**-97%**	0%	**+67%**	**-94%**	**+114%**	**-17%**

As shown explicitly in Table 4, most cells demonstrate a strong difference between the values of R_S and R_{Sh} in the dark and under illumination. In some cells a very large reduction in R_S is observed: -47% for cell A-1, -20% for cell C-2 and -36% for cell E-1. In the other cells little or no reduction ($\leq$ 10%) is observed. This suggests that in some cases a barrier is present for charge carrier collection which is significantly reduced under illumination. Such effects of illumination have been explained by a variation in the conduction band offset (CBO) at the CIGS/CdS interface, or a reduction in the voltage drop across the CdS/CIGS interface due to the photo-excitation of holes close to the interface [8]. Another possible explanation would be a barrier formed at the Mo/CIGS interface in opposite direction of the diode of the cell, thus limiting the forward current. As was observed during some experiments performed during this thesis (Appendix B. CIGS/Mo interface) in some cases a photovoltaic effect occurs in such a barrier, so that illumination reduces the limitation of the forward current. The observed change in R_{Sh} with illumination also varies significantly between different cells. Increase in the range of +67% $\leq \Delta R_{Sh} \leq$ +114% is observed for cells C-2 and D-2, and a decrease in the range -97% $\leq \Delta R_{Sh} \leq$ -17% is observed for cells A-1, B-1, D-1 and E-1. From these results it appears illumination also has a significant effect on the R_{Sh} of LTPED-devices. However, no consistent correlation is found and most likely a number of different effects play a role. The decrease in R_{Sh} can be explained by photoconductive shunting paths. The increase in R_{Sh} was only observed in cells for which the dark R_{Sh} was quite low ($R_{Sh} \sim 180\ \Omega \cdot cm^2$).

Table 5 Comparison of the range, mean and relative standard deviation of the performance parameters calculated for cells A-1, B-1, C-1, D-1 and D-2. Here it should be noted that cell A-1 has a slightly lower bandgap (GGI = 0.2). 'Dark' refers to dark conditions at 25°C, while 'STC' refers to illumination with AM1.5 at 1 sun, at a sample temperature of 25°C.

	Parameter	Range	Mean	Standard
STC	η (%)	10.2-12.1	11.1	7%
	V_{OC} (mV)	541-591	574	3%
	J_{SC} (mA/cm^2)	23.7-29.3	26.6	2%
	FF (%)	61-75	70	5%
	R_S ($\Omega \cdot$cm^2)	0.2-2	1.2	65%
	R_{Sh}($\Omega \cdot$cm^2)	476-16670	3801	170%
Dark	R_S ($\Omega \cdot$cm^2)	0.5-2	1.3	58%
	R_{Sh}($\Omega \cdot$cm^2)	180-16670	9157	79%

The EQE curves shown in Figure 36 were obtained from cells sample A (yellow curve) and sample E (black curve) and two cells with the same architecture as samples B, C, D and E with GGI = 0.3 (blue curve) and GGI = 0.375 (red curve) that aren't considered in the remainder of this chapter.

In the range of 520 nm $\leq \lambda \leq$ 800 nm a quantum efficiency > 70% is measured for all cells. In the same region, the large peaks show strong interference due to reflection from the interfaces at the different interfaces. In the range 800 nm $\leq \lambda \leq$ 1000 nm a decrease of the EQE is always observed, starting at different wavelengths for the different cells, dropping below 70% EQE for $\lambda \geq$ 800 nm. Here the differences in GGI are observed as a reduction in the absorption of the longest wavelengths (i.e. lower photon energy) with increasing GGI (i.e. higher bandgap). The 'shoulder' observed in the 400-500 nm range shows the large effect of the CdS layer on the absorption of LTPED-devices (as in most CIGS devices) which absorbs part of the incident light in this range.

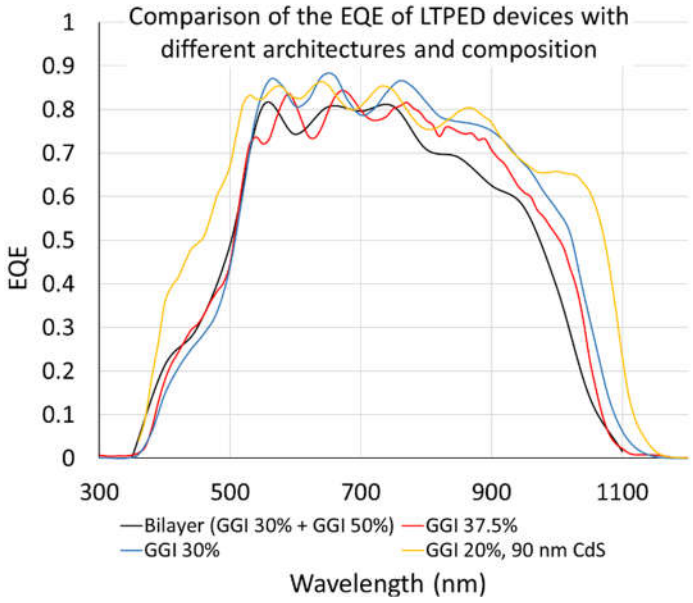


Figure 36 Comparison of EQE curves measured on four different LTPED devices with slight differences in architecture and GGI. Yellow curve = 90 nm CdS + 100 nm i-ZnO and GGI = 0.2, blue curve = 180 nm CdS without i-ZnO and GGI = 0.3, red curve = 180 nm CdS without i-ZnO and GGI = 0.375, black curve = 180 nm CdS without i-ZnO and bilayer GGI (0.3 + 0.5)

4.3.2 Defect response and charge carrier density

The defect response for all cells was analysed using AS. The corresponding C-f profiles are shown in Figure 37 and Figure 38Figure 38, with indications of the apparent free carrier density N and depletion layer width w determined by C-V profiling. The appropriate temperature and frequency at which to perform the C-V measurements were determined using the AS-spectra from the regions in which saturation of the C-f curves was observed. This occurred at low temperature and high frequency in all cells, so that for each cell the measured N-w profiles (see

Table 6 and Figure 40) were expected to be accurate. The N-w profiles aren't reported for cells B-1, C-2, D-1 and D-2 as they were found to have a completely depleted absorber, i.e. the depletion layer didn't change with applied bias in C-V measurements.

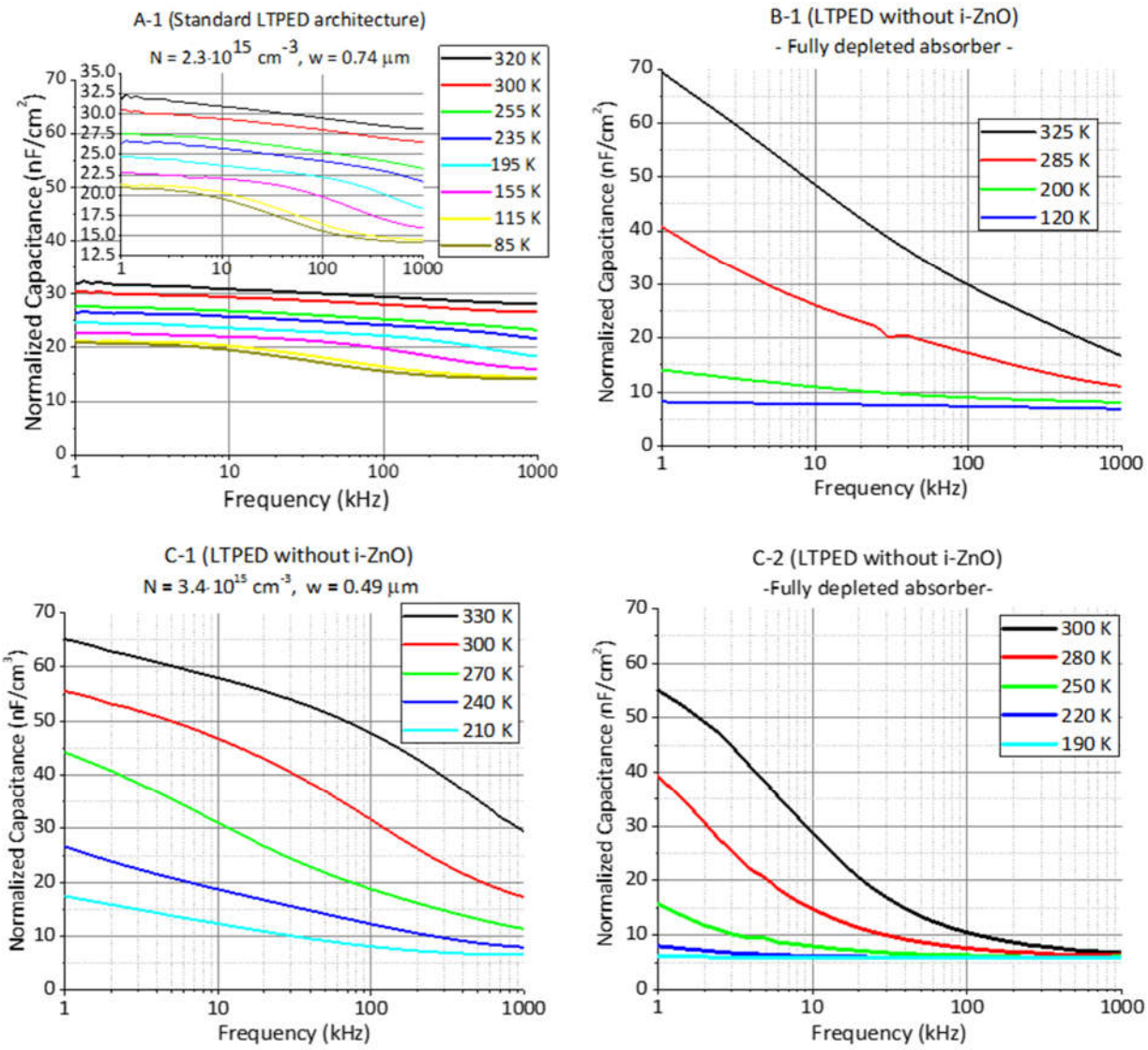


Figure 37 AS-spectra obtained for LTPED devices A-1, B-1, C-1 and C-2. Cell A-1 has GGI = 0.2 and is the only cell with an i-ZnO layer and 90 nm CdS layer. All other cells have GGI = 0.3, no i-ZnO layer and 180 nm CdS layer. The inset was added for cell A-1 to give a better indication of the variation with temperature, not observable in the same scale used for the other cells. A 25 mV oscillation amplitude was used for the capacitance measurements.

A large reduction in the capacitance with reducing temperature and frequency is found in all samples, indicating a high contribution from defects to the measured capacitance in each case. A nearly monotonic decrease in capacitance (i.e. with little or no variation in the slope) is usually observed at high temperature and low frequencies for all cells, with exception of C-2 where a distinct step occurs and is only visible at low frequency at each temperature. For cells A-1 and C-1 at high frequencies ($f \geq 100$ kHz) a sharper more distinct step is also observed, for A-1 only for $T \leq 195$ K and for C-1 already at the highest temperature (330 K).

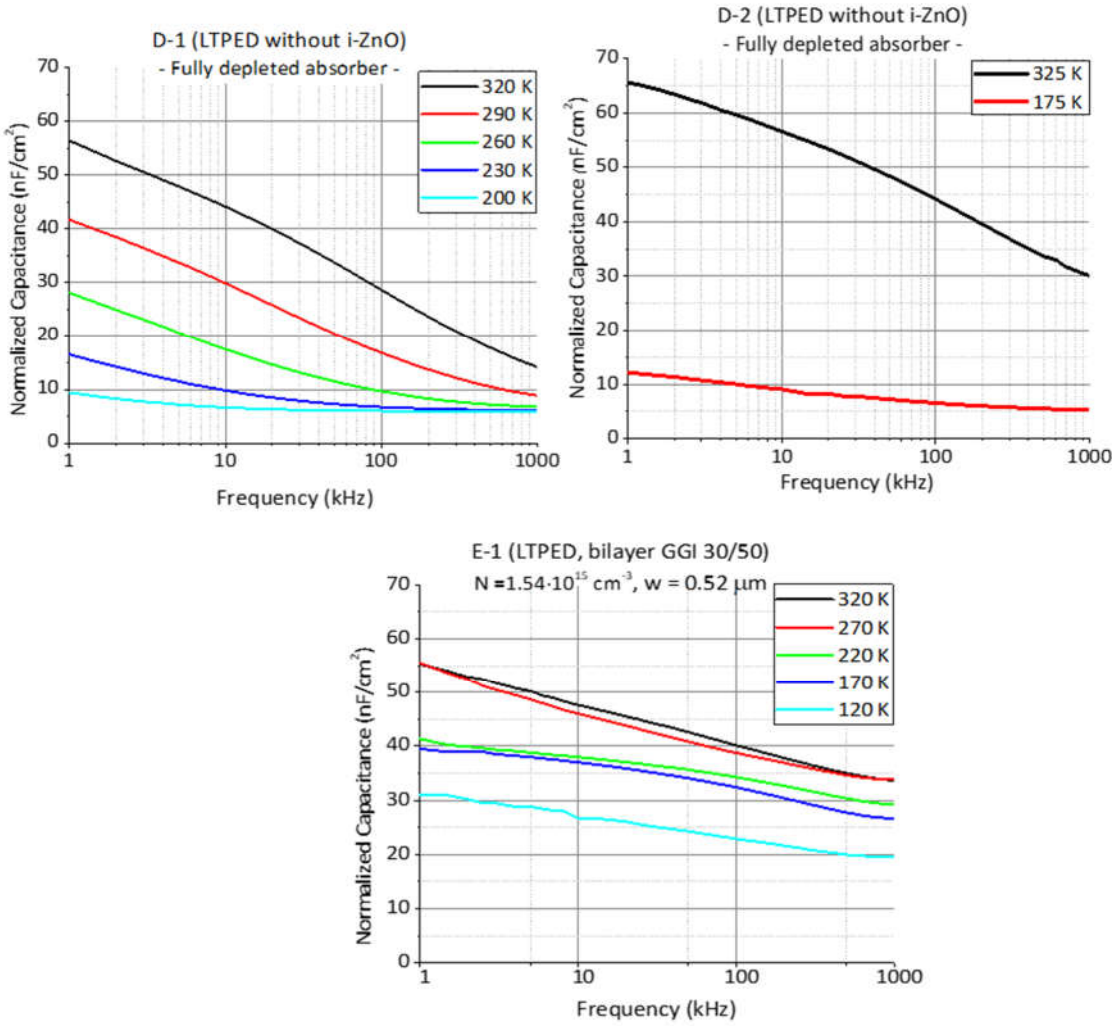


Figure 38 AS-spectra for cell D-1 (top-left), D-2 (top-right) and cell E-1 (bottom). Cells D-1 and D-2 have GGI = 0.3, while in cell E-1 a bilayer (GGI = 0.3 + GGI = 0.5) was applied. All cells lack a i-ZnO layer and have a 180 nm CdS layer.

The observation of a monotonic decrease at low frequencies and high temperature and a sharper step at higher frequencies/lower temperatures corresponds well with the respective N2 and N1 steps typically observed in AS-spectroscopy in CIGS-based devices (see Chapter 3). Hence, in the following the monotonic decrease at lower frequency and higher temperature will be referred to as N1 while the sharper step at higher frequency and lower temperature will be referred to as N2 also in the current results. Both the size of the N1 and N2 steps and the range of frequencies and temperatures over which they occur vary between different cells. The total step size in capacitance between the highest temperature at 1 kHz and the lowest temperature at 1 MHz (ΔC_{tot}) gives an indication of the concentration of majority carrier traps that stop responding within the frequency range. The range of temperatures and frequencies over which the step occurs indicates the range of activation energies for which a significant concentration of contributing defects is present.

Cell A-1 would clearly have the lowest defect concentration, as the total variation in capacitance is only ΔC_{tot} ~18 nF/cm^2, corresponding to ~56 % of the initial capacitance. Of the total variation in capacitance, the N2 step would appear to contribute ~12 nF/cm^2, i.e. ~2/3 of the total defect contribution. The N1 step would appear to contribute ~6 nF/cm^2, ~1/3 of the total defect contribution. The N2 step appears to be due to defects widely distributed in activation energies, starting at energies deep inside the absorber bandgap. The N1 step appears to be related to very shallow defects, since the step only becomes observable for $T < 200$ K, with a narrow distribution of defect energies.

For cells B-1, D-1, D-2 and E-1 a large variation in capacitance is also observed, but no different steps can be clearly distinguished. The activation energies of the contributing defects appears to be distributed continuously throughout deep and shallow energies inside the bandgap. The total capacitance variations ΔC_{tot} in the different cells are observed as 63.1 nF/cm^2 (B-1), 49.7 nF/cm^2 (D-1), 60.3 nf/cm^2 (D-2) and 36.1 nF/cm^2 (E-1), indicating ~90%, ~88%, ~92% and ~65% respectively of the C_0 values for these cells can be attributed to defect response.

For cell C-1 the total capacitance step $\Delta C_{tot} \sim 59$ nF/cm^2 is ~90% of the initial capacitance value. The contribution from the N2 step would appear to be ~25 nF/cm^2 or 42% of the total defect contribution, while that from the N1 step would appear to be ~33.9 nF/cm^2, ~58% of the total defect contribution. For cell C-2 a large step of ~49 nF/cm^2 occurs at low frequencies, which corresponds to ~89% of the original capacitance value. Occurrence of this step at low frequencies (~1 kHz $\leq f \leq$ 100 kHz) at a temperature of 300 K indicates the centre of the corresponding trap distribution lies deep inside the bandgap. In both cells the capacitance is clearly seen to saturate at high frequencies and ~200 K, indicating a relatively low concentration of shallow defects. This would suggest the doping in these samples is also relatively low, in particular for cell C-2 where the same value of C_∞ is obtained at low and high temperature. This is found to be in agreement with the values of N obtained form C-V profiling (see Figure 40 and

Table 6).

For four cells (A-1, C-1, C-2 and D-1) reasonably clear peaks were observable in the $\left[-\omega \cdot \frac{dC}{d\omega}\right]$ curves. The Arrhenius plots constructed from the analysis of these peaks are shown in Figure 39.

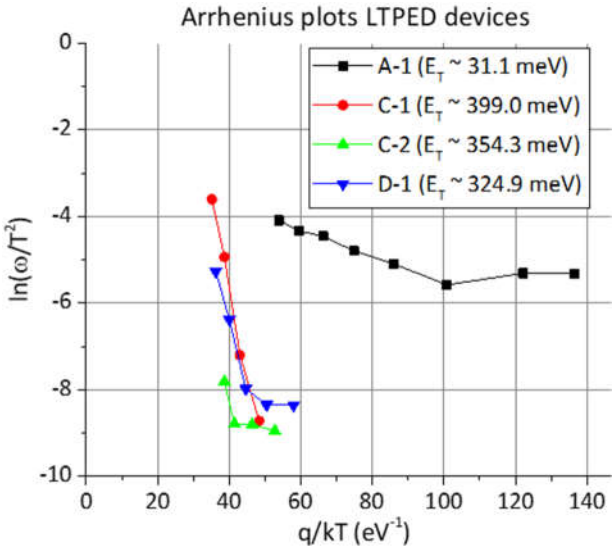


Figure 39 Arrhenius plots of peak locations ω_0 in the $\left[-\omega \cdot \frac{dC}{d\omega}\right]$ profiles against $\ln\left(\frac{\omega_0}{T^2}\right)$ for cells A-1 (black squares), C-1 (red circles), C-2 (green up-triangles) and D-1 (blue down-triangles). The indicated trap energies E_d were estimated from the linear region of each plot at high temperature (i.e. lower values of $\frac{q}{kT}$)

For cell C-2, the inflection point in the C-f curves could only be accurately identified for two temperatures, so that essentially only two points appeared reliable in the final Arrhenius plot. The slope obtained by interpolating between the two points of ~354.3 meV agreed well with those observed for cell C-1 and D-1 of ~399.0 meV and ~324 meV respectively. These results suggest a deep trap level at 320-400 meV from the VBE, in each of the samples. This relatively high value for E_d, which would agree best with that usually reported for the N2 step and the V_{Se} defects of ~290-300 meV [118] [119], contradicts the expected correspondence to the typical N1 step, reported to have E_d~100 meV. Since normally the N1 step is reported to be an interfacial defect with E_d varying with surface treatment or annealing, a possible explanation for the higher value of E_d could be interfacial states with different activation energies, due to the different processing of LTPED devices than most commonly reported CIGS-based devices.

In contrast, the value of E_d obtained for cell A-1 is ~31.1 meV from the VBE. If the explanation given in the preceding paragraph is correct, this would indicate interfacial defects in cell A-1 with a much lower activation energies than in cells C-1, C-2 and D-1. Differences in interfacial states between these cells might be explicable, since sample A was prepared using the most recent CBD process at IMEM-CNR, while samples C and D were older and prepared with the preceding CBD process.

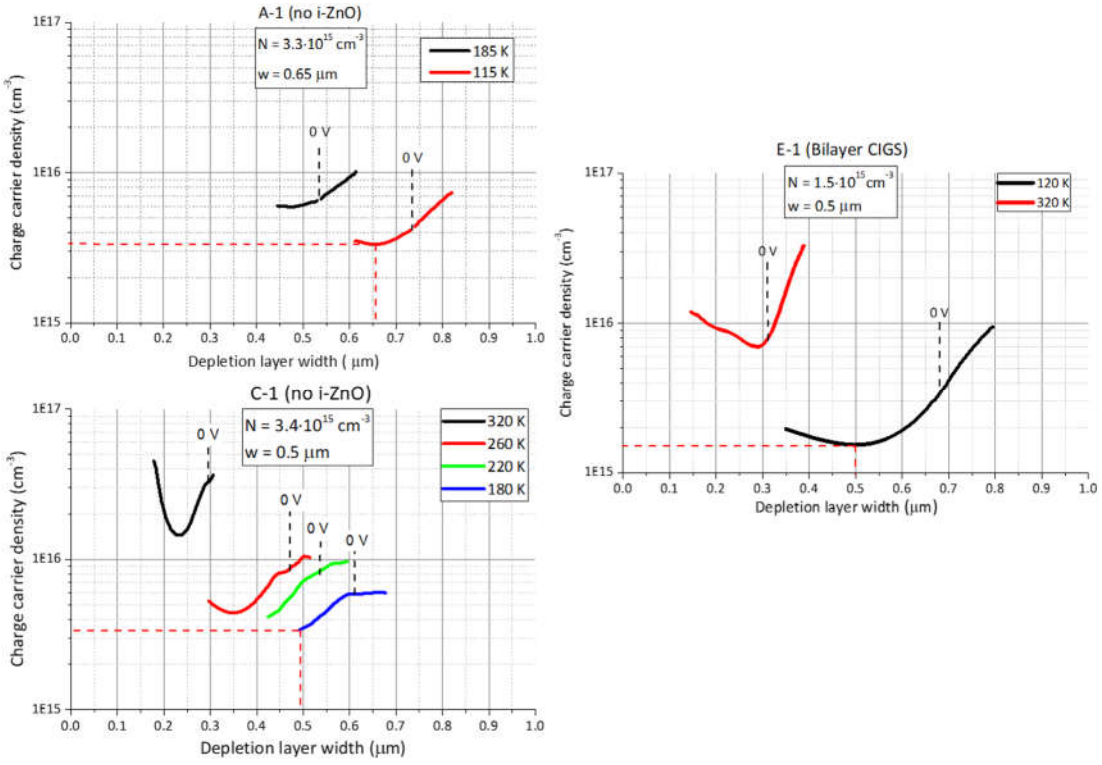


Figure 40 Apparent free carrier density (N-w) profiles determined by *C-V* for cells A-1, C-1 and E-1. For the small-amplitude AC-signal a 1 MHz frequency and 25 mV amplitude were used. The profiles are shown also for higher temperatures, to illustrate the significant effect of defect response to the calculated charge carrier density N and calculated depletion layer width w. Red dashed lines indicate the points from which the effective carrier densities were taken, i.e. at the minima of the profiles measured at 115 K (A-1), 180 K (C-1) and 120 K (E-1).

The apparent free carrier density profiles obtained for cells A-1, C-1 and E-1 are shown in Figure 40. The results for cells B-1, C-2, D-1 and D-2 aren't shown since these were found to have a completely depleted absorber layer, indicating a free carrier density $N \ll 10^{15}$ cm^{-3} (see

Table 6). In these samples the value of the depletion layer width would be expected to correspond approximately to the thickness of the CIGS absorber layer, i.e. ~1.6-2 µm. This was found to be the case for each cell, with some error due to some uncertainty in the actual area of the device contributing to the capacitance.

The doping density and depletion layer are seen to be highly temperature dependent, reflecting the strong contribution from defects at high temperatures. Note that although for cell C-1 the C-V profiling was performed at 180 K (i.e. at higher temperatures than for the other cells) the C-f curves showed saturation from $\mathrm{T} < 210$ K, so that the obtained carrier density was still considered to be accurate. All N-w profiles of the non-depleted cells have the typical 'U'-shape often reported for CIGS-based devices (see section 3.1.1.3 and references [101] [74] [120]). Different explanations have been given for this shape in N-w profiles in CIGS devices. The increase with reducing depletion layer width has been explained as an actual increase of the charge carrier density toward the CdS/CIGS heterointerface. However the accuracy of the increase toward the heterointerface is questionable as it is only observed at high temperatures and relatively high forward bias conditions ($\mathrm{V} \geq 0.4$ V) for which the forward current density might make the measured capacitance value inaccurate. The increase toward the back-contact has also been explained as an increase in carrier density toward the CIGS/Mo back-contact, but another explanation often given is a response of deep defect states to the slowly varying DC-bias. Charging of these deep defects during the longer application of reverse bias would lead to an apparent increase in the charge carrier density [101].

The depletion layer widths extracted at the minimum of the reported profiles (see

Table 6) are found to be ~0.5 μm for cells C-1 and E-1 and ~0.75 μm for cell A-1, corresponding to carrier densities in the range of $1.5 \cdot 10^{15}$ $cm^{-3} \leq N \leq 3.4 \cdot 10^{15}$ cm^{-3}.

Table 6 Free carrier densities (N) and depletion layer widths (w) derived from the low-temperature (T, indicated for each sample) and high-frequency ($f = 1$ MHz) C-V profiles. For the samples that showed complete depletion, the observed value of w is reported, while N indicates the lower bound from consideration of CIGS material properties. The C-V measurements were performed using a 25 mV amplitude for the AC-signal.

Cell	η	N	w	Measurement temperature
A-1	12.0	2.3	0.75	115
B-1	10.2	$\ll 1$	1.8	120
C-1	10.7	3.4	0.5	180
C-2	6.4	$\ll 1$	1.8	270
D-1	12.1	$\ll 1$	2	120
D-2	10.7	$\ll 1$	2	115
E-1	13.5	1.5	0.5	120

The relatively low doping levels observed in LTPED devices compared to the optimum (i.e. $\sim 10^{17}$ cm^{-3} [6]) and the large number of cells with fully depleted absorber layer reflect the difficulty of obtaining sufficiently high Na-doping at the low temperature used for LTPED. The strong variation on sample C (i.e. C-1 having N$\sim 3.4 \cdot 10^{15}$ cm^{-3} and w$\sim$0.5 μm while C-2 is found fully depleted with) also shows Na-diffusion is typically non-uniform across the sample at such low temperature.

No very clear correlation was found from between these results and the cell efficiency: both the fully depleted cell D-1 and the cell A-1 with w $\sim$ 0.75 μm and N $\sim 2.3 \cdot 10^{15}$ cm^{-3} show efficiencies of $\sim$12%. while the efficiency of cell C-1 (η = 10.7%, N = $3.4 \cdot 10^{15}$ cm^{-3} and w = 0.5 μm) is among the lowest efficiencies. Furthermore, also the record efficiency cells obtained by LTPED were found to have doping densities in the order of $\sim 10^{15}$ cm^{-3} at 120 K [54] [113].

4.3.3 Recombination mechanisms

For cells A-1, B-1, C-1, C-2, and E-1 the V_{OC}-T characteristics (Figure 41) and dark IV-T characteristics (Figure 42) were determined to identify the main recombination mechanisms limiting cell performance.

The behaviour of the V_{OC} as function of temperature is approximately linear in the region 200 K $\leq T \leq$ 350 K for each cell. The non-linearity and saturation observed for $T <$ 200 K in most samples are an indication of a change of recombination mechanism corresponding to tunnelling and freezing out of charge carriers. The intercepts with the vertical axis obtained from linear fits of the high temperature region lie within the range of 687 mV (cell C-2) to 1144 mV (cell C-1).

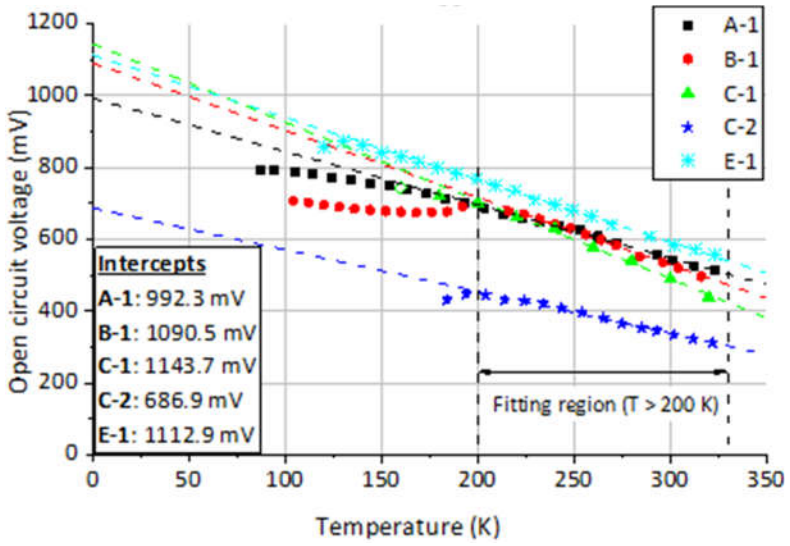


Figure 41 Measured temperature dependence of the open-circuit voltage (V_{OC}) for cells A-1 (full black squares), B-1 (red circles), C-1 (green triangles) C-2 (blue stars) and E-1 (cyan asterisks)

As explained in section 3.1.2.3, the intercept of the V_{OC}-T curve gives an indication of the activation energy E_a of the dominant recombination mechanism. The obtained values of E_a are shown in Table 7. Values of ~1100 meV (close to the absorber bandgap, ~1.1-1.2 eV) were observed for cells B-1, C-2 and E-1, indicating Shockley-Read-Hall (SRH) recombination is the dominant recombination mechanism limiting the V_{OC} in these cells. For cell C-2 the obtained intercept leads to $E_a \sim 0.69$ eV, i.e. an alternative recombination path to SRH recombination limits the V_{OC}. Recombination mechanisms with much lower activation energies than the absorber take place at other locations in the cell, typically at the CdS/CIGS interface in the form of interface or tunnelling-enhanced interface recombination. The activation energy would then be equal to the hole barrier for recombination at the interface [104] [121]. The high amount of interface recombination is consistent with the much lower V_{OC} of cell C-2.

From Figure 41, it can be noted that the range in which the V_{OC}-T characteristics showed linear behaviour varied strongly between the different cells. For cell E-1 the entire range of 150 K $\leq$ T $\leq$ 350 K was found to give a good linear fit with intercept ~1113.9 mV. For cell A-1 a linear fit for T >243 K gave a slope of ~1040 meV, while for lower temperatures intercepts < 1000 meV were obtained. This suggests interface recombination is absent in the entire range 150 K $\leq$ T $\leq$ 350 K for cell E-1, while it already becomes an important limiting recombination mechanism for T $\leq$ 243 K in cell A-1.

Table 7 Efficiency η measured at STC, ideality factor A and activation energies E_a of the main recombination mechanisms calculated from V_{OC}-T and IV-T measurements

Cell	η(%)	A (at RT)	E_a-V_{OC} (meV)	E_a-IV-T (meV)
A-1	12.0	1.7	994	890
B-1	10.2	2.0	1085	1440
C-1	10.7	1.6	1162	1072
C-2	6.4	2.4	690	1435
E-1	13.5	1.5	1089	1113

In the lower bias region 0 V $\leq V \leq$ 0.25 V of the dark IV-T curves (Figure 42) the current densities are observed to be $\geq 10^{-1}$ mA/cm^2 and relatively independent of temperature for all cells except B-1 and E-1. This temperature independence suggests the dominant recombination mechanism isn't thermally activated but rather limited by tunnelling.

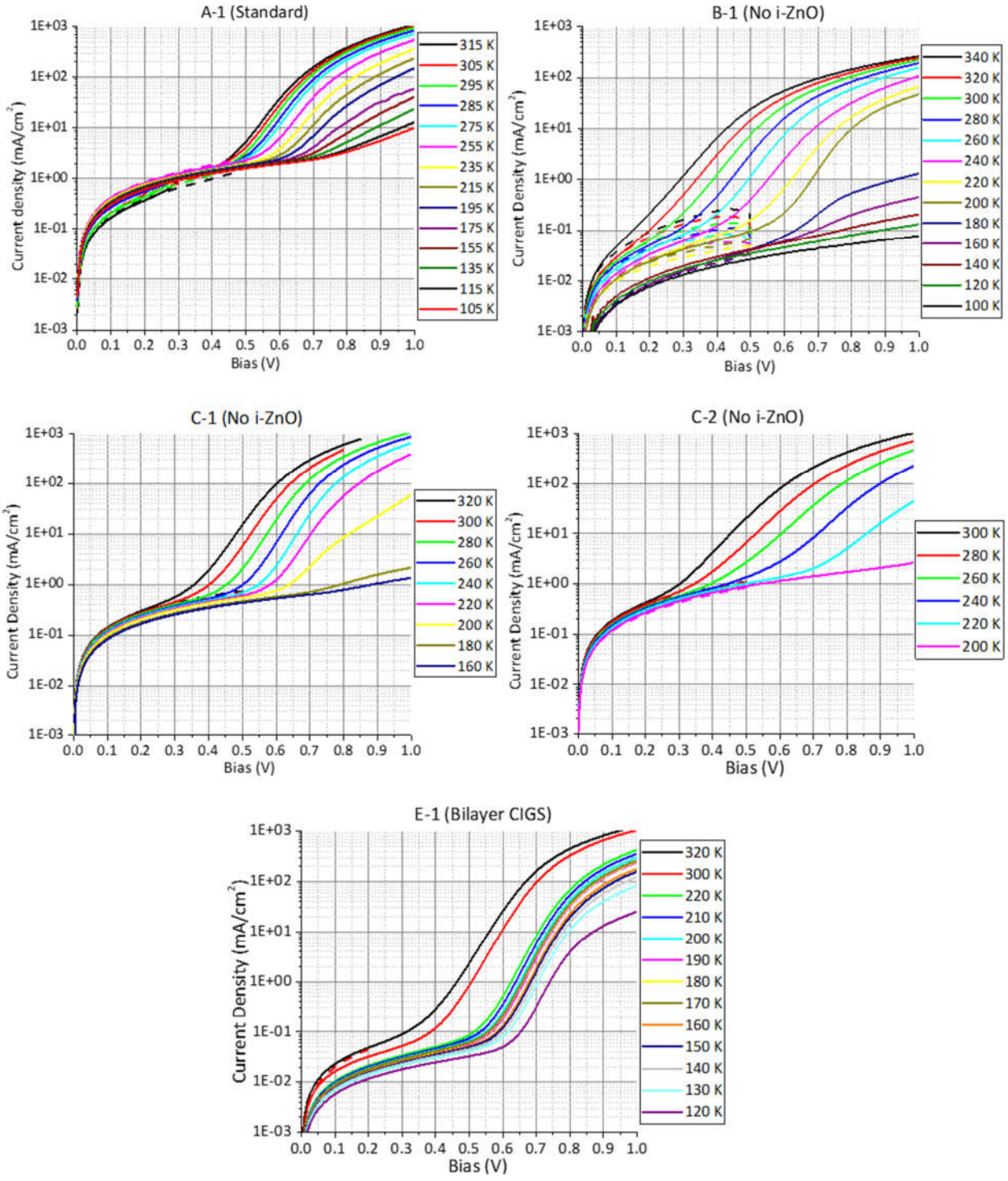


Figure 42 Dark IV-T curves for cells A-1, B-1, C-1, C-2 and E-1. Full lines indicate the forward current density, dashed lines indicate the reverse current density.

For each cell the ideality factor A and saturation current density J_0 were fitted as function of temperature from the characteristics showing good diode behaviour (~0.4 V $\leq V \leq$ 0.8 V at room temperature) following the procedure described in [29]. For all cells except E-1 this region quickly becomes smaller as the temperature is reduced, and nearly overlaps with the reverse bias at $\mathrm{T} <$ 120 K. For cell E-1, even at 120 K good diode quality is observed in this range. Accordingly, cell E-1 shows a much lower ideality factor ($A\sim$ 1.5) and much higher efficiency (η = 13.5%) than the other cells. Also for cells A-1 and C-1 low ideality factors (1.7 and 1.6 respectively) were found, but in this case quickly increase for lower temperature, indicating a larger contribution of tunnelling in these cells. Generally, values of 1.5 $\leq A \leq$ 2.4 were found for the ideality factors (see Table 7). The highest value of 2.4 corresponds to the worst performing cell C-2, as would be expected. The ideality factors in the range 1.3 $\leq A \leq$ 2 observed for cells A-1, B-1, C-1 and E-1 indicate SRH recombination in the space charge region of the absorber layer [29].

In Figure 43 the constructed Arrhenius plot of $A \cdot \ln(\mathrm{J}_0)$ (see section 3.1.2.2) are shown. From the slopes of the linear regions in the plots the activation energy E_a of the dominant recombination mechanisms were extracted (see also Table 7). For cells C-1 and E-1 E_a was found quite close to the expected bandgap of the absorber: E_a~1072 meV for C-1 and E_a~1113 meV for cell E-1, indicating SRH recombination also limits the recombination of injected charge carriers in the dark in these cells. The activation energy of cell A-1 was somewhat below the expected bandgap, at E_a~890 meV, again showing a contribution from what is most likely interface recombination. Finally, cells B-1 and C-1 showed higher activation energies than the absorber bandgap: E_a~1440 meV for B-1 and E_a~1435 meV for C-1. The very similar activation energy suggests that for both cells the additional recombination mechanism is due to the same effect. A possible explanation for a higher activation energy E_a is the occurrence of interface recombination, in presence of a large CBO between the CdS and CIGS interface. For cells A-1 and B-1 the fitted values of E_a don't agree with the absorber bandgap, notwithstanding the ideality factor in the range of 1.3-2. This shows SRH isn't the dominant recombination mechanism limiting the dark current.

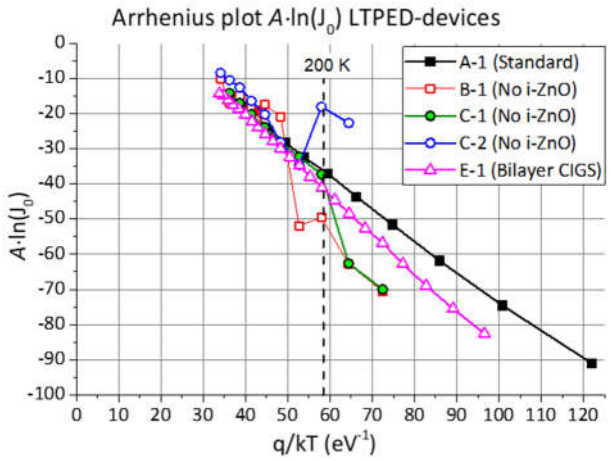


Figure 43 Arrhenius plots constructed using fitted values of the ideality factor A and saturation current density J_0 as $A \cdot \ln(J_0)$. The corresponding activation energy of the dominant recombination mechanism E_a was found from the slope of the curve.

For cell B-1 the dark IV-T characteristics were performed for higher bias in the range $T < 180$ K (see Figure 44). This made it possible to observe an additional increase in the forward current at higher bias, indicating the presence of a thermal barrier to charge carriers limiting the forward current for $T < 180$ K that required biases $V > 1.3$ V to be overcome.

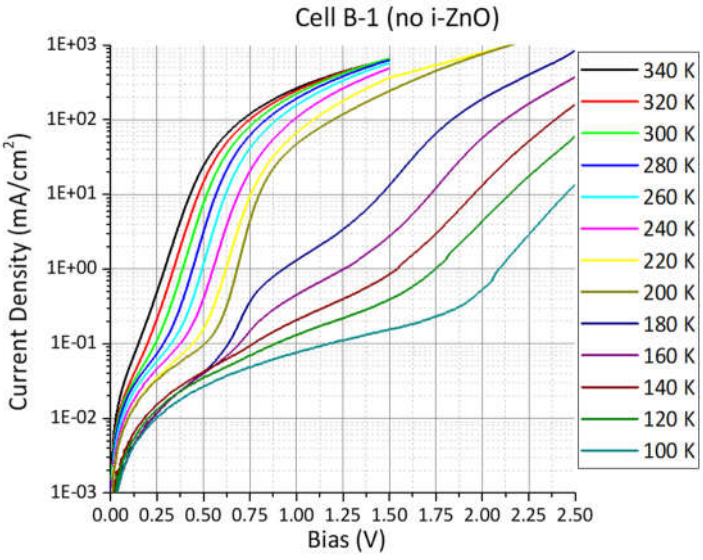


Figure 44 IV-T characteristics of cell B-1 (standard LTPED-device without i-ZnO, $\eta = 10.2\%$) where for biases up to 2.5 V a second barrier becomes observable at $T < 200$ K.

4.3.4 Summary and conclusions

A number of LTPED-devices with near to standard architecture was analysed using IV, EQE, AS, C-V, IV-T and V_{OC}-T measurements. The typical performance parameters were found to be relatively uniform between samples, with $\eta \sim$ 10-14%, $V_{OC} \sim$ 540-591 mV, $J_{SC} \sim$ 26-29 mA/cm^2 and FF~65-75%. Both R_S and R_{Sh} were found to depend on illumination. A strong reduction in R_S (by up to 47%) was observed for various cells, suggesting presence of a barrier to forward current in the dark. This could indicate presence of a photo-active barrier at the CdS/CIGS layer often suggested in literature [8] [122]. The R_{Sh} values were observed to either increase or decrease with Illumination, depending on the cell. A large decrease in R_{Sh} with illumination might indicate presence of photoconductive shunting paths while an increase in R_{Sh} with illumination isn't completely understood.

The devices were found to have highest EQE (70%-90%) in the 520-800 nm range. The limited EQE in the 350-500 nm (only 20-40%) was directly correlated to absorption in the CdS buffer layer, leading to a reduced EQE with increasing CdS-layer thickness. At increasing wavelength, the EQE was found to increase with decreasing GGI, due to the lower bandgap. For GGI of 20% the EQE was found to reach 65% up to 1050 nm.

In AS results the relative capacitance variations between high and low frequencies (calculated as C_∞/C_0) in the range of 56%-92% were found, indicating a high concentration of defects in all cells. Similar to what is often reported in literature the C-f profiles usually showed a more gradual variation in the high temperature/low frequency region ($T > 240$ K, $f < 100$ kHz, 'N2' step) and more 'sharp' variation in the low temperature/high frequency region ($T < 240$ K $f >$ 100 kHz, 'N1' step). The activation energy E_d (expressed in distance from the VBE) for the N1 step was found to vary significantly between cells, with $E_d \sim$ 31 meV observed for cell A-1 and $E_d \sim$ 320-400 meV for the other cells. The lower value of 31 meV is much lower than what is typically reported in literature for the N1 defect, while the values 320-400 meV are much higher and agree better with typical values reported for the N2 defect. For one cell (C-2) only a large step at lower frequencies was observed in the C-f curves at all temperatures, with the activation energy of the corresponding defect estimated as $E_d \sim$ 354 meV. This suggested a band of defect states with

similar activation energy as those in other cells, but more narrowly distributed throughout the bandgap. From the reported results no clear conclusions can be drawn on the type and origin of the defects giving rise to the observed steps, but they clearly demonstrate a large variation in the activation energies of the dominant defect states among LTPED devices.

In C-V profiling most cells were found to be completely depleted, indicating a charge carrier density $N \ll 10^{15}$ cm^{-3}. The three cells that didn't show a completely depleted absorber layer still had relatively low apparent free carrier densities, with $1.5 \cdot 10^{15}$ cm^{-3} $\leq N \leq$ $3.4 \cdot 10^{15}$ cm^{-3} corresponding to 0.5 μm $\leq w \leq$ 0.7 μm. These results were expected to be free of defect response, since the capacitance was observed to saturate high frequency and low temperature in each case. The low carrier densities were attributed to insufficient Na-doping, resulting from the difficulty of promoting Na-diffusion through the CIGS absorber layer at the low temperature of LTPED deposition.

In cells C-1 and E-1 both V_{OC} and dark current were found to be limited by SRH recombination in the bulk of the absorber. In cell A-1, both V_{OC} and dark current were found limited by a recombination mechanism with lower activation energy, with E_a ~890 meV and E_a~994 meV at V_{OC} under illumination, probably indicating interface recombination playing an important role in this cell. For cell B-1, from V_{OC}-T measurements E_a was estimated to be approximately equal to the absorber bandgap (E_a~1085 meV) suggesting bulk SRH-recombination limiting the V_{OC}. However, the dark current appeared to be limited by a recombination mechanism with E_a~1440 meV. This might well be related to the additional barrier to the dark forward current observed at lower temperatures for this cell. For cell C-2 the V_{OC}-T characteristics showed a dominant recombination mechanism with E_a~690 meV, again suggesting interface recombination, while in the dark current E_a~1440 meV was found also in this case. These high values of E_a in the IV-T characteristics and lower values of E_a in the V_{OC}-T characteristics might be explained by a high CBO at the CIGS/CdS interface forming a barrier to the forward current in the dark, which reduces under illumination. The results obtained for cell A-1 ($\eta = 12\%$) with $E_a < E_G$ both from V_{OC}-T and IV-T measurements suggest that reasonable efficiencies can be obtained in cells even in presence of interface recombination.

5 ODC-phase CIGS in LTPED-devices

INTRODUCTION

As already discussed in Chapter 2, various investigations of CIGS/CdS based Thin Film Solar Cells (TFSC's) showed the active junction is usually formed between the P-type CIGS absorber and a thin layer of the N-type Ordered Defect Compound (ODC) phase of CIGS located close to the CIGS/CdS interface. This contradicts the original picture of a heterojunction formed between P-type CIGS and N-type CdS [70] [82]. As discussed in section 2.3, the ODC-phase corresponds to off-stoichiometric compositions such as $Cu(In_{1-x}Ga_x)_3Se_5$, and a slight change in the crystal structure from the standard chalcopyrite to the so-called defect-chalcopyrite. For the typical composition of Ga/(Ga+In) (GGI) ~0.3, the ODC-phase has been observed to have a slightly higher bandgap than CIGS: ~1.45 eV, and very little lattice mismatch with the P-type CIGS absorber layer. This allows the formation of a homojunction with smoother interface than a heterojunction between the CIGS-absorber and CdS buffer, leading to a low contribution of interface recombination and improved device performance, which was also confirmed experimentally [1, 2, 3, 4]. The thin ODC-phase layer is thought to be formed during the standard Chemical Bath Deposition (CBD) of CdS, but a type-inversion can also be achieved by special post-deposition treatments of the CIGS absorber. The observed ODC-layer thicknesses were experimentally determined to be in the range of ~10-50 nm.

The results presented In the current chapter were obtained using samples in which it was attempted to deposit a thin layer of ODC-phase material (ODC-layer) using LTPED. The attempt of the ODC-layer deposition was performed directly after the deposition of the standard P-type absorber, by lowering the acceleration voltage, as will be explained in detail below. Using this approach, samples were prepared to have an ODC-layer with thicknesses ranging from 0 to 800 nm. Two of the studied devices had fluorine doped tin-oxide doped (FTO) substrates, and five of the devices had Molybdenum (Mo) substrates. In addition to standard IV measurements and EQE

measurements the same electrical characterization techniques discussed in Chapter 4 were used, i.e. C-V, AS, IV-T and V_{OC}-T measurements.

In section 5.1 a more detailed description of the approach to deposition of the ODC-phase by LTPED is given. The results are presented and discussed in section 5.3 (CIGS/FTO samples) and section 5.4 (CIGS/Mo samples). In section 5.5 a summary of the results and conclusions is given.

5.1 EXPERIMENTAL APPROACH: LTPED DEPOSITION OF ODC-PHASE CIGS

The attempts to incorporate an ODC-layer in LTPED devices were motivated by the apparent improvement of some of the electrical characteristics in sample 'F-1' (see below) in which presence of a thick ODC-layer could be observed in Raman spectroscopy (Figure 1). For sample F-1 the deposition of the ODC-layer was an unintended result of a much longer deposition than usual. The prolonged heating of the target was thought to have caused a change of phase from chalcopyrite to ODC-phase at the ablation depth of the target, resulting in ablation of ODC-phase material from target directly onto the substrate during part of the deposition.

For the intentional ODC-layer deposition a slightly different approach was used. Instead of increasing the deposition time, the acceleration voltage was lowered from the standard 16 kV to 12 kV, leading to most material being transferred from the target by evaporation (see Chapter 4). In earlier investigations incongruent evaporation was observed to result in deposition of the Cu-poor ODC-phase [1]. Following this approach, six additional samples were prepared with the ODC-layer deposited directly onto the CIGS absorber. By varying the number of pulses at 12 kV samples with different expected ODC-layer thicknesses were deposited, as shown in

Table 8.

Sample F-1 mentioned above was deposited onto a FTO substrate. Since the ODC-layer in sample F-1 was unintentionally deposited its thickness was unknown. However, the strong 'A1-ODC-mode' at ~150 cm^{-1} observed in the Raman-spectrum shown in Figure 45 indicates a higher thickness than observed for other samples. The sample F-2 was intentionally prepared with ODC-layer, and also deposited onto an FTO substrate to have a direct comparison to sample F-1. Samples M-1 to M-5 followed the standard LTPED architecture with Mo-substrate and were intended for a more detailed investigation of the role of the thickness of the ODC-layer on device performance. The variation in the GGI between sample F-1 (GGI = 0.3) and the other samples (GGI = 0.2) was due to problems experienced with the CIGS target with GGI = 0.3. In two of the samples (F-1 and M-5) the usual annealing procedure (20-minutes at 250°C directly after deposition) was skipped. For sample F-1 this was done to compensate for the longer time the sample had already been kept at 250°C due to the long deposition. For sample M-5 this was done to test whether the post-deposition annealing treatment had a significant influence on the formation of a junction in devices with intentionally deposited ODC-layers. The experimental results for the samples on FTO substrates (F-1 and F-2) and with standard LTPED architecture (M-1 to M-5) are presented separately in section 5.3 and section 5.4 respectively.

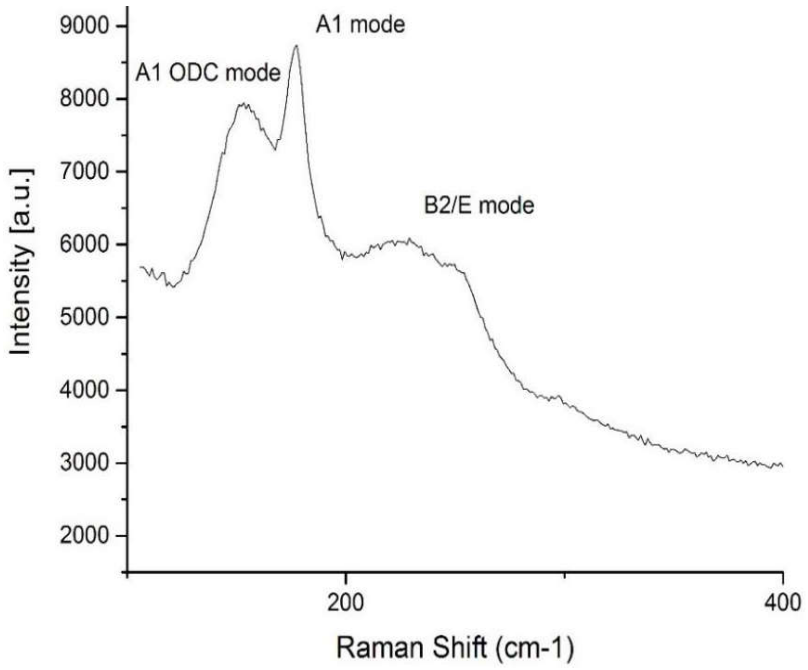


Figure 45 Raman spectrum obtained for sample F-1. The broad peak at ~150 cm^{-1} indicates presence of a significant amount of the ODC-phase of CIGS.

Table 8 Properties of the LTPED-devices prepared with intentionally deposited layer of ODC-phase material. 'Pulses at 12 kV' indicates the number of pulses at this acceleration voltages used during the LTPED preparation, which was used to estimate the indicated 'ODC-layer' thickness. Since deposition of the ODC-layer was unintentional in sample F-1, the thickness is unknown.

Sample	GGI	Substrate	Pulses at 12 kV (x 1000)	ODC-layer (nm)	Post deposition annealing (min) at 250°C
F-1	0.3	FTO	0	Unknown	0
F-2	0.2	FTO	4	160	20
M-1	0.2	Mo	0	0	20
M-2	0.2	Mo	1	16	20
M-3	0.2	Mo	2.5	40	20
M-4	0.2	Mo	50	800	20
M-5	0.2	Mo	0.6	10	0

5.2 CONTRIBUTION OF ODC-LAYER TO MEASURED CAPACITANCE

Although the doping level of the ODC-phase material couldn't de experimentally determined for the samples shown in

Table 8, it was expected to be much higher than that of the P-type CIGS absorber (i.e. $N_D \gg N_A$) leading to nearly the entire depletion layer lying in the P-type material, as for a CdS/CIGS heterostructure. The concentration of interfacial states between the ODC-layer and P-type CIGS layer was expected to be negligible. Following these assumptions no significant influence from the ODC-layer on capacitance measurements was expected. Nevertheless, without proof that $N_D \gg N_A$ holds, it is useful to consider the effects of the ODC-layer on the measured capacitance in the extreme case where $N_D \sim N_A$, i.e. where the doping level of the ODC-layer would be comparable to that of the absorber. From equation 1.6 in Chapter 0, this would result in

$$w_N \sim w_P = \sqrt{\frac{\epsilon(V_{bi} - V)(N_A + N_D)}{2q(N_A N_D)}} \sim \sqrt{\frac{\epsilon(V_{bi} - V)}{qN}} \qquad 5.1$$

where w_N and w_P are the depletion layer widths on the N- and P-side and $N = N_D = N_A$. Hence the variation in the depletion layer width with external bias would also be comparable in this case, but with w_N in equation 5.1 limited by the total thickness of the ODC-layer. Since in typical devices the depletion of the absorber layer is ~400 nm, in samples with thin ODC-layers ($\leq$ 40 nm) a fully depleted ODC-layer would contribute $\leq$ 10% to the total capacitance. For the thicker ODC-layers of sample F-2 (160 nm), sample M-4 (800 nm) and sample F-1 (unknown), a fully depleted ODC-layer would correspond to ~1/3-1/2 of the total measured depletion layer width. As a result, in AS-spectroscopy majority carrier traps in both the ODC-layer and CIGS layer could contribute to the measured capacitance, while in C-V profiling following the standard Mott-Schottky approach (in which $N_D \gg N_A$ is assumed) would lead to an overestimation of the depletion in the CIGS absorber. For measured capacitance C the calculated depletion layer width $w' = \frac{\epsilon A_J}{C}$ would correspond to $w' = w_N + w_P \sim 2\, w_P$. Since a completely depleted absorber layer would correspond to constant depletion layer width with bias, while a partially depleted absorber would correspond to a depletion layer width increasing with reverse bias, the two cases might still be distinguished.

5.3 SAMPLES CIGS/FTO

In the current section the results obtained on the samples F-1 and F-2 with CIGS/FTO architecture are presented. The investigated samples showed significant non-uniformity and low performance, as clear from

Table 9 and Figure 46 and Figure 47. Efficiencies of $\eta \sim$ 4-5% were measured on sample F-1, and $\eta \sim$ 1-2% on sample F-2. The IV-characteristics measured for the best performing cells on each sample are shown in Figure 46 and Figure 47, together with the characteristics measured on a higher efficiency sample 'Ref' with CIGS/FTO architecture but without an intentionally deposited ODC-layer.

Table 9 Measured performance parameters for samples F-1 (CIGS/FTO, ODC-layer with unknown thickness), F-2 (CIGS/FTO ~ 160 nm ODC-layer) and Ref (standard CIGS/FTO samples) as measured in the dark and in STC conditions (AM1.5G, 1 sun, 25°C sample temperature). Note that the GGI differs between cells: ~30% for F-1, ~20% for F-2 and ~50% for Ref.

	Cell	F-1A	F-1B	F-1C	F-2A	F-2B	Ref
STC	V_{OC}	567.0	586.5	558.5	514.1	478.3	635.9
	J_{SC}	15.3	13.5	12.6	9.1	16.6	29.4
	η (%)	4.7	4.4	3.9	1.2	1.9	14.0
	FF (%)	54.2	55.2	55.5	25.3	23.8	74.5
	R_S ($\Omega \cdot cm^2$)	3	3	8	10	22	1.7
	R_{Sh} ($\Omega \cdot cm^2$)	**170**	**230**	**240**	**30**	**30**	**385**
Dark	R_S ($\Omega \cdot cm^2$)	5	4	21	10	29	1.7
	R_{Sh} ($\Omega \cdot cm^2$)	800	710	1000	1920	560	840
	ΔR_S (%)	-40%	-25%	-62%	0%	-24%	0%
	ΔR_{Sh} (%)	-76%	-77%	-75%	-98%	-95%	-54%

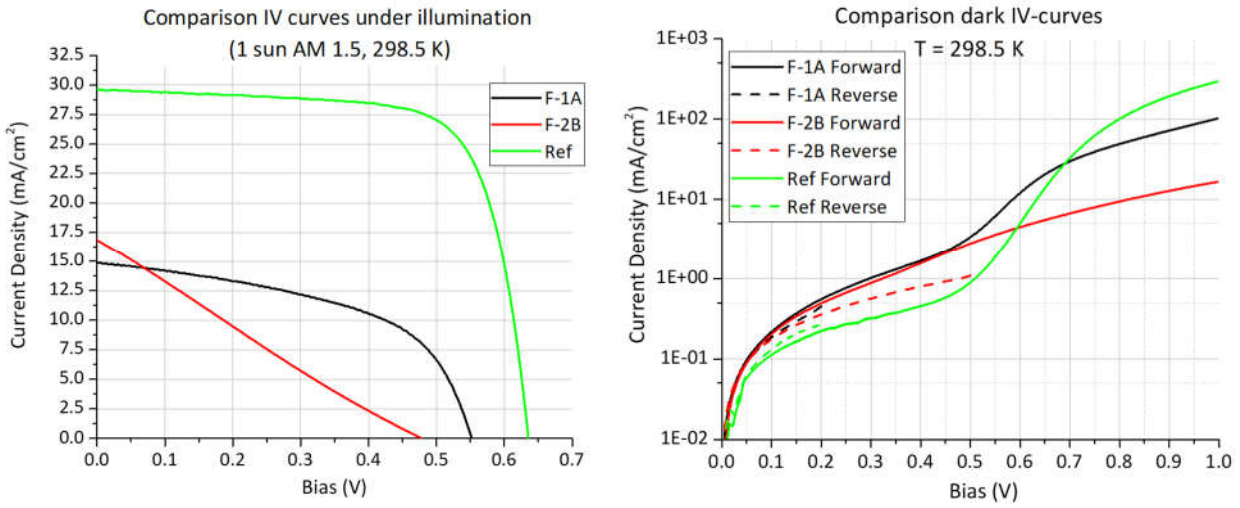


Figure 46 Comparison of the illuminated (left) and dark (right) IV-curves of cells F-1A (CIGS/FTO with unknown thickness of ODC-layer, black curves), F-2B (CIGS/FTO, ~160 nm ODC-layer, red) and 'Ref'(standard CIGS/FTO)

The inhomogeneity observed in samples F-1 and F-2 appears to be comparable to that observed in standard LTPED devices, and hence wouldn't appear to be attributable to presence of an ODC-

layer. However, comparison of the performance of both samples with respect to that observed in LTPED devices with the CIGS/FTO architecture but without the ODC-layer (see Figure 46) suggests a negative effect of the ODC-layer. Both samples have a much lower efficiency, mainly due to low FF's (24-26% on F-2, 54-56% on F-1 and ~75% on Ref) and low J_{SC}'s (9-17 mA/cm^2 on F-2, ~13-15 mA/cm^2 on F-1 and ~30 mA/cm^2 on Ref). The most important reason for this large FF-loss appears to be the very low R_{Sh} under illuminated conditions. The low J_{SC}'s are confirmed in the low EQE of both samples (see Figure 48 and text below).

In addition to the noticeably low performance, the R_S and R_{Sh} are found to show more illumination dependence than typically observed in other LTPED devices, as is clear from Figure 47. In the dark the R_{Sh} values on these cells are found to lie the range of 710-1920 $\Omega \cdot cm^2$, while under illumination a reduction in the R_{Sh} values is observed (i.e. with respect to the values in the dark) of up to 80% on sample F-1 and by up to nearly 100% on sample F-2. The values of R_S in the dark are found in the range of ~4-29 $\Omega \cdot cm^2$, while under illumination it reduces by up to 62% on sample F-1, and by 24% on sample F-2. In contrast, on sample Ref illumination caused a 54% reduction in R_{Sh} and no change in R_S.

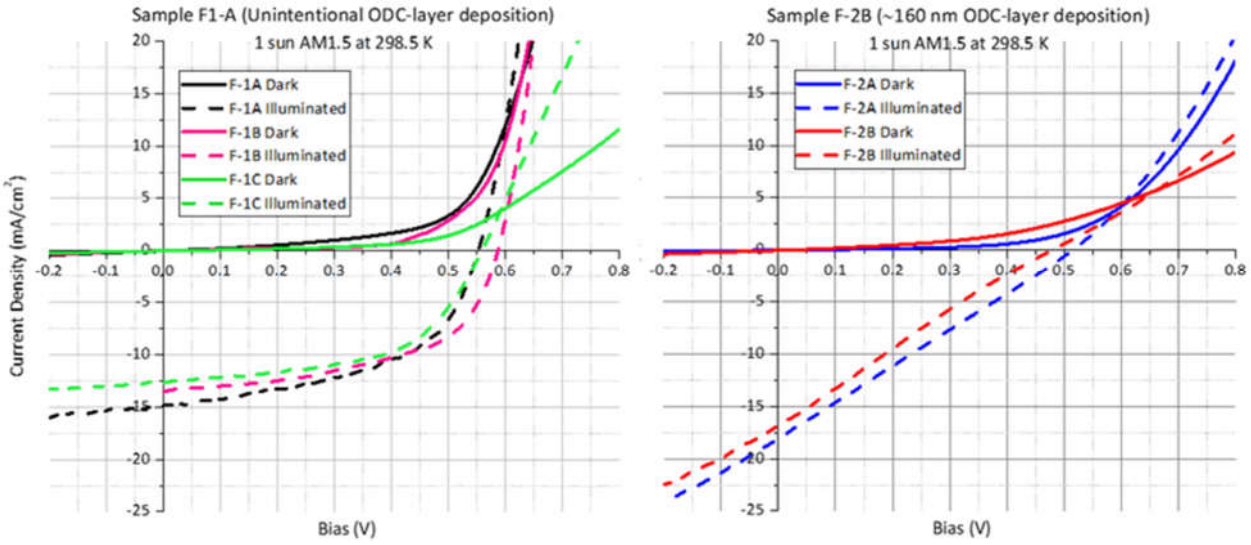


Figure 47 Dark and illuminated IV-curves for sample F-1 (left) and sample F-2 (right)

These results suggest the observed variation in R_S and R_{Sh} at the application of illumination are correlated to the presence of a thick ODC-layer. This could be explained by significant

photoconductivity in the ODC-layer. In a model described in [8] the dark current in CIGS-based devices is limited due to a high concentration of traps in a thin ODC-layer and an unfavourable CBO between this ODC-layer and CdS layer. Upon illumination photogenerated holes are suggested to neutralize traps and cause a reduction in an electron barrier. Standard CIGS by LTPED. Since in samples F-1 and F-2 the ODC-layer was made much thicker ($>$ 100 nm) than would be the case in usual CIGS-based devices (i.e. including the ones in the model described in [8], where a thickness for the ODC-layer of $\sim$15 nm was assumed) the proposed effects of photoconductivity in the ODC-layer could explain the much larger variations observed in the current results than those for standard LTPED devices or other typical CIGS-based devices. The increased R_{Sh} values in the dark might in this case be explained by increased coverage of shunting paths in the CIGS absorber due to the additional ODC-layer. At illumination the increased conductivity in the ODC-layer would then lead to photoconductive shunting paths, hence explaining the strong drop in R_{Sh} values.

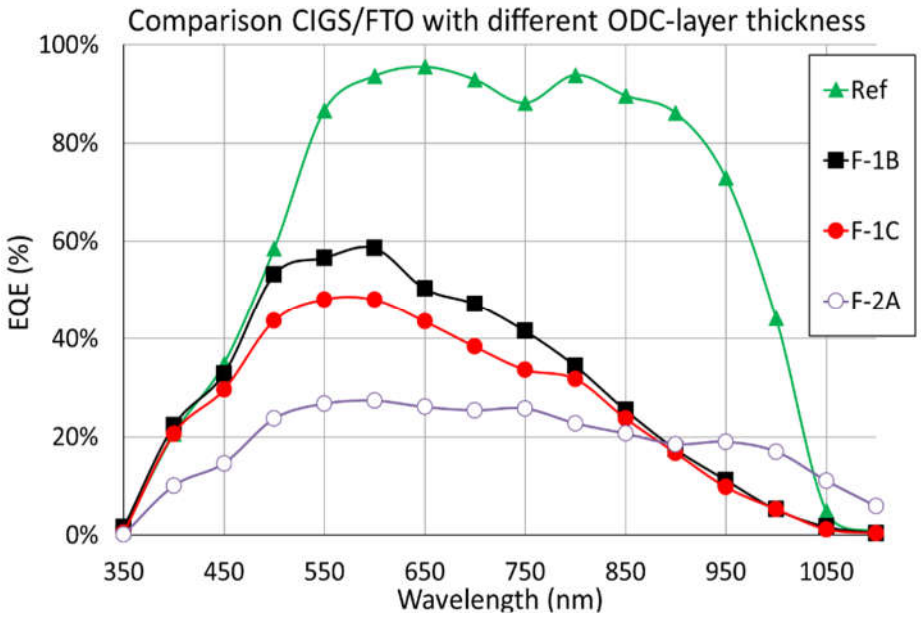


Figure 48 Comparison EQE measurements on different CIGS/FTO samples Ref (no ODC-layer), F-1 (thick ODC-layer, unknown thickness) and F-2 (ODC-layer, ~160 nm thick)

The EQE measured for two cells on sample F-1 and for one cell on sample F-2 are found to be much lower than in the reference sample with CIGS/FTO architecture without ODC-layer, as shown in Figure 48 above. The EQE's of the three cells containing the ODC-layer are found to be

much lower in the entire wavelength region $\lambda > 550$ nm, indicating either a much lower photogeneration or collection of photogenerated charge carriers in these samples throughout the entire absorber layer. The lower EQE for shorter wavelengths, corresponding to light closer to the buffer layer (i.e. $\lambda < 550$ nm) might be related to recombination-losses due to a high concentration of defects, either in the ODC-layer or at the CdS/ODC or ODC/CIGS interfaces. However, the most significant losses in conversion efficiency are observed for wavelengths penetrating deeper into the absorber (i.e. $\lambda > 750$ nm). This suggests efficiency losses due to effects in the bulk of the absorber or at the interface with the FTO back-contact. Such effects wouldn't be expected to be correlated to the presence of an ODC-layer at the surface of the absorber, unless significant diffusion would be assumed to have taken place between the deposited ODC-layer and the absorber bulk during or after deposition. A lower quality of the CIGS/FTO interface for samples F-1 and F-2 than for sample Ref on the other hand could be explained by insufficient Na-doping in both samples.

To obtain an indication of the defect response in samples F-1 and F-2, AS measurements were performed on three cells (F-1B, F-2A and F-2B) with results shown in Figure 50-Figure 51. The large differences between the AS-spectra obtained on the cells from the same sample (F-2A and F-2B) are an indication that effects related to sample inhomogeneity likely overshadow possible differences related to different ODC-layer thicknesses between sample F-1 and F-2. In the C-f spectra obtained for cell F-2B a large reduction in capacitance was observed at high frequencies ($f > 100$ kHz) with an inflection point apparently independent of temperature. This was considered to be an artefact due to series resistance effects [111]. Also the step observed in the spectra for cell F-1B for $T < 200$ K and $f > 200$ kHz was expected to be due to artefacts.

The C-f profiles obtained for cell F-1B at temperatures $T > 110$ K (Figure 49) are quite similar to the typical AS-spectra in relatively good efficiency LTPED-devices. Similar to the observations made in Chapter 4 a gradual reduction in capacitance occurs in the lower frequency range (1 kHz $\leq f \leq 100$ kHz at 300 K) corresponding to the typically reported 'N2' step, and a clearer step is observed for $f > 100$ kHz corresponding to the typically reported 'N1' step (see Chapter 3). For cell F-1B, the difference in the step size would reflect a higher concentration of N1 defects than

N2 defects. By constructing an Arrhenius plot from the peak positions in the $\left[-\omega \cdot \frac{\mathrm{d}C}{\mathrm{df}}\right]$ profiles for cell F-1B (see Figure 49 and Figure 51) the centre of the N1 defect distribution within the absorber bandgap could be estimated. The changing slope in the Arrhenius plot indicates a slight temperature dependence, with $\mathrm{E_d} \sim 111.2$ meV for $\mathrm{T} < 230$ K and $\mathrm{E_d} \sim 169.5$ meV for $\mathrm{T} > 230$ K. Both values agree well with the energies typically reported in literature for the N1 defect step.

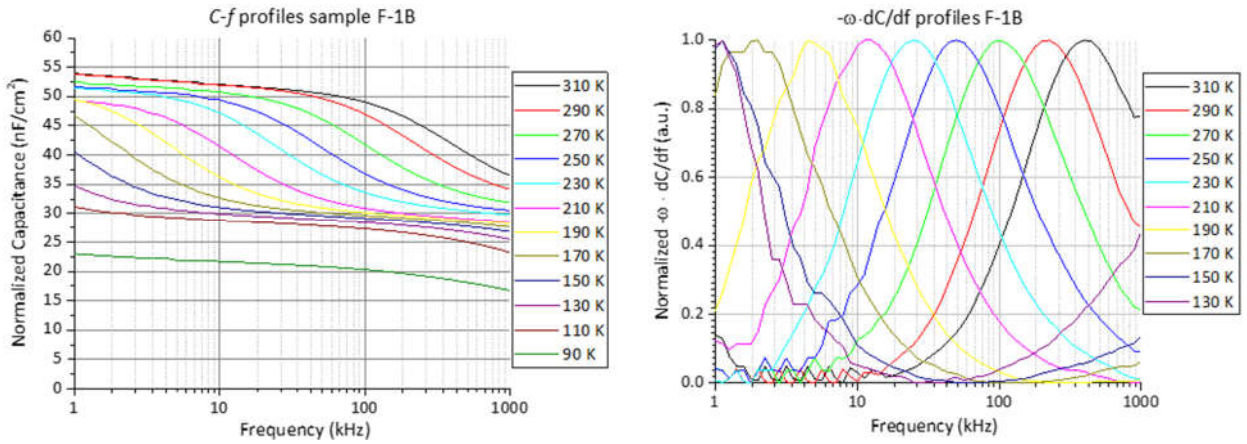


Figure 49 AS-spectra for cell F-1B. Left: C-f profiles as function of temperature. The reduction in the temperature region 100 kHz $\leq f \leq$ 1 MHz is considered to be an artefact due to series resistance or inductance. Right: Corresponding normalized$[-\omega \cdot \frac{dC}{df}]$ profiles.

For cell F-2A (see the top graphs in Figure 50) a large capacitance step is observed at low frequencies ($f < 10$ kHz) that shifts relatively little within the entire investigated temperature range (120 K $\leq \mathrm{T} \leq$ 300 K). As reported in [123], such behaviour might be an indication of response from defects close to or at the CIGS/CdS interface. The low temperature sensitivity of the C-f curves caused a higher uncertainty in the peak positions in the $\left[-\omega \cdot \frac{\mathrm{d}C}{\mathrm{df}}\right]$ profiles. Hence, the value that was obtained for the centre of the corresponding defect distribution of $\mathrm{E_d}$~20-82 meV is considered as a very rough indication.

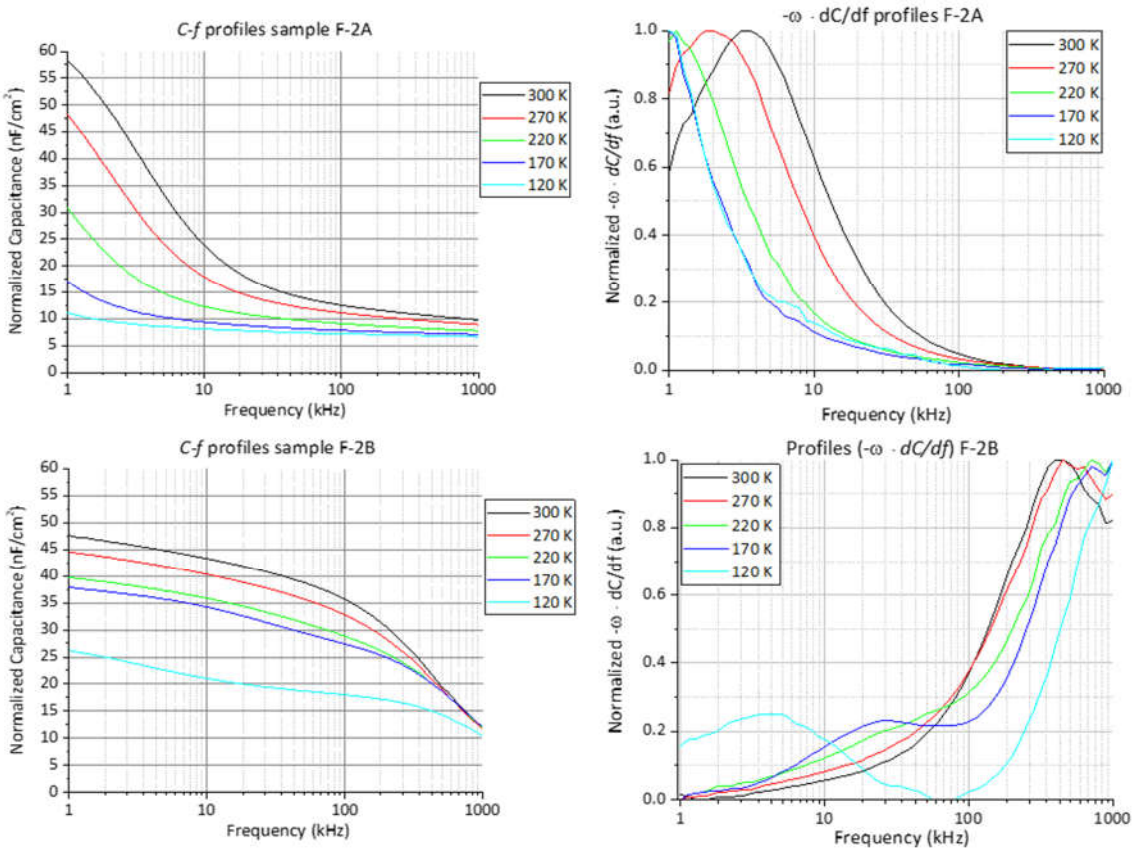


Figure 50 AS-spectra for cells F-2A (top row) and F-2B (bottom row). Left: C-f profiles as function of temperature. For sample F-2B, the large reduction in capacitance in the region 100 kHz $\leq f \leq$ 1 MHz is considered to be an artefact due to series resistance or inductance. Right: Corresponding normalized$[-\omega \cdot \frac{dC}{df}]$ profiles.

The characteristics for cell F-2B were strongly influenced by artefacts due to inductance at higher frequencies, making it difficult to distinguish the actual defect contribution to the C-f profiles. However, the large step at lower frequencies appeared to be most similar to the N2 step.

The similarity between the AS-spectra observed for cell F-1B and standard LTPED devices (see Chapter 4) suggests the AS-spectra obtained on this cell are free of influences from the ODC-layer, notwithstanding the very high thickness expected. The presence of interfacial states suggested in cell F-2A above might be related to interfacial states at the CdS/ODC-layers, as proposed in the model given in [8] which would also explain the observed illumination dependence on sample F-2. However, the large differences observed between cell F-1B and F-2B remain unexplained in this case, as both samples are expected to have an ODC-layer with

significant thickness. Possibly, the difference in the deposition approach between F-1 and F-2 (i.e. gradual change of phase of ablated material for sample F-1 and sudden change from ablation to evaporation for sample F-2 as explained in 5.1) caused a more defected ODC/CIGS interface for sample F-2 than for sample F-1.

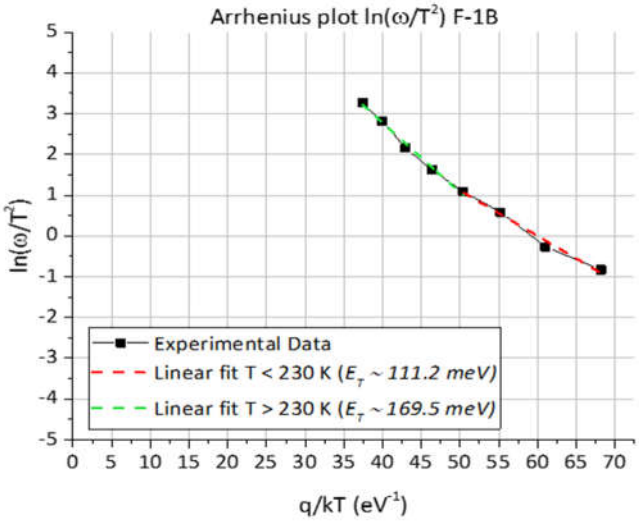
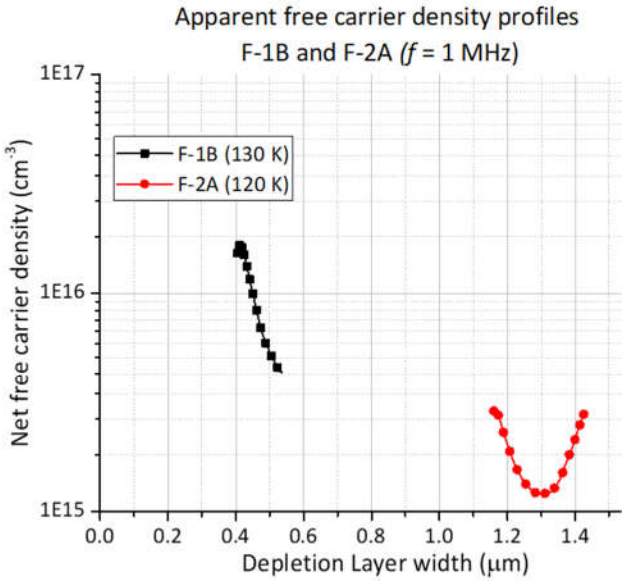


Figure 51 Arrhenius plot obtained by analysis of the temperature dependence of the $\left[-\omega \cdot \frac{dC}{df}\right]$ profiles of sample F-1B. The slope of the characteristic appears to vary with temperature, giving an energy E_d for the center of the defect distribution of E_d ~ 111.2 meV for $T < 230$ K and $E_d \sim 169.5$ meV for $T > 230$ K

For cells F-1B and F-2A the apparent free carrier density (N-w) profiles, shown in Figure 52, were determined by performing C-V measurements performed at 1 MHz oscillation frequency and ~120-130 K sample temperature. Under these measurement conditions the AS-spectra of both samples showed a saturation in the capacitance, which was interpreted as absence of defect contributions to the measured capacitance values. Hence, the extracted apparent net free carrier density profiles and depletion layer widths were expected to be accurate.



Cell	η (%)	w (µm)	N (10^{15} cm^{-3})
F-1B	4.4	0.5	5.4
F-2A	1.2	1.3	1.2

Figure 52 Calculated apparent free carrier density profiles obtained by C-V profiling (using a AC-signal with 25 mV amplitude and 1 MHz oscillation frequency) for cell F-1B (black squares, measured at 130 K) and cell F-2A (red circles, measured at 120 K) in the bias range -0.3 V $\leq$ V $\leq$ +0.3 V. Depletion layer width w and net free carrier density N were derived from the minima in the profiles.

The difference in shape between the two profiles is due to the difference in bias region that was used for cells F-1B and F-2A. For sample F-1 only a relatively low reverse bias (i.e. low extension of the depletion layer width) was investigated, to prevent damage to the cell. Sample F-2A was expected to support higher reverse biases. This allowed observation of the typical 'U'-shape for cell F-2A, while in cell F-1B most the continuous decrease most likely corresponds to the left-most edge of the similar U-shape, that would be expected to increase again for higher reverse bias. The apparent free carrier densities were estimated from the minima of the profiles, and found to be $5.4 \cdot 10^{15}$ cm^{-3} for cell F-1B and $1.2 \cdot 10^{15}$ cm^{-3} F-2A, with corresponding depletion layer widths of $\sim$ 0.5 µm and 1.3 µm respectively. These results indicate a very low doping in cell F-2A, while the values for cell F-1B appear to be close to the typical values found in standard LTPED devices with reasonable efficiency (see Chapter 4).

The dominant recombination mechanisms were determined for in cells F-1B and F-2B using V_{OC}-T (Figure 53) and IV-T measurements (Figure 54). In the V_{OC}-T characteristics, a linear fit of the high temperature range ($T > 220$ K) gives an intercept with the vertical axis somewhat below the expected bandgap for both cells: ~ 957 meV for F-1B (E_G~ 1.2 eV) and ~ 916 meV for F-2B (E_G ~ 1.1 eV). This indicates a significant contribution from other recombination mechanisms than Shockley-Read-Hall (SRH) recombination in the bulk in limiting the V_{OC}. A likely contribution of alternative recombination mechanisms would be interface recombination, suggesting the deposition of ODC-phase material resulted in a higher concentration of interfacial defects at either the CdS/ODC interface, or the ODC/CIGS interface.

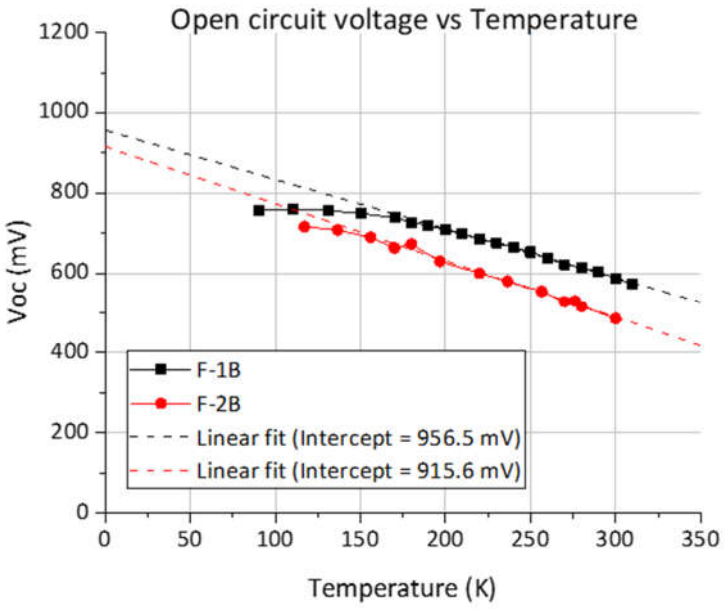


Figure 53 The V_{OC}-T characteristics obtained on cells F-1B and F-2B. The intercept taken from the linear fit of the high-temperature ($T>200$ K) region shows quite low values for both devices: 957 meV for cell F-1B and 916 meV for cell F-2B, indicating effects of interface recombination

The IV-T characteristics of F-1B and F-2B reflect the large difference in performance between the two cells. For cell F-1B a much lower ideality factor A is obtained at room temperature (~1.5 as opposed to A slightly above 2 for F-2B) and a more clearly distinguishable region of ideal diode behaviour is observed. The characteristics of cell F-1B also show a much larger temperature dependence, as is also clear the temperature dependence of the ideality factors plotted in Figure 54 (C). From the values of A and saturation current density J_0 fitted from the IV-curves after

correction according to [29], the Arrhenius plots of $A\ln(J_0)$ were constructed, shown in Figure 54 (D) below. The Arrhenius plot for cell F-2B showed a straight line for the entire temperature range $120 \leq T \leq 320$ K, with the slope giving an estimation of the activation energy of the dominant recombination mechanism of $E_a \sim$ 950-983 meV. For cell F-1B the Arrhenius plot showed a change of slope for $T < 200$ K, with the slope of the high temperature region indicating an activation energy of $E_a \sim 1175$ for the dominant recombination mechanism.

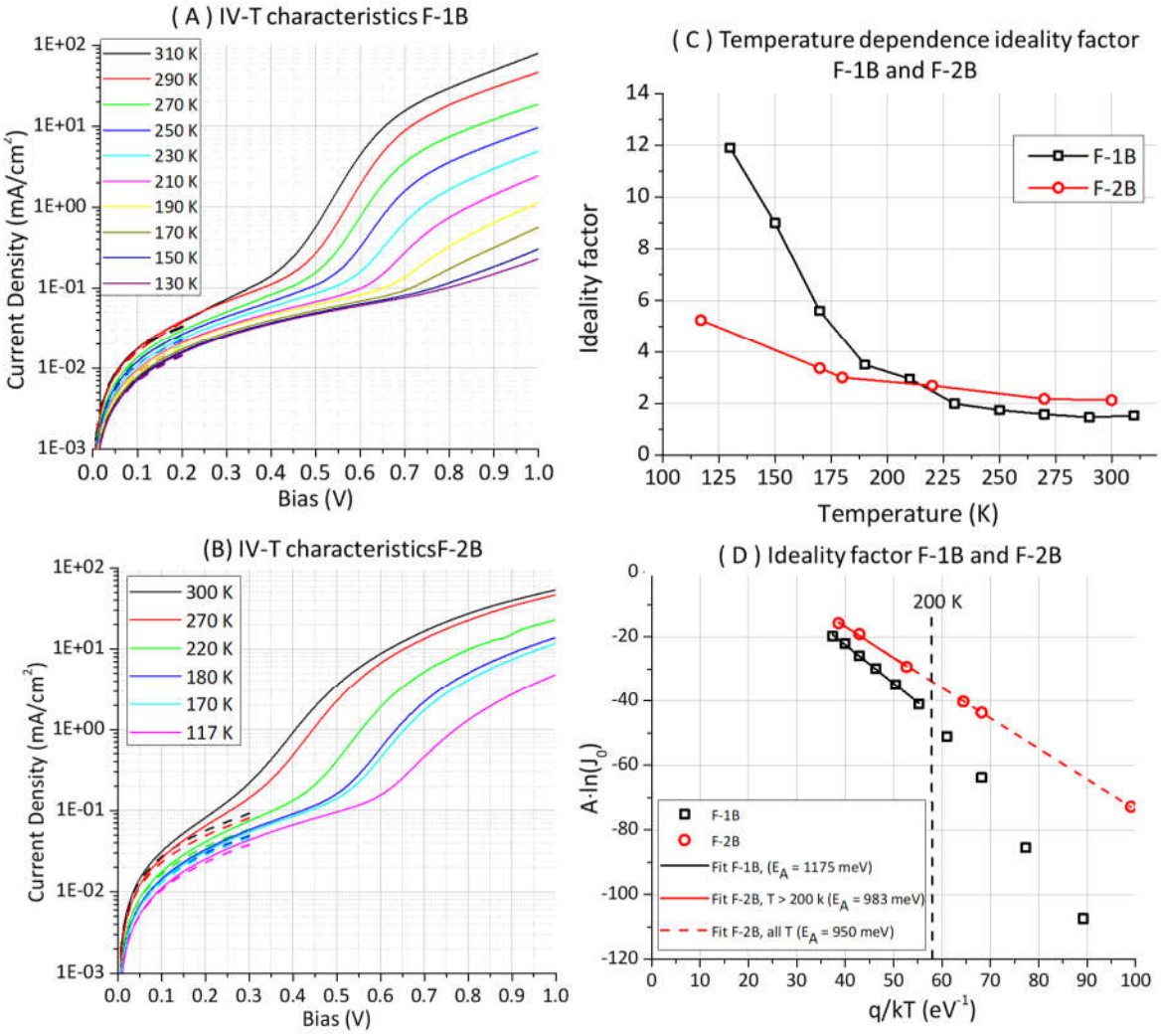


Figure 54 (A) and (B): IV-T characteristics cell F-1B (A) and F-2B (B), (C): Ideality factor of both cells as function of temperature (D): Arrhenius plots A ·ln(J0) Fits of ideality factor and J_0 were performed following the procedure reported in [29].

The value E_a slightly below the expected bandgap for cell F-2B suggests other recombination mechanisms than SRH play an important role in limiting recombination current. Again, a contribution from interface recombination would appear to be reasonable. For cell F-1B on the other hand, the value of E_a very near the expected bandgap suggests that under these dark conditions SRH recombination is the limiting factor in the dark current. Hence, for both cells the V_{OC} appears to suffer from interface recombination, considering the intercept slightly below the expected bandgap value. In the dark, the recombination current of cell F-1B appears to be limited by SRH recombination for normal operating temperatures while alternative recombination mechanisms (most likely tunnelling enhanced recombination) become more important for $T <$ 200 K. For cell F-2B the dark recombination current is appears to be limited by other recombination mechanisms than SRH recombination in the bulk at all temperatures. These results strongly suggests deposition of the ODC-layer has resulted in an increased number of interfacial defects. In particular in the sample F-2 with intentionally deposited ODC-layer interface recombination appears to play an important role both under illumination and in the dark.

5.4 SAMPLES CIGS/MO: VARIATION OF ODC-PHASE THICKNESS

In this section results are presented from the investigation of the samples with intentionally deposited ODC-layer having standard CIGS/Mo architecture (thicknesses $0 \leq d \leq 800$ nm, see

Table 8). To test for presence of ODC-phase material, micro-Raman spectroscopy was performed on one cell from each sample. The resulting spectra are shown in Figure 55. The shoulder at ~150 cm^{-1} Raman shift indicating presence of the ODC-phase was only observable in the sample with highest expected ODC-layer thickness of 800 nm (M-4). Since the depth-resolution of the micro-Raman technique is only ~100 nm, these results only confirm the presence of ODC-phase in sample M-4, not the absence of the ODC-phase in the other samples. No further investigations have been performed identify presence of an ODC-layer, as the observation of the clear Raman peaks in samples F-1 and M-4 and results from earlier investigations [114] [1] were considered as sufficient evidence of the evaporation phase corresponded to the intended ODC-phase.

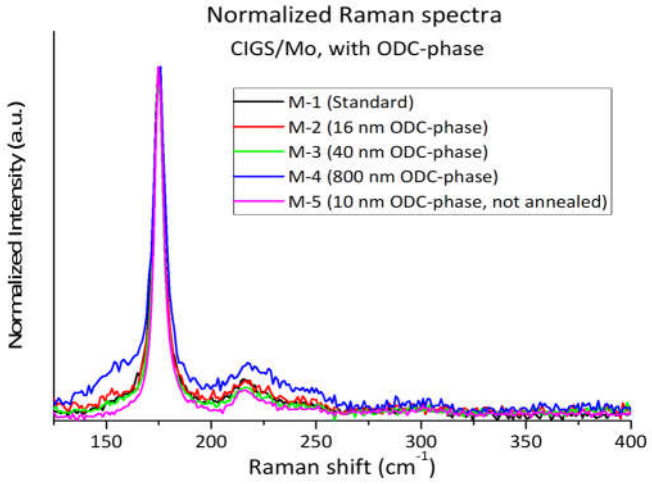


Figure 55 Raman spectra obtained from a representative cell on each of the samples M-1 to M-5. The ODC-phase mode (~150 cm-1) was only detectable on sample M-4 with expected 800 nm ODC-layer (blue line).

The results of IV-and EQE measurements performed on one representative cells on each sample are shown in Figure 56. The average performance parameters of the five best cells on each sample are reported in

Table 10.

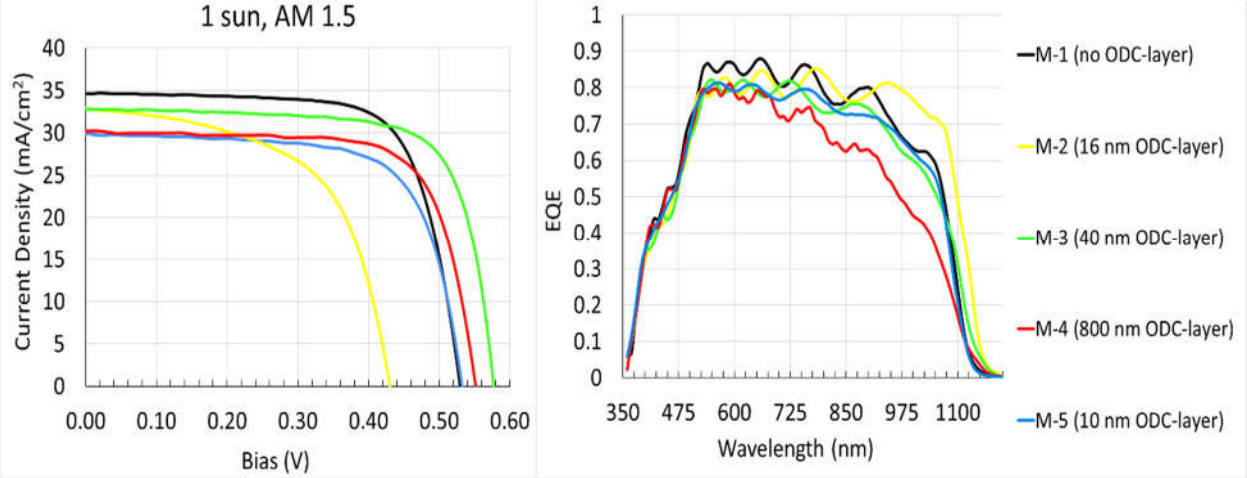


Figure 56 Left: IV-characteristics measured at STC (AM1.5G at 1 sun, 25°C sample temperature). Right: EQE of best cell from each of the samples M-1 to M-5. All samples had the standard LTPED architecture presented in Chapter 4. All samples were annealed for 20 minutes at 250°C after the CIGS deposition with exception of M-5, which wasn't annealed.

Table 10 Properties and average performance parameters of the 5 best cells of CIGS/Mo samples with varying ODC-layer thickness. All samples were prepared with GGI = 0.2. All samples were annealed for 20 minutes at 250°C after the CIGS deposition with exception of M-5, which wasn't annealed.

		M-1	M-2	M-3	M-4	M-5
Pulses at 12 kV (x 1000)		0	1	2.5	50	0.6
ODC-layer (nm)		0	16	40	800	10
Average performance parameters from 5 best cells						
STC	**V_{OC}**	531.9	411.0	540.8	546.8	511.1
	J_{SC}	32.1	30.1	33.0	29.6	31.3
	η (%)	12.3	7.3	12.3	11.6	10.6
	FF (%)	72.1	59.0	69.4	71.3	66.7
	R_S ($\Omega \cdot cm^2$)	0.5	0.7	0.9	0.9	0.5
	R_{Sh} ($\Omega \cdot cm^2$)	**660**	**160**	**430**	**660**	**390**
Dark	**R_S ($\Omega \cdot cm^2$)**	0.6	0.8	1.2	1.2	0.6
	R_{Sh} ($\Omega \cdot cm^2$)	1900	2330	6780	12000	2310
	ΔR_S (%)	-17%	-12.5%	-25%	-25%	-17%
	ΔR_{Sh} (%)	-65%	-93%	-94%	-95%	-83%

All samples show a high amount of uniformity. Nevertheless, some rough trends become distinguishable from the comparison of the averaged performance parameters.

Sample M2, expected to have an ODC-layer thickness of ~16 nm, shows much lower average efficiency than the other samples, with $\eta \sim$ 7.3% as opposed to $\eta \sim$ 10.6-12.3%. The lower efficiency in sample M-2 appears to be mainly attributable to a lower V_{OC}, (~411 mV for M-2, as opposed to 511-547 mV for the other samples) and lower R_{Sh} under illumination (~160 $\Omega \cdot cm^2$ in contrast to the 430-660 $\Omega \cdot cm^2$ for the other samples). The lower R_{Sh} results in a slightly lower FF: 59.0% on sample M-2 as opposed to the 66.7-72.1% on the other samples. From the current results these effects can't be attributed to the presence of the thin ODC-layer in sample M-2, but might be related to other differences between the devices due to some issues in reproducibility in the LTPED preparation approach.

The performance parameters which do show variations that appear to be correlated to ODC-layer thickness, are the R_S and R_{Sh} obtained from the IV -curves measured in STC and dark conditions. The R_S in the dark increases with ODC-layer thickness, from 0.6 $\Omega \cdot cm^2$ for M-1 (no ODC-layer) to 1.2 $\Omega \cdot cm^2$ for M-4 (800 nm ODC-layer). The R_{Sh} increases even more significantly, from 1900 for M-1 to 12000 for M-4. Just as for the CIGS/FTO samples presented in the previous section, illumination is observed to induce a reduction in both R_{Sh}, and R_S, which appears to increase with increasing ODC-layer thickness. The illumination-induced reduction in R_S varies from 17% for sample M-1 to 25% for sample M-4 (800 nm ODC-layer), while illumination-induced reduction in R_{Sh} varies from 65% for cell M-1 to 95% for cell M-4. Although more statistics would be required to draw stronger conclusions about the correlation between presence of an ODC-layer deposited by LTPED and these variations in R_S and R_{Sh}, these results support the hypothesis based on the model in [8] that was presented in section 5.3 in which the ODC-layer demonstrates photoconductivity due to a high concentration of defects.

From the EQE measurements presented in Figure 56 the conversion efficiency appears to reduce with increasing ODC-layer thickness. The EQE measured on the best cell on sample M-2 (16 nm) is an exception to this trend, which was measured to be higher over the entire wavelength region. The same shape of the EQE was observed for all cells on sample M-2, but this apparently higher EQE at long wavelengths isn't reflected in a higher average J_{SC}. This result wasn't completely understood, and difficult to explain considering the absence of a similar effect in other samples.

The loss in EQE at the longer wavelengths for sample M-4 with 800 nm ODC-layer was also consistently observed for each cell and agrees well with the results obtained on samples F-1 and F-2 presented Figure 48 of the previous section 5.3. These results suggest losses in conversion efficiency occurring deeper in the bulk of the absorber for very thick ODC-layers of ($>$ 100 nm) . This result supports the hypothesis of interdiffusion taking place between ODC-phase material and the standard absorber material, either during ODC-layer deposition or afterwards. This could result in a higher defect concentration in the bulk of the absorber, causing higher recombination.

From the similar device performance observed for reference sample M-1 (without intentionally deposited ODC-layer) and samples M-3 and M-5 (with intentionally deposited ODC-layers expected to be 40 nm and 10 nm respectively) it can be concluded that very thin layers of ODC-phase material ($<$ 50 nm) have only a negligible effect on device performance, and/or that the reproducibility in performance for these samples is too low to allow this effect to be distinguished. Furthermore, it should be kept in mind that no direct evidence of an ODC-layer was obtained for any of the samples except M-4 and it might be that such a layer simply isn't present in the other samples M-2, M-3 and M-5. The clearest conclusion that can be drawn from the results presented here, is that thick ODC-layers (on the order of ~100-800 nm as present in samples F-1, F-2 and M-4) are clearly detrimental to standard device performance as it results in losses in conversion efficiencies possibly explained by the higher concentration of defects.

For the investigation of the doping densities, defect response and recombination mechanisms in the samples presented in this section, smaller area cells (with active area $\leq$ 0.1 cm^2) were selected from each sample for performing AS, C-V, IV-T and V_{OC}-T measurements. The performance parameters of these samples are shown in Table 11.

Table 11 ODC-layer thickness and performance parameters of small-area cells used for AS-, C-V, IV-T and V_{OC}-T measurements.

		M-1A	M-2A	M-3A	M-4A	M-5A	M-5B
Pulses at 12 kV		0	1	2.5	50	0.6	0.6
ODC-layer (nm)		0	16	40	800	10	10
STC	V_{OC}	576	431	527	552	480	381
	J_{SC}	28	33	33	30	29	22
	FF	75	58	65	72	66	62
	η	12.0	8.2	11.2	12.0	9.1	5.2
	R_S	0.5	0.8	1.9	0.9	0.7	1.1
	R_{Sh}	850	140	210	830	450	220
Dark	R_S	0.6	1.1	2.2	1.6	0.6	0.7
	R_{Sh}	1270	5000	710	10000	2500	830

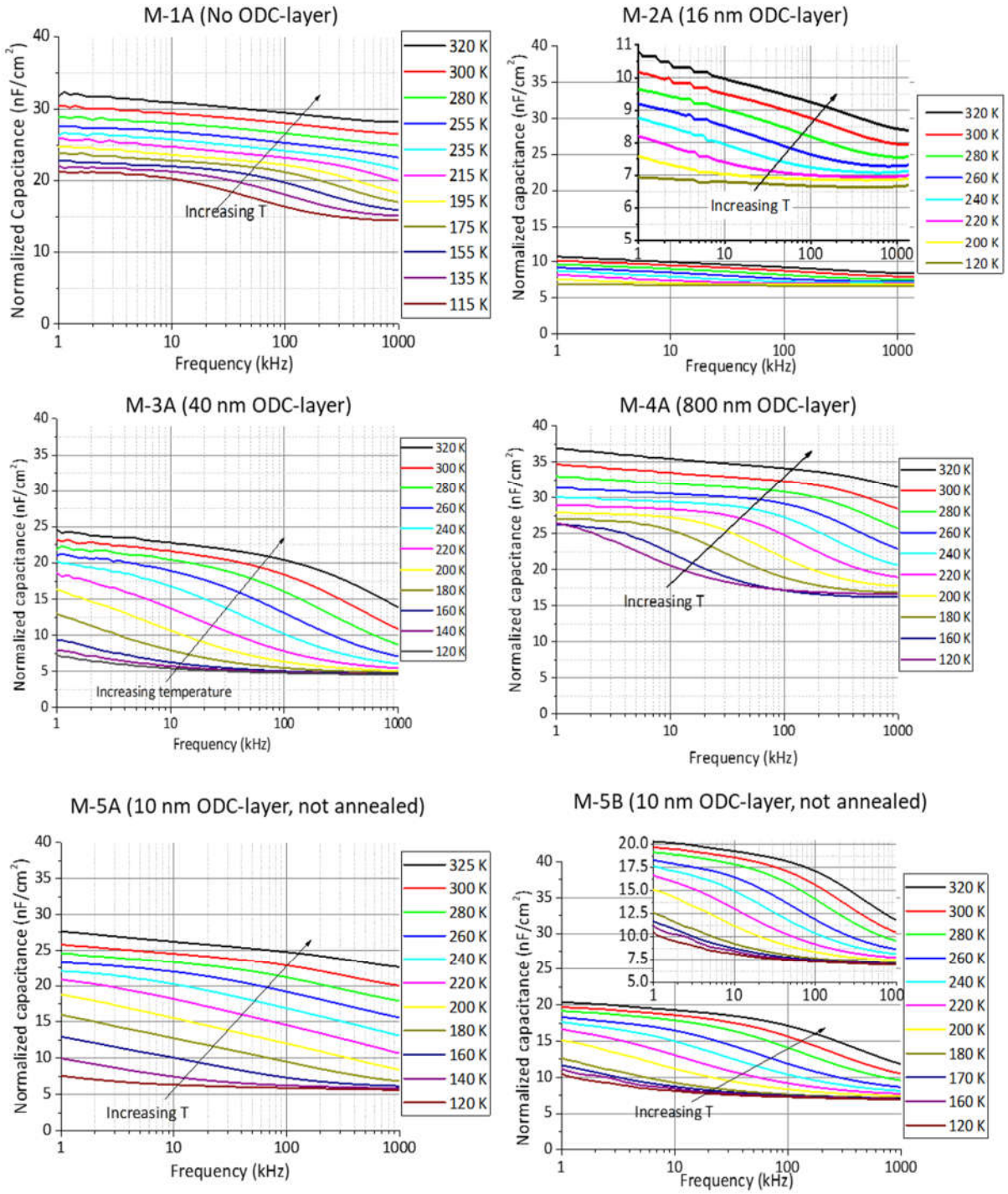


Figure 57 C-f profiles obtained for cells M-1A (no ODC-layer), M-2A (16 nm ODC-layer), M-3A (40 nm ODC-layer), M-4A (800 nm ODC-layer), M-5A and M-5B (both 10 nm ODC-layer). A 25 mV oscillation level was used for the AC-signal. In consideration of the difference in capacitance variation in M-2A and M-5B insets were added to show the most dynamic range in more detail.

The AS-spectra shown in Figure 57 are quite similar for each of the investigated cells, with exception of M-2A where very little variation in the capacitance is observed . In cell M-2A (16 nm ODC-layer, $\eta = 8.2\%$). Similar profiles reported in [48] were attributed specifically to low Na-doping. Insufficient Na-doping in sample M-2 would be in agreement with the low efficiencies observed on most cells on this sample (see

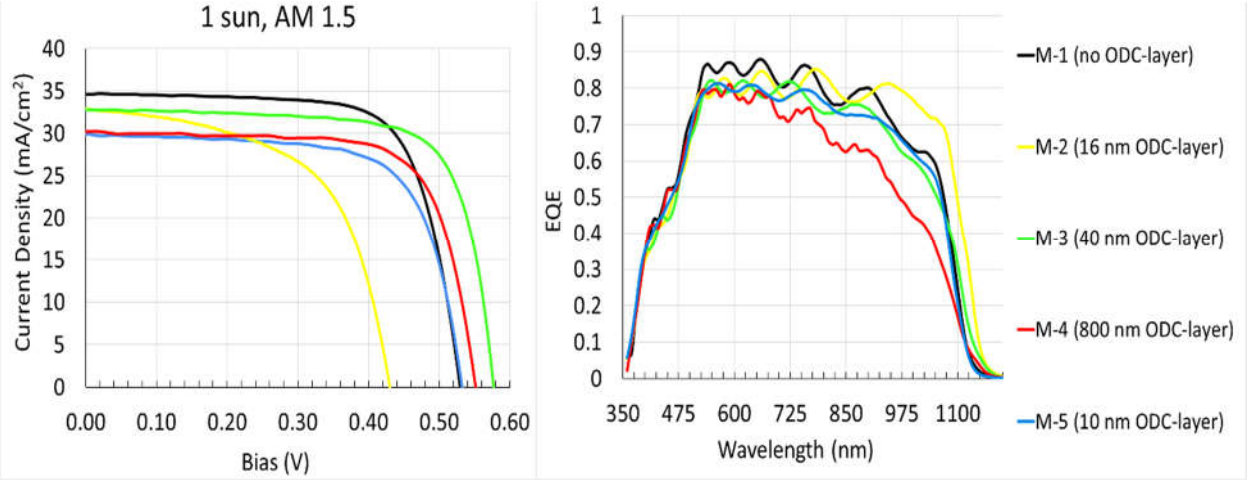


Figure 56 Left: IV-characteristics measured at STC (AM1.5G at 1 sun, 25°C sample temperature). Right: EQE of best cell from each of the samples M-1 to M-5. All samples had the standard LTPED architecture presented in Chapter 4. All samples were annealed for 20 minutes at 250°C after the CIGS deposition with exception of M-5, which wasn't annealed.

Table 10) and the complete depletion derived from C-V measurements performed on cell M-2A (see Figure 59)

In the AS-spectra of the other cells, steps similar to the N1 and N2 steps commonly reported in literature can be distinguished from the profiles. By comparing the initial capacitance at low frequency and high temperature (C_0) with the capacitance high frequency and low temperature (C_∞) or the capacitance at frequencies and temperatures at which the N1 or N2 step were completely observable, the relative contribution to the capacitance originating from defect response was estimated from each AS spectrum, with results shown in Table 12. The reported estimates for the 'Total' contribution due to defects were estimated from the ratio $\frac{C_0-C_\infty}{C_0}$, while the contributions from N1 and N2 were estimated from the ratios $\frac{C_1-\Delta C_N}{C_1}$, with C_1 referring to the capacitance at the start of the N1 or N2 step (i.e. for the N2 step $C_1 = C_0$ while for the N1 step $C_1 < C_0$). From these estimates, the total defect contribution to the capacitance is found to vary from ~38% for cell M-2A ~81% for cell M-3A (40 nm ODC-layer, $\eta = 11.2\%$).

Table 12 Rough estimations of the relative defect contribution as calculated from the AS-measurement results, as explained in the text.

Cell	ODC-layer thickness	η	Total	N2	N1
M-1A	0	12.0	54	15	28
M-2A	16	8.2	38	---	---
M-3A	40	11.2	81	14	70
M-4A	800	12.0	55	10	37
M-5A	10	9.1	79	12	66
M-5B	10	5.2	66	10	53

The large variations in the relative contribution from defects mostly reflects variations in the contribution from N1 defects, which ranges from 28% in M-1A (no ODC-layer, η = 12.0%) to 70% in M-3A (40 nm ODC-layer, $\eta = 11.2\%$) while the relative contribution from the N2 defect lies in the 10-15% range for all samples. The relative contribution to the capacitance from defects shows

no clear correlation to the ODC-layer thickness, suggesting the electronic levels detected in AS are related to defects in the bulk of the P-type CIGS absorber or at the ODC/P-CIGS interface, and that the CIGS absorber layer is still the material being investigated.

For cells M-2A, M-3A, M-4A, M-5A and M-5B Arrhenius plots of $\ln\left(\frac{\omega_0}{T^2}\right)$ could be constructed (see Figure 58), by determining ω_0 corresponding to the N1 step from the peaks in the $\left[-\omega \cdot \frac{dC}{df}\right]$. The activation energies E_d derived for the centre of the trap distributions from these plots varies significantly between cells. For M-2A (16 nm ODC-layer) and M-3A (40 nm ODC-layer) values of respectively $\sim$232 meV and $\sim$202 meV are found in the entire range of investigated temperatures. For cell M-4A (800 nm ODC-layer) an estimate of E_d $\sim$113 meV is found. For cell M-5A (10 nm ODC-layer) the estimated value of E_d shows some temperature dependence, with a value of $E_d \sim$ 29 meV for $T < 180$ K, and$dE_d \sim$ 51 meV for $T > 180$ K. For cell M-5B an estimate of $E_d \sim$180 meV is found in the entire temperature range.

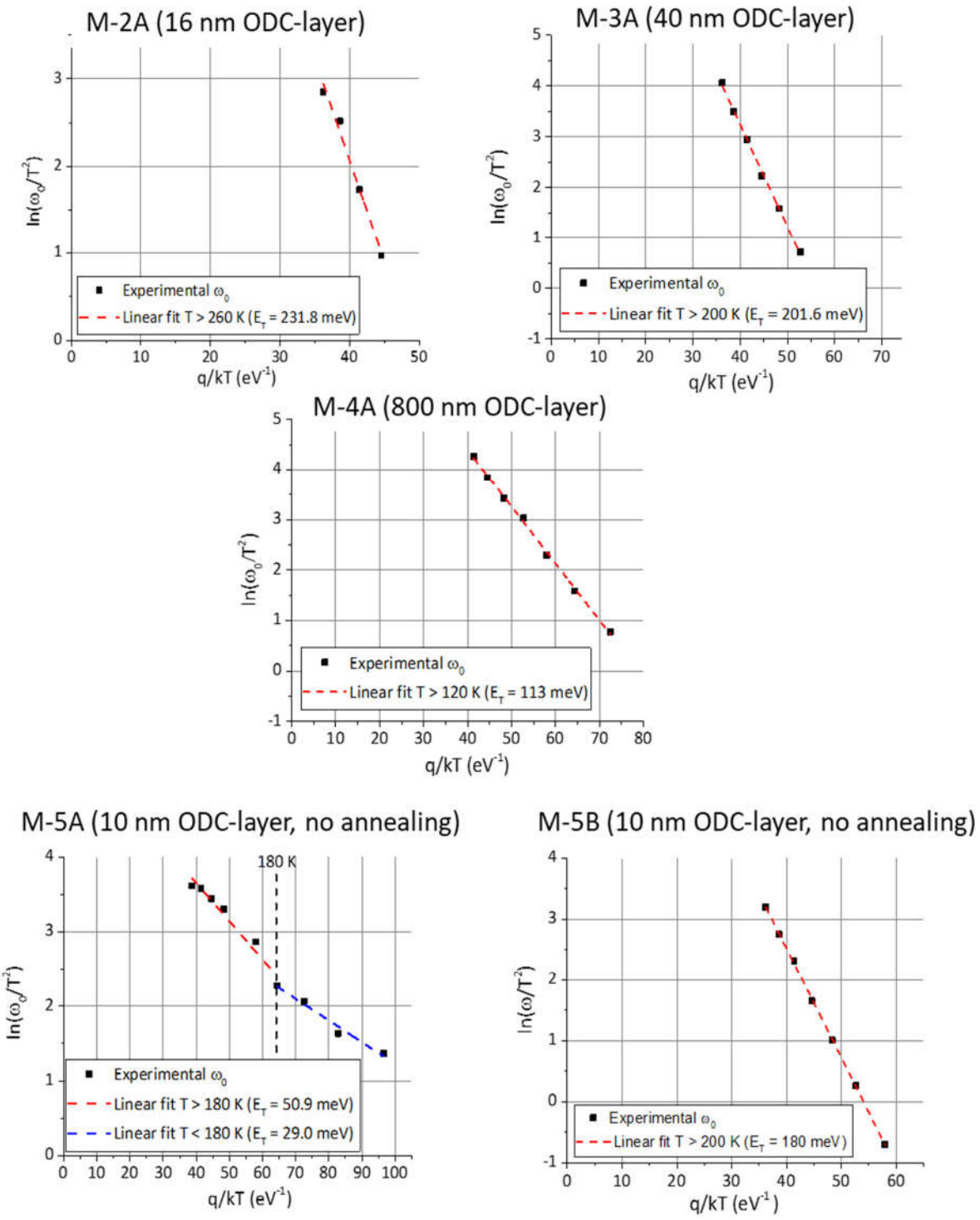


Figure 58 Arrhenius plots of $\left[\omega \cdot \frac{dC}{d\omega}\right]$ for cells M-2A (16 nm ODC-layer, top left), M-3A (40 nm ODC-layer, top-right), M-4A (800 nm ODC-layer, centre), M-5A (10 nm ODC-layer, bottom-left) and M-5B (10 nm ODC-layer, bottom-right). Energies of the N1 trap level were found to be located in the range of 29-232 meV from the VBE.

The values of $\mathrm{E_d}$ obtained for cells M-4A and M-5A agree quite well with the typical range reported for the N1 defect in literature (∼50-150 meV). The values of $\mathrm{E_d}$ obtained for cells M-2A, M-3A and M-5B, all ∼200 meV, seem to lie between the values typically reported for the N1 and N2 defect (the latter being in the range of ∼260-280 meV) [105] [106]. This suggests in these three cells the trap distribution corresponds to neither the typical N1 or N2 level, or that the N1 and N2 levels in these cells overlap, leading to a common centre in the distribution. Judging from the AS-profiles in Figure 57 cell M-2A might be expected to contain a single distribution of defects (i.e. possibly formed by an overlapping N1 and N2 distribution). For cells M-3A and M-5B on the other hand, the distinction between the N1 and N2 steps seems to be quite clear, suggesting presence of a N1-like' defect with slightly deeper activation energy than those typically reported. Since the N1 defect is also reported to strongly depend on the surface treatment applied to the absorber, this would also seem plausible in this case where an additional deposition step was performed.

The apparent free carrier density profiles obtained for the same cells from C-V measurements are shown in Figure 59. The depletion-layer width w and free carrier density N derived from the minima of the profiles obtained in C-V measurements performed at ∼120 K and 1 MHz oscillation frequency of the AC-signal (see Table 13) were expected to be accurate, considering the saturation observed in the C-f spectra in this temperature- and frequency-range. Also in this case, no clear correlation was found between the values obtained for N and w and the ODC-layer thickness.

The doping level of $\sim 3 \cdot 10^{15}$ cm^{-3} and depletion layer width of 0.7 μm observed for cell M-1A (without ODC-layer), is comparable to the typical values obtained in standard LTPED devices reported in Chapter 4. Similar results are obtained for cell M-4A (800 nm ODC-layer, $\eta = 12.0\%$) with a doping level of $\sim 2.8 \cdot 10^{15}$ cm^{-3} and depletion layer width of 0.6 μm. These results confirm the importance of sufficient Na-doping for reaching efficiencies $\eta \geq 12\%$.

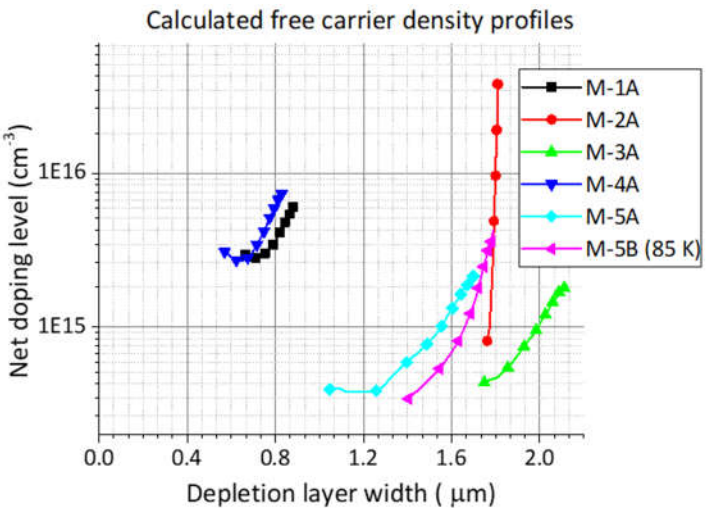


Figure 59 Apparent free carrier density profiles calculated from C-V measurements performed on CIGS/Mo samples with intentionally deposited ODC-layer. All measurements were performed at 1 MHz using a 25-mV amplitude AC-signal. The DC-bias was swept in the range of -0.5 V $\leq$ V $\leq$ 0.5 V. With exception of the measurement for cell M-5B, all measurements were performed at 120 K.

The shape of the profiles obtained for cells M-3A, M-5A and M-5B suggest a nearly (but not fully) depleted absorber layer, as some variation in the depletion layer is still observed. The efficiencies of these samples are relatively low (9.1%-11.2%) but not significantly lower than in typical LTPED devices. Nevertheless, the calculated apparent free carrier densities (N~$4.4\cdot10^{14}$ cm^{-3}, $3.8\cdot10^{14}$ cm^{-3} and $3\cdot10^{14}$ cm^{-3}) are well below the doping level of 10^{15} cm^{-3} for which a depleted absorber layer would be expected. These values for N and w might be inaccurate due to a inaccuracies in the optically determined active areas of the cells.

Table 13 The ODC-layer thickness, conversion efficiencies, calculated depletion layer widths w and calculated free carrier densities N derived from the minima of the N-w profiles shown in Figure 59 for the investigated CIGS/Mo cells.

Cell	ODC-layer	η	w	N
M-1A	0	12.3	0.7	$2.8\cdot10^{15}$
M-2A	16	8.2	1.8	$\ll 10^{15}$
M-3A	40	11.2	1.8	$4.4\cdot10^{14}$
M-4A	800	12.0	0.6	$2.8\cdot10^{15}$
M-5A	10	9.1	1.2	$3.8\cdot10^{14}$
M-5B	10	5.2	1.4	$3\cdot10^{14}$

The results of V_{OC}-T measurements performed on cells M-1A, M-2A, M-3A, M-4A and M-5A are reported in Figure 60. Linear fits performed in the high temperature region ($T \geq 200$ K) give an intercept with the vertical axis in the range of 1000-1050 meV (i.e. close to the absorber bandgap of ~1.05 eV) for each cell with exception of M-2A, indicating SRH recombination in the bulk of the absorber limits the V_{OC} in nearly all cells, except in cell M-2A. This is quite similar to the observations made in Chapter 4 for typical LTPED devices, again indicating no significant effect due to the ODC-layer.

For cell M-2A, the lower V_{OC} (431 mV) and an intercept with the vertical axis in the V_{OC}-T characteristics well below the expected bandgap (~768 mV) suggest interface recombination plays an important role in this cell. This would be expected to be mainly due to the CIGS/CdS, ODC/CIGS or ODC/CdS interface.

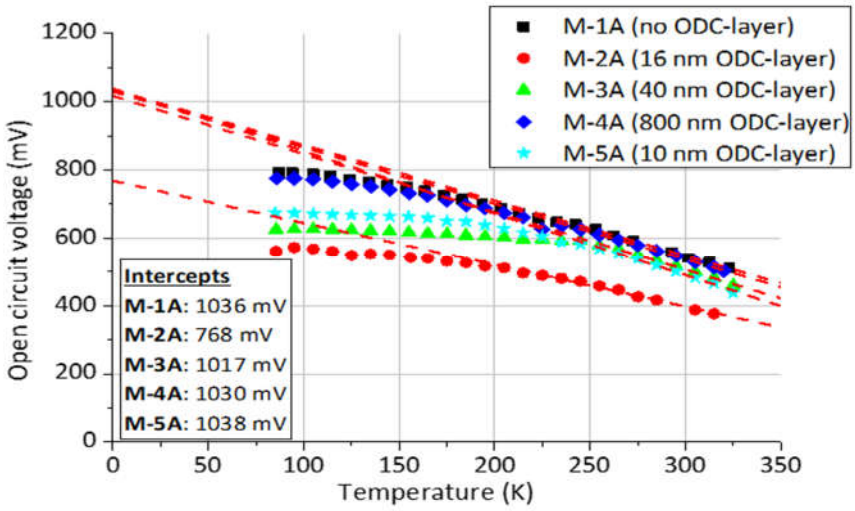


Figure 60 The V_{OC}-T characteristics obtained for the CIGS/Mo samples with varying ODC-layer. The intercepts are calculated from linear fits of the high-temperature ($T>200$ K) region.

5.5 SUMMARY AND CONCLUSIONS

Introduction of ODC-phase material in LTPED devices was observed to have very little effect for thin layers ($<$ 100 nm) and negatively impact device performance for thick layers ($>$ 500 nm). The negative effects observed for thick ODC-layers were mainly a loss in J_{SC}, increase in R_S, reduction in R_{Sh} and, hence, reduction in FF. In a few cases increased interface recombination also appeared to cause significant reduction in the V_{OC}, but these effects weren't found to be consistently correlated to presence of the ODC-layer.

In comparison to standard LTPED devices, devices with implemented ODC-layer showed higher R_S and R_{Sh} which more strongly depended on illumination. The observed illumination dependence was attributed to low dark conductivity and photoconductivity of ODC-phase material. The low dark conductivity in the ODC-layer would explain an increased R_{Sh} in samples with high ODC-layer thickness, as the ODC-phase material might cover shunting paths at the surface of the absorber. Under illumination, the increased conductivity in the ODC-layer would then lead to the strong reduction in R_{Sh} observed for various samples. The same effect would explain the variation in R_S under illumination. Various models have already been proposed for photoconductivity in the ODC-layer and/or reduction of a barrier to charge carriers at the ODC/buffer or ODC/absorber interfaces [8].

In EQE measurements some samples showed slight losses in conversion efficiency, most notably at higher wavelengths for samples with thick ODC-layers (100-800 nm). Meanwhile, for various samples with thin ODC-layers no or a negligible effect in the EQE was observed. The observed variations in spectral response might be unrelated to presence of an ODC-layer, and be correlated to e.g. variations in the quality of the absorber material closer to the back-contact (explaining the losses occurring at higher wavelengths). Under the assumption that presence of a thick ODC-layer does cause the observed losses in EQE, this would be best explicable if during or after the ODC-layer deposition interdiffusion of the normal P-type absorber layer and ODC-layer took place, such that a higher defect concentration also occurs deeper inside the bulk of the absorber.

The results from AS in the samples with ODC-layer showed similar behaviour as observed in typical LTPED devices. Usually two steps similar to the typical N1 and N2 levels can be distinguished (see Chapter 3 and Chapter 4). The activation energy of one of the steps (expected to correspond to the same N1 defect) could be estimated from Arrhenius plots, and was found to vary from 51 meV to 232 meV. The results indicated no correlation with presence or thickness of the ODC-layer. Only the AS-spectra obtain for cell F-2A (CIGS/FTO with expected 160 nm ODC-layer) were rather unusual, as a large capacitance step was observed at low frequency with very little temperature dependence in the inflection point. The low temperature dependence might be an indication of interfacial states, which would be located at the CIGS/ODC or ODC/CIGS interface.

The C-V profiles showed the same type of variations in the carrier densities as in typical LTPED devices. In devices with reasonable performance the depletion layer width was found as $w \sim 0.5$ μm, with charge carrier densities $N \sim 10^{15}$ cm^{-3}. Also in this case no clear effect of the ODC-layer was observed.

The main recombination mechanisms derived from V_{OC}-T measurements were found to vary between the CIGS/FTO and CIGS/Mo samples. In the CIGS/FTO samples the low value of the intercept with the vertical axis and therefore the low activation energy $E_a \sim$ 915-956 mV showed an important contribution of interface recombination in limiting the V_{OC}. In CIGS/Mo samples on the other hand, the activation energies of ~1.05 mV showed the dominant recombination mechanism limiting the V_{OC} to be SRH recombination in the bulk. The only exception in this case was cell M-2A (with an expected ODC-layer thickness of only 16 nm) where interface recombination was found to be the most probable explanation for the large V_{OC} loss observed in the cell.

6 Damp heat and degradation

INTRODUCTION

During this thesis the most important goal of the activity at IMEM-CNR related to LTPED was still the optimization of the performance of small area (lab-scale) devices. However, with the perspective of upscaling the technology for application on an industrial scale the stability and predictability in performance of the solar cells produced by LTPED are at least as important as the initial efficiency. Although predicting the lifetime of CIGS-based devices is still complicated due to the relative youth of the technology, a current standard has been established for testing whether devices will meet the typical demands for product lifetime [124]. The current chapter reports on some preliminary results of such tests on LTPED devices with standard architecture presented in Chapter 4 and without additional encapsulation. Hence, these results can be considered to give an indication of the intrinsic stability of the active materials in LTPED devices. The treatment and measurements for these investigations were performed at Solliance located in Eindhoven, The Netherlands.

Before the obtained results are presented in sections 0 and 6.3, a brief introduction of the concept of Accelerated Lifetime Tests' (ALT's) is given in section 6.1. Finally, a summary with conclusions is presented in section 6.4

6.1 ACCELERATED LIFETIME TESTS (ALT) AND DAMP HEAT TREATMENT

Efficient implementation of photovoltaics requires an indication of the period for which stable and cost-effective performance can be expected (the 'economic lifetime') for a solar cell or module. In photovoltaics 'stable' performance is typically considered to be failure-free operation at no less than 80% of the initial performance. Increasing the average economic lifetime reduces overall product cost and material usage.

The economic lifetime needs to have high predictability and reproducibility for different solar cells from the same production line so that good assessments of the economic feasibility can be

made for any application [125]. To achieve these goals, solar cell manufacturers need to be aware of the origin of the most important failure mechanisms and how to prevent their occurrence. ALT's have been designed specifically to test for and identify the failure mechanisms that can be expected to occur over the lifetime of a typical photovoltaic device. In ALT's the solar cells are exposed to extreme conditions for a relatively short period of time to simulate the stresses expected during long-time outdoor exposure. The 'Damp Heat' (DH) test, exposure to 85% relative humidity and 85°C for at least 1000 hours, is currently considered to be one of the most important benchmarks.

The design of effective ALT's for CIGS TFSC's isn't straightforward, since the technology is still relatively new (i.e. in comparison with Si) and not much field data is available from which the most important stresses for CIGS based devices can be derived. Even though during the past decades much has been learned in this respect, too much fundamental knowledge is still lacking. Hence, most of the current standards for testing CIGS-based devices were adopted and slightly adapted from those for c-Si and α-Si [124] which most likely resulted in tests that don't reveal all failure mechanisms relevant for CIGS-based devices. As a result, the protective 'barriers' used for thin film CIGS-based devices are very probably overdesigned with more expensive material than necessary [9]. Currently, the costs of these protective materials constitute $\sim$1/3 of the total price of commercial modules.

Although, as mentioned above, the LTPED technique is still in a relatively premature phase (i.e. relatively far from industrial application) it is a promising technique to allow further cost reduction in processing of CIGS based devices. By already testing unprotected LTPED devices in ALT's at this early stage, an indication of the most important failure mechanisms might be obtained, which could give indications of further possible improvements for the technique to optimize the lifetime of the devices and offer indications about how these devices ought to be protected in the most cost-effective way. This was the most important motivation for the preliminary tests presented in the following sections of this chapter.

6.2 EXPERIMENTAL APPROACH

Two standard 1-inch by 1-inch LTPED devices (see Chapter 4), referred to as DH-1 (GGI = 0.375) and DH-2 (GGI = 0.3) in the following (see Table 14) were used to investigate failure mechanisms in unprotected LTPED devices. Each sample was cut in half after completion. One half (referred to as part 'A' for both samples, i.e. DH-1A and DH-2A) was stored in a N_2 environment in a glove box over the entire course of the experiment as reference. The IV-curves of these samples were measured directly before and directly after the experiment, with results shown in Figure 61. The other two halves of the samples (DH-1B and DH-2B respectively) were exposed to DH to study the degradation. For the B-samples, the performance was monitored by measuring the IV-curves at STC after every 20 hours in DH.

Table 14 Properties and average performance parameters of the 1-inch by 1-inch laboratory scale LTPED devices used in degradation experiments for this thesis, before being exposed to DH. Only results for cells with initial efficiencies $\eta \geq 5\%$ are presented. The reported R_{Sh} and R_S refer to the values measured under illumination.

Sample	**DH-1**		**DH-2**	
GGI	0.375		0.3	
	Part A	Part B	Part A	Part B
Damp heat	0	80	0	60
η (%)	7.5 ± 0.7	7.7 ± 0.8	8.6 ± 0.6	7.8 ± 0.7
V_{OC} (mV)	511.7 ± 5.4	530.7 ± 7.4	$540.4 \pm$	521.4 ± 7.9
J_{SC} (mA/cm^2)	23.2 ± 1.5	24.9 ± 0.7	24.9 ± 1.6	25.3 ± 0.3
FF (%)	63.5 ± 1.8	58.1 ± 4.4	64.3 ± 0.6	59.3 ± 4.5
R_{Sh} ($\Omega \cdot$cm^2)	317 ± 71	262.9 ± 135	398 ± 52	343 ± 318
R_S ($\Omega \cdot$cm^2)	3.3 ± 0.4	3.9 ± 0.3	3.1 ± 0.0	2.7 ± 0.2

6.3 RESULTS: DEGRADATION OF LTPED DEVICES

All cells on the investigated samples had relatively low initial efficiencies ($\eta < 10\%$) in comparison to typical LTPED devices. With one exception, only the cells satisfying $\eta \geq 5\%$ (five cells on DH-1B and four cells on DH-2B) are reported here. The average initial performance parameters and standard deviations measured on both parts of the samples before DH treatment are shown in Table 14. The effects of damp heat on the conversion efficiency and spectral response were investigated by performing STC IV measurements (Figure 61-Figure 63) and EQE measurements (Figure 64 and Figure 65). Lock-In Thermography (LIT) was used to investigate changes in the locations of shunts in the cells (Figure 68), and structural damage to the cells was observed using optical microscopy (Figure 66) and Scanning Tunnelling Electron Microscopy (SEM, Figure 69)

In Figure 62 and Figure 63 the performance parameters of the cells on DH-1B and DH-2B are plotted against the time of exposure to DH. For most cells a decrease in efficiency is observed as would be expected. The observed efficiency losses are in the range of $-47\% \leq \Delta\eta \leq -4\%$ on sample DH-1B and $-32\% \leq \Delta\eta \leq -7\%$ on sample DH-2B. Typically the changes in efficiency can be attributed to variations in the R_S and R_{Sh} while the V_{OC} and J_{SC} hardly change ($-6\% \leq \Delta V_{OC} \leq 3.5\%$, $-1\% \leq \Delta J_{SC} \leq 9\%$). These results are in agreement with those typically observed in literature for similar periods of DH treatment applied to CIGS based devices [10].

Cell DH-2B-4 is the only cell on which the V_{OC} decreases significantly (15%) after 60 hours DH, Combined with the 150% increase in R_S, this results in a 50% drop in efficiency, much larger than in the other cells. Also the best performing cells on each sample exposed to DH (DH-1B-1 and DH-2B-1, with IV-curves reported in Figure 61) mostly show variations in R_S and R_{Sh}. Also reported in Figure 61 are the IV-curves measured before and after the DH experiments on the best cells on samples DH-1A and DH-2A, which had been left in the glove box in an N_2 environment as reference. The negligible amount of variation in performance before and after the experiment period confirms the degradation in DH-1B and DH-2B can be ascribed to the DH treatment.

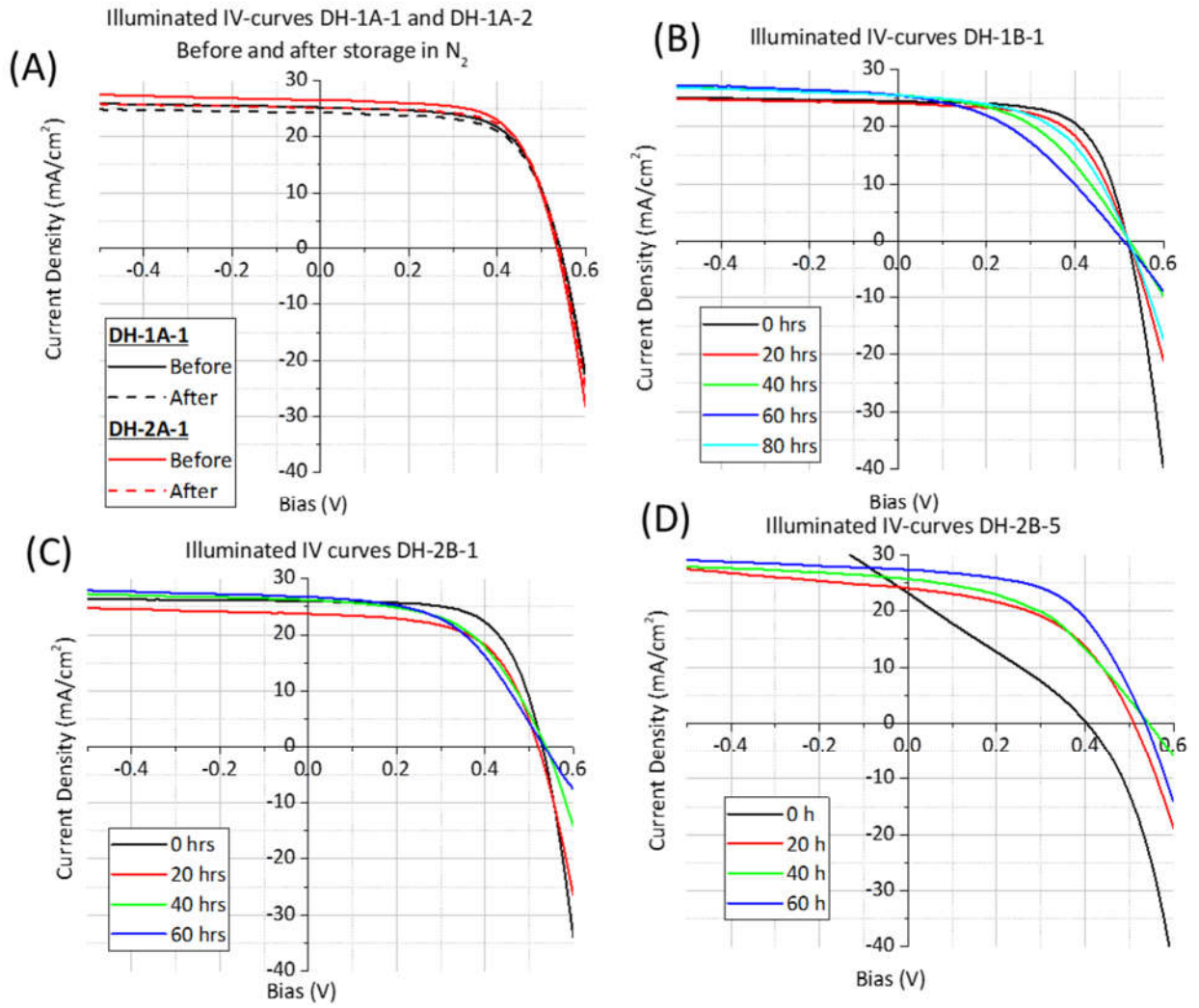


Figure 61 (A) Illuminated IV-curves measured on reference cells DH-1A-1 and DH-2A-2. The reference samples DH-1A and DH-2A were kept in an N_2 environment during the DH experiments on samples DH-1B and DH-2B. Reported IV-curves were of the reference cells were measured 'Before' and 'After' the DH experiments on DH-1B and DH-2B (B), (C) and (D): I-V curves after different times in DH measured on cells DH-1B-1 (B), DH-2B-1 (C) and DH-2B-5 (D). Cell DH-2B-5 was the only cell on which an improvement in performance was observed after DH treatment.

After the exposure to DH R_S is observed to increase by 100% to 400% for the cells on sample DH-1B, and 50% to 275% for the cells on DH-2B. Possible causes typically reported for this increase in R_S are corrosion of the Mo and TCO, and ingression of water into the Al-ZnO layer [11] [9]. Also a reduction of type-inversion at the CIGS/CdS interface and an increase in deep defect density in the CIGS absorber have been suggested [10] [12]. In the LTPED devices studied here, effects of oxidation and degradation were confirmed by optical microscopy (see Figure 66).

The changes in R_{Sh} for the different cells are less consistent. On sample DH-1B decreases in R_{Sh} in the order of 25% to 82% is observed. On the best performing cell on sample DH-2B (DH-2B-1) a reduction of 47% is observed after 80 hours of DH. On the other cells R_{Sh} either remains the same or increases, with the largest observed increase 210% on DH-2B-3. The decrease in R_{Sh} is typical after DH exposure and can be attributed to formation of pinholes in the material or diffusion of metals and dopants [9]. Regarding the diffusion of metals or dopants, it was light-induced migration of Na via the grain boundaries might lead to formation of shunting paths in regions having initial high concentrations of Na [11]. The observed increase in R_{Sh} is anomalous. For two of the investigated cells it leads to a significant increase in overall device performance after the DH treatment: a 300% increase in R_{Sh} and 5% increase in J_{SC} on cell DH-2B-3 after 60 hours of DH resulted in a 10% efficiency increase, and a 1510% increase in R_{Sh} on cell DH-2B-5 after 80 hours of DH resulted in a 290% efficiency increase, with respect to the initial values. These changes are clearly visible in the corresponding IV-curves shown in Figure 61. Also in LIT some 'shunts' (i.e. observed as hot regions with the infrared detector under red light excitation) were observed to disappear (see Figure 68). If these hot spots observed in LIT correspond to actual shunts, their disappearance is in agreement with an increase of R_{Sh} with time in DH for some of the cells. A possible explanation of this effect might be initial shunting at regions where a short circuit is formed between TCO front-contact and Mo back-contact (e.g. at the scribe lines). Under DH, both TCO and Mo are known to degrade, leading to increased resistance of both layers and, possibly, partial detachment of these layers in some areas. This could lead to disappearance of the short-circuited ('shunted') regions present before DH treatment .

Another explanation might be Na-diffusion during DH, in locations where initially a too high Na doping results in shunting. The observations of crystallites formed at the surface of the cells during the DH treatment, as shown in Figure 66 (most likely due to out-diffusing Na) support this second explanation [11] [9].

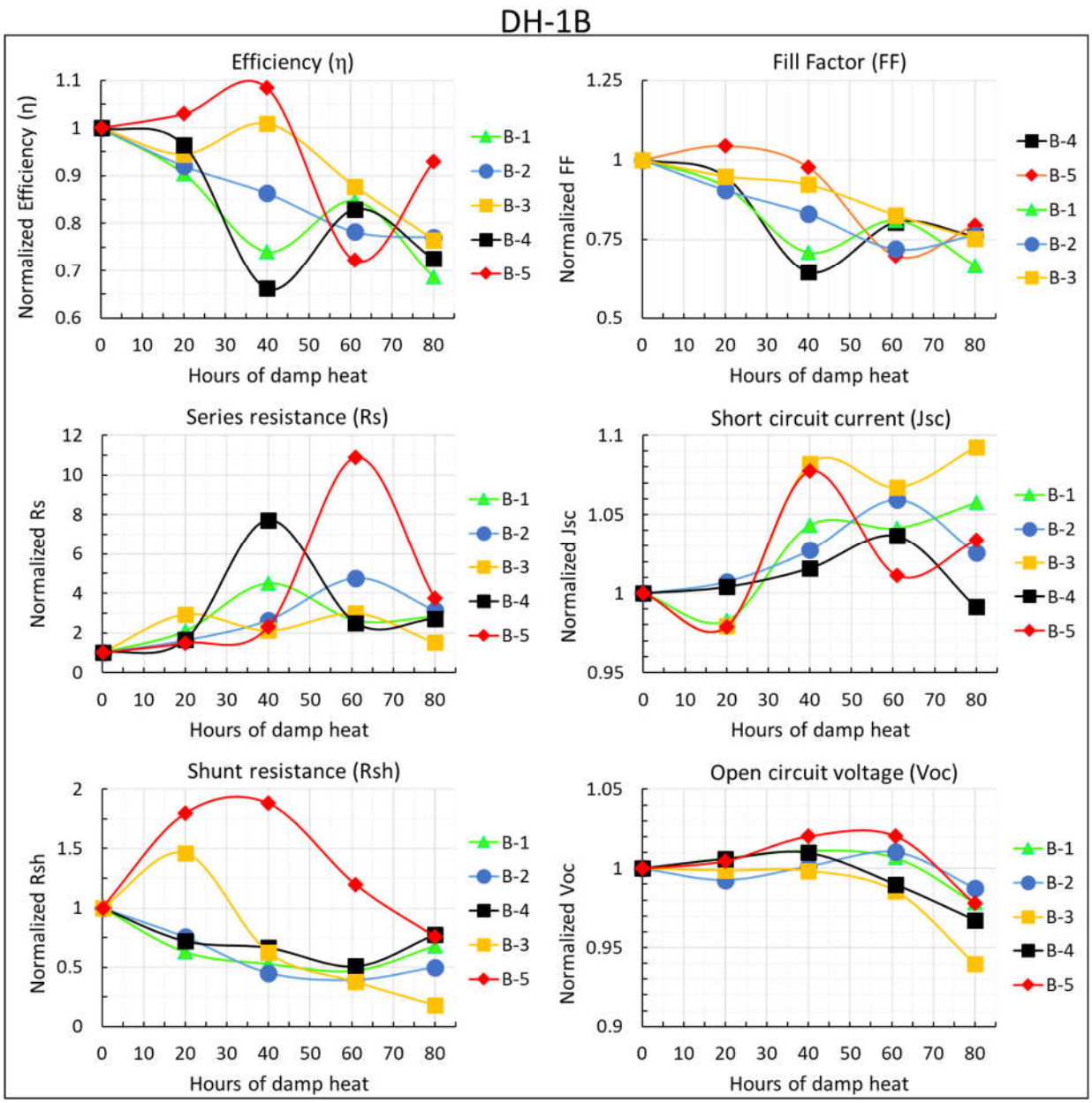


Figure 62 Performance parameters for sample DH-1B (GGI = 0.375) as function of time in damp heat setup. The cells were labelled in order of reducing efficiency. Note that the scales were chosen differently for each parameter to show the full range of variation.

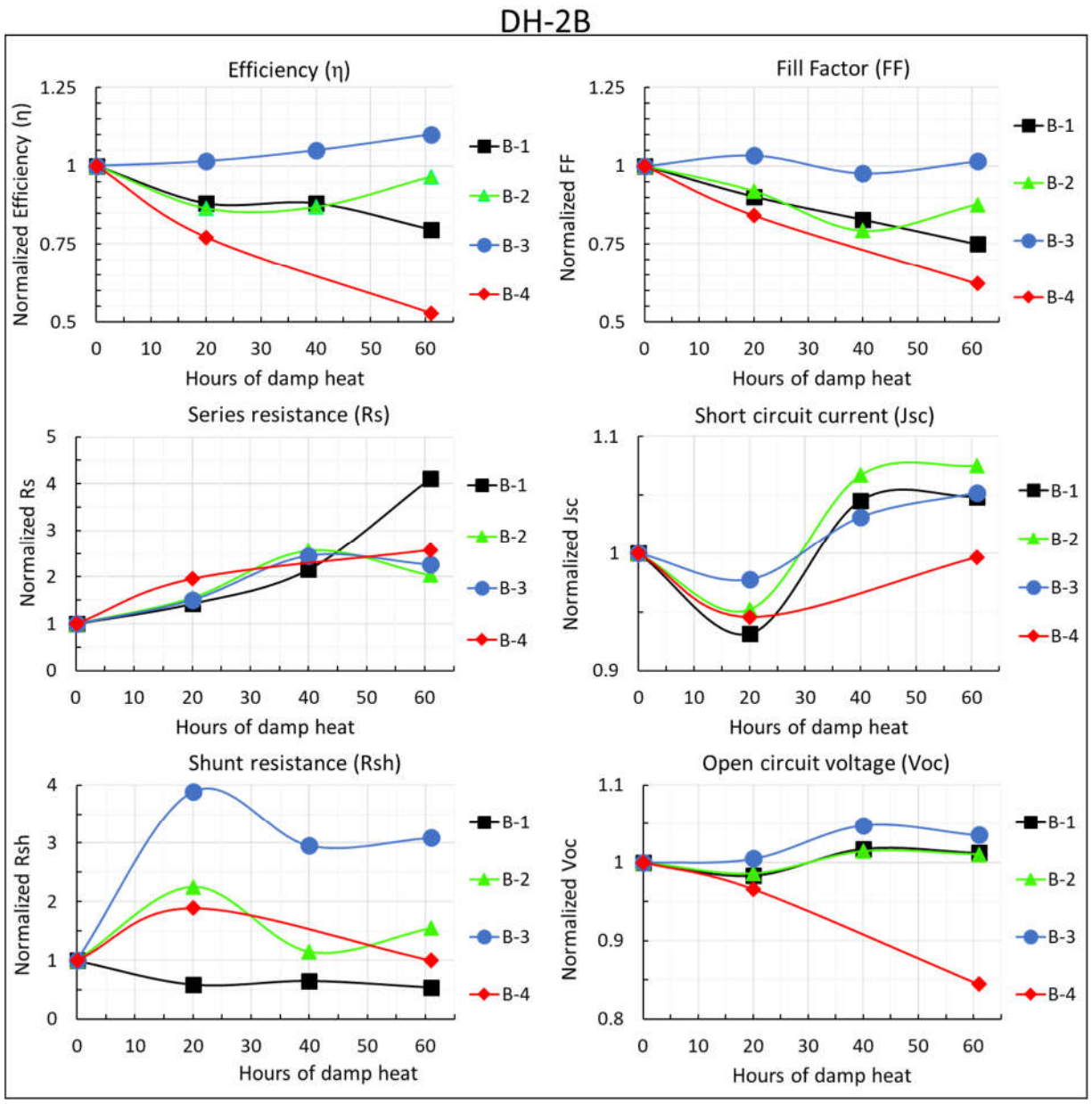


Figure 63 Performance parameters for sample DH-2B (GGI = 0.3) as function of time in damp heat setup. The cells were labelled in order of reducing efficiency. Note that the scales were chosen differently for each parameter to show the full range of variation.

The results of EQE measurements for both samples DH-1 and DH-2 are shown in Figure 64 and Figure 65. The decision to analyse whether effects of damp heat treatment could be distinguished from EQE measurements was made after the degradation, so that no comparison could be made between the EQE of the same cell before and after degradation. Instead, cells from the non-

degraded parts DH-1A and DH-2A (referred to as 'A-1' in both figures) were taken as reference. The efficiencies of the different cells are reported in Table 15 (for DH-1) and Table 16 (for DH-2). Although the absolute EQE curves are also reported, the normalized EQE curves are used for the comparison since the measurements were performed on different cells.

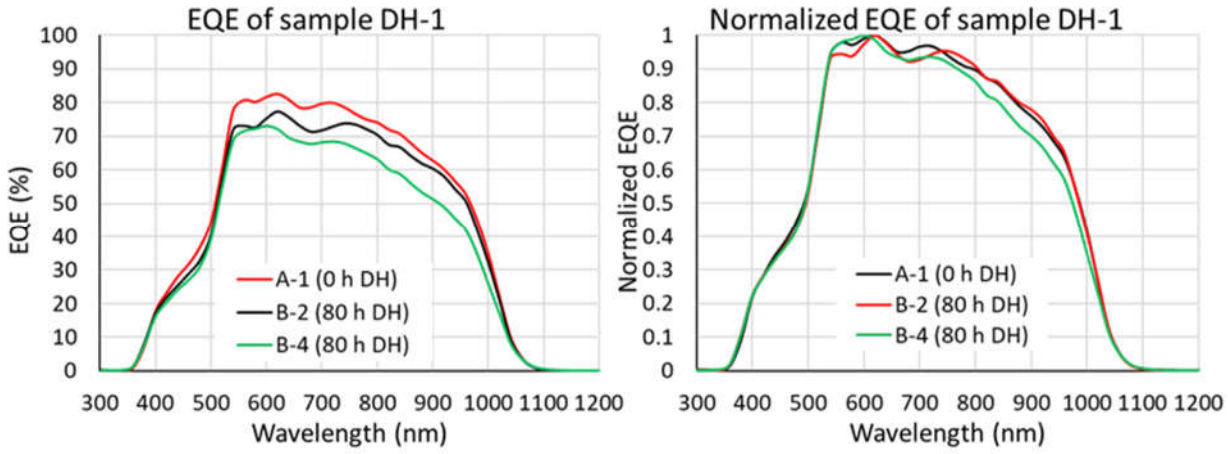


Figure 64 Absolute (left) and normalized (right) EQE measured on sample DH-1 (GGI = 0.375). Cell A-1 (red curve) didn't undergo DH treatment, while cells B-2 (black curve) and B-4 (green curve) have been exposed to 80 hours of DH

Table 15 Efficiencies of cells on sample DH-1, for which EQE curves are reported in Figure 64

DH-1	η (%) before DH	η (%) after 80 h DH
A-1	8.7	*Not exposed to DH*
B-2	8.2	5.8
B-4	7.0	4.9

For both samples DH-1 (Figure 64) and DH-2 (Figure 65) the difference between the EQE curves measured for the reference sample A-1 and the DH-treated samples is small, apart from a lower overall EQE in some cases due to a lower current density. For sample DH-1, cell B-2 appears to have the same shape of the EQE as the reference sample, while for cell B-4 the high wavelength region 750 nm $\leq \lambda \leq$ 1000 nm appears to have a lower (relative) EQE. For sample DH-2 both DH-treated cells show a slightly lower relative EQE in the same region.

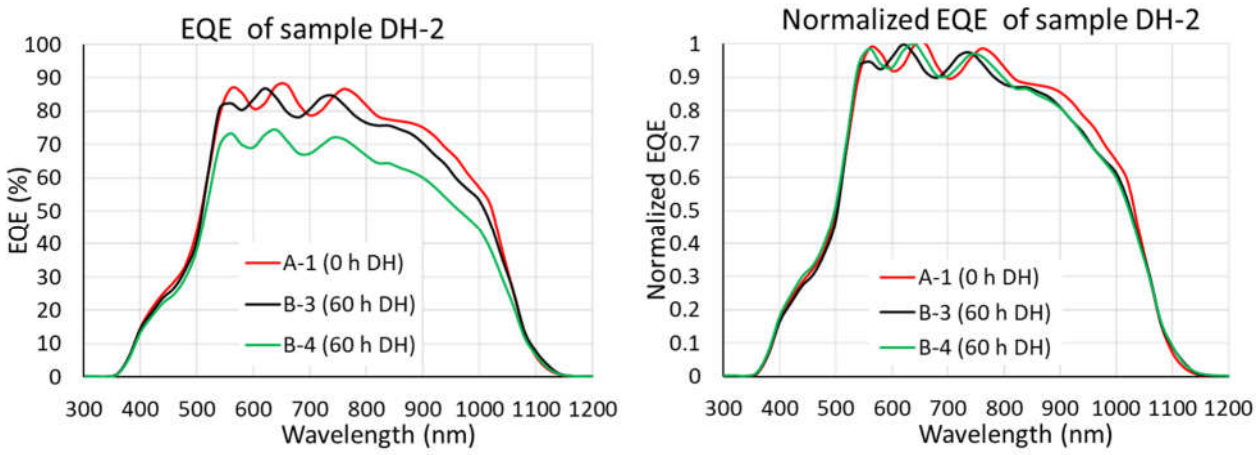


Figure 65 Absolute (left) and normalized (right) EQE measured on sample DH-2 (GGI = 0.3). Cell A-1 (red curve) didn't undergo DH treatment, while cells B-3 (black curve) and B-4 (green curve) had been exposed to 60 hours of damp heat

Table 16 Efficiencies of cells on sample DH-2, for which EQE curves are reported in Figure 65

DH-2	η (%) before DH	η (%) after 60 h DH
A-1	9.2	*Not exposed to DH*
B-2	7.4	8.1
B-4	7.1	3.7

These results indicate a possible effect of the DH exposure on the conversion at longer wavelengths, which is related to light conversion deeper in the absorber layer (i.e. close to the Mo back-contact). A plausible explanation would be discoloration of the Mo due to oxidation (see Figure 66) leading to reduced reflection back into the absorber layer. However, from the results the effect would still appear to be quite small, as also observed in the small variation in the J_{SC} with DH treatment.

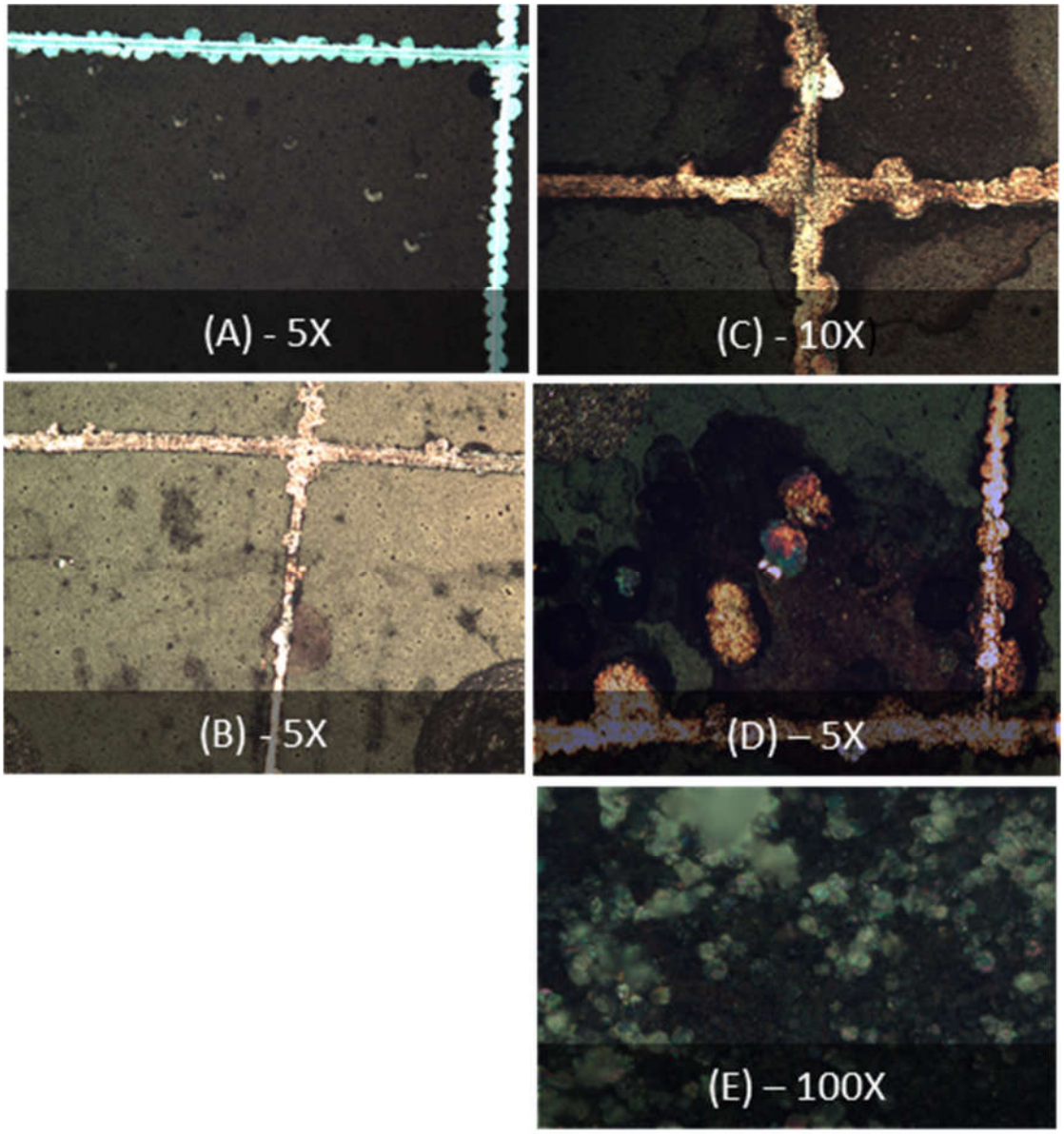


Figure 66 Optical microscopy pictures of the surface of samples exposed to DH. Fig A. and B. show pictures of a sample not exposed to damp heat as reference. (C): Oxidation of the back contact and formation of evaporation stains on the surface. (D): Discolorations (pink/purple dot in the centre) possibly indicating removal of active material at stains formed by moisture. (E) Crystals appearing at the surface, most likely due to out-diffusion of Na from the absorber layer [11].

From the more detailed analysis of the LIT results (Figure 68) it can be seen that on both samples shunts appear to be concentrated at the scribe-lines before DH, most likely due to short-circuiting between the TCO and Mo back-contact. After DH exposure more shunts are also observed toward the central areas of the cells and close to the Ag-paste contacts, suggesting certain isolated points exist at which the material between the front and back-contacts degrades relatively fast. Overall, the concentration and especially the average size of shunts appears to increase after DH treatment. Some of the shunts that were already observable before DH appear to increase in size, while some shunts disappear. The increasing size of shunts already present before DH might be explained by degradation of the material between the TCO and Mo layers, leading to better connection between front and back-contact. A reduction or disappearance of shunts might be explained by oxidation/degradation of the Mo-back or TCO leading to worsening the connection between front and back contact as already mentioned above.

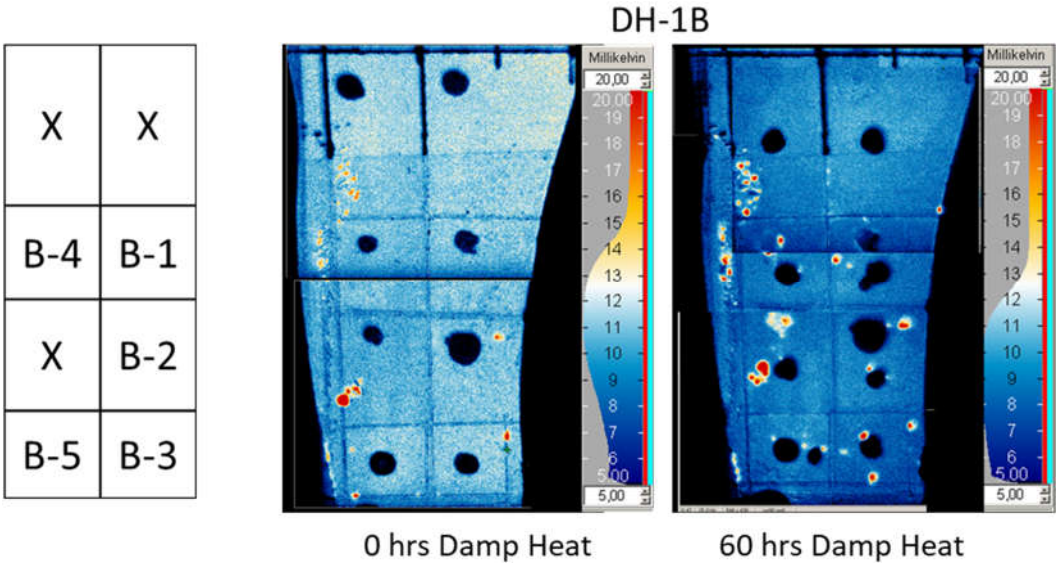


Figure 67 LIT measurements of sample DH-1B before exposure to DH (left) and after 60 hours of exposure to DH (right). The table on the left indicates the position of cells referred to in the text. The vertical scale indicates temperature fluctuations across the sample surface at illumination with pulsed infrared light (see Appendix A. Measurement techniques). Higher temperature variations indicate possible shunts.

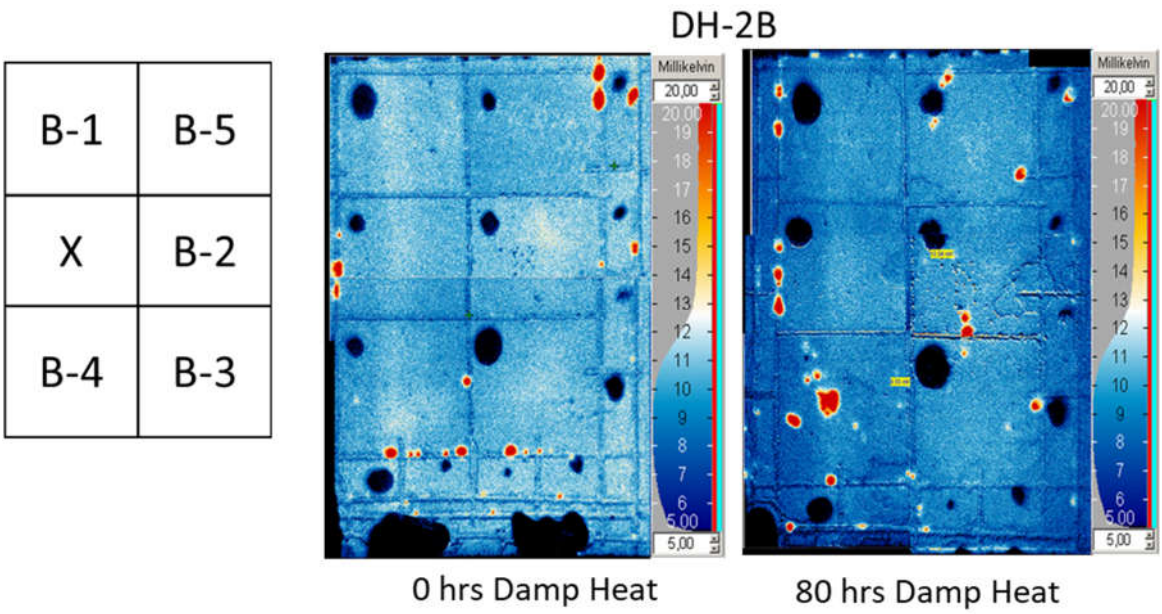


Figure 68 LIT measurements of sample DH-2B before exposure to DH (left) and after 80 hours of exposure to DH (right). The table on the left indicates the position of cells referred to in the text. The vertical scale indicates temperature fluctuations across the sample surface at illumination with pulsed infrared light (see Appendix A. Measurement techniques). Higher temperature variations indicate possible shunts.

The isolated points on the cells further from the scribe-lines at which shunts are formed after the DH treatment, might correspond to the formation of 'craters', where practically all active material between the TCO and Mo back-contact degrades and disappears. This effect was observed by SEM (see Figure 69). With Electron Dispersive X-Ray spectroscopy (EDS) the composition of the top layer was confirmed to be mainly ZnO while the underlying material appeared to be Mo, with apparently no absorber layer material in between. A possible explanation for the formation of such large craters in the samples in the case of LTPED devices might be due to the incorporation of debris formed by the high energy electron beam during deposition, as described in Chapter 4. Larger particulates incorporated into the absorber layer lead to lesser adhesion of the material deposited afterwards, and can hence be expected to result in detachment of part of the absorber layer as the surrounding material becomes damaged. This process would be accelerated in DH.

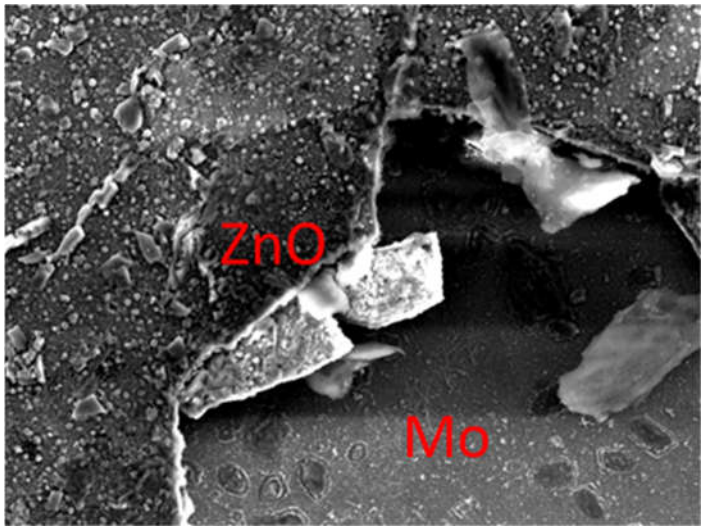


Figure 69 SEM image of a damaged region of a damp heat treated sample. Indicated in red are the compositions found by EDS measurements

6.4 SUMMARY AND CONCLUSION

The exposure of two LTPED devices with GGI = 0.375 (DH-1B) and GGI = 0.3 (DH-2B) to DH conditions (85% relative humidity and 85°C) for relatively short periods (60 and 80 hours respectively) has lead to similar results as typically reported literature for other CIGS-based devices [9] [10]. Usually a very strong increase in R_S in combination with a reduction in R_{Sh} leads to a reduction in FF and efficiency. The V_{OC} and J_{SC} show very small variations, usually smaller than 10%. The increased R_S is most likely explained by corrosion of the Mo-back contact and degradation of the ZnO layers as observed in optical microscopy. Additional effects might be water incorporation into the ZnO layer and a reduced type inversion at CIGS/CdS interface as reported in literature [11] [10] [12]. Corrosion of Mo is possibly also the explanation for the small difference in the EQE measured in untreated and DH-treated cells, where the conversion efficiency appeared to reduce for wavelengths in the range 750 nm $\leq \lambda \leq$ 1000 nm, as discolouration of the Mo due to oxidation would reduce the amount of light reflected back into the CIGS absorber. The reduction in R_{Sh} can most likely be ascribed to a combination of the degradation of active material between the TCO and back-contact, leading to formation of shunting paths. This was supported by observation in SEM. Also, formation of crystallites at the absorber surface after DH treatment suggests there might be significant Na diffusion during the

treatment, which might lead to a reduction in R_{Sh} if the Na reaches and passes through the depletion region [11].

For two cells on sample DH-1B an increase in R_{Sh} after DH was seen to cause a significant increase in efficiency. This observation might also be explained by degradation of TCO or oxidation of Mo at points where initially shunts are formed due to scribing. Another possible explanation is the diffusion of Na leading to an improvement of the doping profile in regions where the Na concentration was initially too high (i.e. a positive 'annealing' effect of the treatment). This appears likely in the case of the cell on which an improvement from 2.7% to 7.9% efficiency was observed mainly due to an increase in shunt resistance.

The complete removal of active material in the devices after short periods DH exposure as observed by SEM is most likely a degradation mechanism related specifically to the LTPED deposition technique. Incorporation of debris and large particulates into the absorber layer during the LTPED deposition can locally result in bad adhesion of the CIGS absorber. Such points in the absorber layer form weak spots, and were here observed to cause relatively fast, local degradation of the active material. Minimizing the size of debris reaching the deposited absorber layer would therefore be one of the main points to increase the durability of LTPED devices.

Conclusions and perspectives

During this thesis, CIGS-based TFSC's deposited using Low Temperature Pulsed Electron Deposition (LTPED devices) were investigated using AS, C-V, IV-T and V_{OC}-T measurement techniques with the aim of determining the typical apparent free carrier concentration, defect response and dominant recombination mechanisms. From comparison of the obtained results with those reported for CIGS-based solar cells in literature, an indication of the comparability of the performance of LTPED devices could be obtained and suggestions for further improvement could be given, as will be discussed in the current chapter. Part of the results of the measurements performed during this thesis were also useful as feedback in the processing of the LTPED devices, to control achieved doping levels and verify or compare different approaches in preparation.

As described in sections 2.2 and 3.2, the application of excitations such as illumination, bias or heat, as required for the above mentioned measurement techniques, is well-known to induce metastable behaviour in CIGS TFSC's [4] [5]. This was also observed in the LTPED devices studied during this thesis. Hence, an important prerequisite to obtain reproducible and reliable results from the above mentioned measurement techniques was a suitable methodology that would limit the influence of long-lived 'metastable' behaviour in the investigated devices and still allow relevant and reliable results to be obtained. The following conclusions could be drawn from the investigations during this thesis regarding the methodology for the experimental techniques:

- A reproducible initial 'relaxed state' (i.e. hardly depending on device history) is achieved by heating LTPED devices in the dark at 320 K for a time between 30 minutes to $\sim$1.5 hours, depending on the sample quality.
- The AS technique induces a negligible amount of metastability if no additional DC bias is used during the measurements. Highly reproducible results were obtained when repeating the measurements shortly after another if an amplitude in the range of $15 < \delta V < 35$ mV was used for the AC-bias and the frequency is limited to the range in which capacitance measurements can be performed accurately (this latter range depends on

sample quality, but usually was found to be 1 kHz $\leq f \leq$ 1 MHz), In the lower frequency range the lower sampling rate causes more noise in the measured capacitance, and in the higher frequency range artefacts related to series resistance and inductance are observed [111]. For the temperature, the range of 120 K $\leq$ T $\leq$ 320 K is usually reliable enough. Typically carrier freeze-out is observed for T $<$ 120 K.

- Using step sizes in the range of 10 K $\leq \Delta$T $\leq$ 20 K, sufficient resolution could be obtained in AS and IV-T measurements to construct Arrhenius plots.
- In nearly all cases, the junction capacitance was found to saturate at frequencies of $f \sim$1 MHz and temperatures of T$\sim$120 K, indicating accurate results can usually be obtained from C-V measurements under these conditions. Only for a small number of cells with low efficiency the measured capacitance already became inaccurate at 1 MHz so that a lower frequency needed to be used in the C-V measurements.
- The bias range in C-V measurements can be limited to -0.7 V $\leq V \leq$ 0.5 V to obtain relevant information.
- In V_{OC}-T measurements the constant heating of the sample by the applied illumination causes a large amount of noise at each measurements step (i.e. at each temperature). The best approach to obtain accurate results is by cooling down/heating up the sample under dark conditions with temperature steps in the range of 5 K $\leq \Delta$T $\leq$ 10 and noting the instantaneous value of the V_{OC} when quickly illuminating.
- Each of the C-V, I-V and V_{OC}-T techniques induces significant changes in device behaviour due to the applied bias or illumination at high temperatures. At lower temperature (T $<$ 200 K) the amount of induced metastabilities significantly decreases.

As discussed in more detail in Chapter 4, the results obtained using the developed methodology for performing AS, C-V, V_{OC}-T and IV-T measurements gave some important insights regarding properties of typical LTPED devices:

- Nearly all LTPED devices suffer from a high concentration of defects, as clearly observed in AS. Roughly estimated, $\sim$50-95% of the measured capacitance at low frequency and high temperature corresponds to defect response. Two different steps in capacitance

could usually be distinguished: a more gradual reduction at lower frequency and higher temperature (corresponding well with the often reported 'N2' step) and a sharper reduction at higher frequency and lower temperature (corresponding well with the often reported 'N1' step) [101] [6].. The 'N2' step would correspond to response from deep defects with broad distribution throughout the bandgap, while the 'N1' step would correspond to shallower defects with a more narrow distribution throughout the bandgap. A higher contribution from the N2 step seemed to be correlated to lower device performance, while the best devices showed a very clear distinction between the two steps. The centre of the distribution $\mathrm{E_d}$ could only be determined for the N1 step, and was found to vary significantly between cells: from $\sim$ 30 meV to $\sim$300 meV. From the results obtained during this thesis, no further conclusions can be drawn about the origins of this response in the material. In a small number of very low efficiency cells a single step in capacitance occurred at low frequency and high temperature, which would suggests a high concentration of deep defects with a relatively narrow distribution throughout the bandgap.

- From C-V measurements the depletion layer width in LTPED devices with reasonable efficiency was found to lie in the range of 0.5 µm $\leq \mathrm{w} \leq$ 0.8 µm. In this case, typically the apparent free carrier density was found in the range of $1{\cdot}10^{15}$ cm^{-3} $\leq \mathrm{N} \leq 10^{16}$ cm^{-3}, quite low in comparison with devices produced using other techniques (where a more common range would be 10^{16} cm^{-3} $\leq \mathrm{N} \leq 10^{17}$ cm^{-3}). This was expected to be due to difficulty in obtaining sufficient Na-doping at only 250°C processing temperatures when using the Na precursor layer. This also explains the quite common observation of completely depleted cells (i.e. with $\mathrm{w} \sim 2$ µm, $\mathrm{N} \ll 10^{15}$ cm^{-3}). Improving the achieved doping levels would still seem to be one of the most important points to aim for in further optimization of the LTPED technique.
- The dominant recombination mechanism was most often observed to be bulk SRH recombination, since from both V_{OC}-T and IV-T measurements activation energies of $\mathrm{E_a} \sim \mathrm{E_G}$, i.e. 1.1-1.2 eV. However, it should be noted that also in the case of interface recombination in presence of a large CBO, $\mathrm{E_a} \sim \mathrm{E_G}$ might be observed. In some cases much

lower activation energies (down to ~0.7 eV) most likely indicated a significant contribution of interface recombination. The lower values in E_a were always found to correspond to a lower device performance. Higher values of E_a, of ~1400 meV were also observed, which was expected to be due to a contribution of interface recombination in combination with a high CBO.

Investigations of LTPED devices with an incorporated layer of the 'Ordered Defect Compound' (ODC) phase of CIGS (Chapter 5) showed no clear effects of presence of this layer in the applied measurement techniques. The clearest variation for thick ODC-layers was found to be an increase in the R_{Sh} in dark conditions, with a strong reduction (up to 95%) when illumination was applied.

However, an apparent increase in both the R_S and R_{Sh} was observed for thicker ODC-layers, with a drastic reduction (up to 95% for the R_{Sh} at application of illumination. The proposed mechanism behind this effect was an illumination dependent conductivity in the ODC-layer, with low conductivity in the dark and high increase in conductvity under illumination (possibly due to photo-excitation of defects in the ODC-layer, as suggested in [8]). Deposition of an ODC-layer on top of the standard CIGS absorber might then lead to increased R_{Sh} by covering shunting paths, while the increased conductivity under illumination leads to the observed drop in R_{Sh}. Also observed for thicker ODC-layers, was a drop in the conversion efficiency at longer wavelength, suggesting superficial deposition of ODC-phase material might also influence the material deeper into the bulk of the absorber, and hence interdiffusion between both phases might take place during ODC-phase deposition or post-deposition annealing. No beneficial effects was observed in the performance of any of the devices.

Accelerated Lifetime Tests (ALT's) were performed on two LTPED devices by placing them in Damp Heat (DH, 85% humidity and 85°C) for short amounts of time (60-80 hours). From these experiments similar results were obtained as those already reported in literature for more standard CIGS-based devices, with an increase in R_S and a decrease in R_{Sh} due to degradation of TCO and Mo-layers. Notably, in two cells on the investigated LTPED devices a significant increase in performance was observed. This was attributed to an improvement in the initial Na-doping

profile by storing the samples at high temperatures (i.e. diffusion promoted by the higher temperatures). In addition to the typically reported degradation mechanisms, a mechanism more relevant to LTPED devices appeared to be 'crater' formation as parts of the absorber were found to detach within the short period of DH treatment. This was explained as an effect related to the presence of larger particulates in the absorber bulk which are incorporated during LTPED deposition [1]. These particulates lead to a loss of adhesion of the material deposited on top. Reducing the incorporation of particulates in LTPED would then seem to be the most important aim to further improve the durability of LTPED devices.

The main results from this thesis for typical LTPED devices discussed above don't indicate very big differences in the typical defect response and recombination mechanisms, but mainly relatively low doping even in the best performing devices, when compared to otherwise prepared CIGS-based TFSC's. The uniformity of most lab-scale devices was also still relatively low. This suggests the most important limiting factor in the performance of LTPED devices is achieving sufficient Na-doping, which very probably is explained by the low processing temperature of 250°C. Achieving controlled and uniform diffusion of Na through the absorber at these temperatures might require alternative approaches, although until now attempts such as incorporation of Na into CIGS target or application of multiple NaF precursor layers haven't allowed much improvement [54].

The results that have been obtained at IMEM-CNR in the past years by application of the LTPED technology for preparation of CIGS based devices has proved it to be a promising technique for single stage depositions at low temperature [113] [126] [1]. This technique was also proven to be easily adaptable for deposition onto a wider range of substrates and for the deposition of absorbers with various CIGS compositions and Ga-profiles. Although the low processing temperatures used in LTPED could lead to significant cost reduction and deposition on a wider range of materials than in conventional deposition techniques, the disadvantages of this low deposition temperature are a lower amount of diffusion, especially important to achieve sufficient doping. Hence, it would appear to be a very promising technique if performed in highly controlled deposition conditions, and with alternative approaches to Na-doping.

Appendix A. Measurement techniques

This appendix contains a short description of the different measurement techniques that were used during this thesis and weren't already treated in Chapter 3.

STANDARD CURRENT-VOLTAGE (IV)

As was already explained in Chapter 0 (section 1.2.2) the most important performance parameters of solar cells are derived from current-voltage (IV) measurements. The majority of IV-measurements presented in this thesis were performed at IMEM-CNR using a Keithley 2635 connected to the investigated sample in a two-point probe configuration and interfaced with a computer running an IV-measurement program. The bias was swept in the desired range (typically $-0.5 \leq V \leq 1$ V in steps of 15 mV) while limiting the current. Measurements were performed under standard test conditions (STC) with the sample kept at 25°C and using an ABET Sun 2000 class A solar simulator to illuminate with the AM 1.5G spectrum at 1000 W/m^2. For dark measurements the sample was covered with a black cloth or other black cover.

At Solliance a similar setup was used, with a Keithley 2400 in a four-point probe configuration, and a TriSOL class AAA solar simulator for illuminated measurements.

EXTERNAL QUANTUM EFFICIENCY (EQE)

The external quantum efficiency (EQE) gives an indication of the conversion efficiency of the investigated device as function of the wavelength of the incident light. This can be determined by measuring the produced photo-current at short-circuit conditions at monochromatic illumination (i.e. $J_{SC}(\lambda)$) for a desired range of wavelengths, depending on the bandgap of the material and the absorption in the buffer layers. For CIGS typically a range of $350 \text{ nm} \leq \lambda \leq 1200$ nm is sufficient, as shown in Figure 70. The EQE is then defined as the ratio between the short-circuit current $dJ_{SC}(\lambda)$ and the known photon flux $d\Phi(\lambda)$ (cm^{-2}s^{-1}) for each wavelength interval $d\lambda$:

$$EQE(\lambda) = \frac{1}{q}\frac{dJ_{SC}(\lambda)}{d\Phi(\lambda)}$$

In an ideal solar cell one electron-hole pair would be produced and collected for each photon satisfying $E \geq E_G$. However, in any real device the effects of reflection, absorption and recombination limit the conversion efficiency as well as the carrier collection efficiency at each wavelength, leading to values for the EQE well below the ideal. As indicated in Figure 70, the mechanisms limiting the conversion efficiency will be different depending on the incident wavelength, so that analysis of the EQE can give important insights into the main reasons for limited efficiency in a solar cell [127].

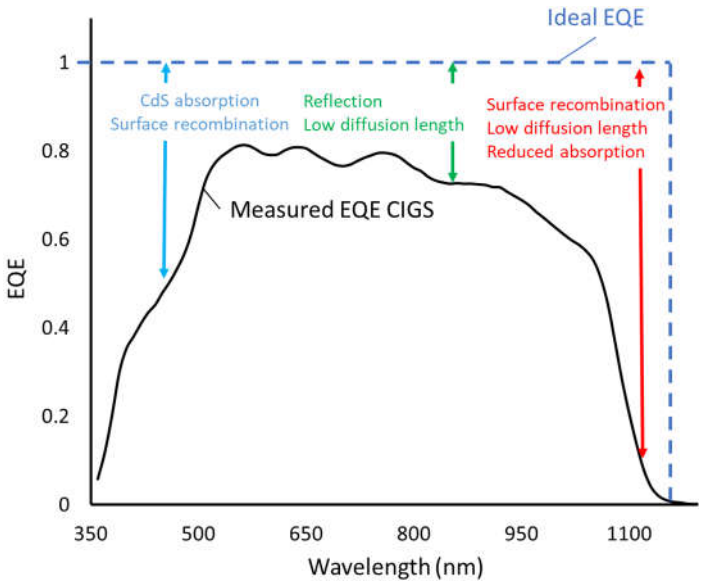


Figure 70 Indication of theoretically ideal EQE (blue dashed line) and experimentally observed EQE (black solid line) of a CIGS device. Possible origins of the losses for the short wavelength (blue), medium wavelength (green) and long wavelength (red) are indicated. Adapted from [128]

Two different setups were used for EQE measurements during this thesis. At IMEM-CNR, the light from the same ABET Sun 2000 class A simulator was filtered using 16 different narrow band filters from Thorlabs with passbands in the range of 350 nm to 1100 nm ($\pm$ 2 nm in each case). The filters were placed onto a small opening in a box enclosing the sample, which was otherwise completely screened from ambient light. By measuring the J_{SC} at each wavelength the EQE could be calculated. A Si- reference cell with known spectral response was used for calibration before

each measurement. In the setup at Solliance light from a 100-Watt Philips Halogen lamp was passed through an Omni-λ 3009 monochromator with pass-band filters spaced at 10 nm in wavelength, a Thorlabs optical chopper tuned at 66 Hz and an optical system that focused the monochromatic light into a small area beam. Using a Lock-In Amplifier, the J_{SC} was measured automatically at each wavelength in a computer-controlled setup. For calibration, a Si reference cell was used for the 350-990 nm region and a Ge reference cell was used for correction of the 1000-1200 nm region.

LOCK-IN THERMOGRAPHY

Lock-In Thermography (LIT) is a useful, non-destructive technique for investigation of presence and location of spatial defects (in particular shunts) in a device. The LIT results shown in Chapter 6 were obtained from an illuminated LIT setup at Solliance in which the sample was measured under open-circuit conditions (uncontacted) and illuminated using a pulsed light source under constant monitoring of the surface temperature using an infrared camera ('V_{OC}-ILIT'). In this approach, charge carriers excited by the illumination either gradually lose energy as they relax back to equilibrium, thus causing moderate homogeneous heating of the sample, or they give rise to currents in regions with low series resistance thus causing significant Joule heating [129]. Under open circuit conditions, mainly vertical currents due to shunts can be expected to lead to currents and corresponding Joule heating. Hence, regions showing large increase in temperature are expected to correlate to shunts in the device, as shown in Figure 71.

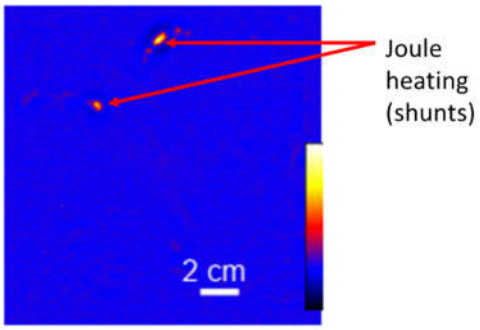


Figure 71 Example of VOC-ILIT picture, as reported in [129]. While on most of the sample surface no significant variation in temperature is observed, small red/white spots can be correlated to shutns.

In the setup used at Sollicance two 320 Watt infrared LED panels were used to periodically illuminate the sample. The surface temperature was continuously monitored using an ImageIR 8300 camera connected to a Lock-In Amplifier. The images presented in Chapter 6 were obtained using a Lock-In frequency of 25 Hz, a camera frequency of 100 Hz at 4 frames per period, and a measurement time of 500 seconds. The entire setup was enclosed inside a cabinet to prevent ambient light from reaching the sample.

SCANNING ELECTRON MICROSCOPY (SEM)

Scanning Electron Microscopy (SEM) can be used to determine various properties of the sample surface or its cross-section, such as layer thickness, local composition, topography and local surface potential. In SEM an electron beam is accelerated toward the sample and focused onto an area < 1 nm using electromagnetic lenses. The penetration depth of the incident electron beam into the sample can be varied by changing the acceleration voltage of the beam. Due to the incident electron beam, electrons are scattered from the studied sample at various angles and energies, which can be analysed to obtain information about composition, topology and surface potential. Additionally, X-rays emitted by the sample can be analysed using an energy dispersive X-ray (EDX) detector to obtain more accurate information about the material composition in different regions. Scanning the investigated surface with the electron beam results in a 2D image with the above information [130].

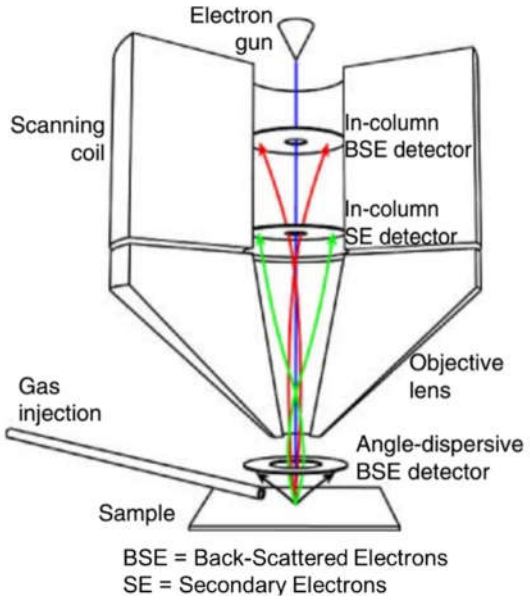


Figure 72 Typical configuration of SEM setup, as reported in [130]

The SEM results presented in this thesis were used to determine different layer thicknesses, structural properties and compositions at different points on the sample surface (Chapter 6 and

Appendix C. CdS photoconductivity). These results were obtained from both setups at IMEM-CNR and Solliance. At IMEM-CNR a Philips 515 was used at 20kV acceleration voltage. At Solliance a JEOL JSM-6100LA InTouchScope with EDS and Backscatter detector was used .

RAMAN SPECTROSCOPY

Raman spectroscopy can be used to obtain information about phases and crystal structures of a studied sample. The principle behind the measurement technique is analysis of the non-elastic (or 'Raman') scattering of the incident laser light at frequency ω_0. Crystal vibrations (phonons) cause a shift in the photon frequency such that light is scattered at frequencies $\omega_0 \pm \delta\omega$, where the Raman shift $\delta\omega$ (expressed in inverse wavelength, cm^{-1}) equals the phonon frequency inside the studied material. Each crystal structure has a specific number of normal vibrational modes at different wavelengths, so that identification of the Raman shift allows to distinguish different structures and their properties [131]. For this thesis, results obtained using a micro-Raman configuration were used, in which the incident laser beam is focused in a small volume to allow analysis at different depths from the surface with resolutions up to ~100 nm in thickness**.** Using the micro-Raman technique, the GGI and phase of CIGS thin films can be studied as function of depth, as shown in Figure 73 [132].

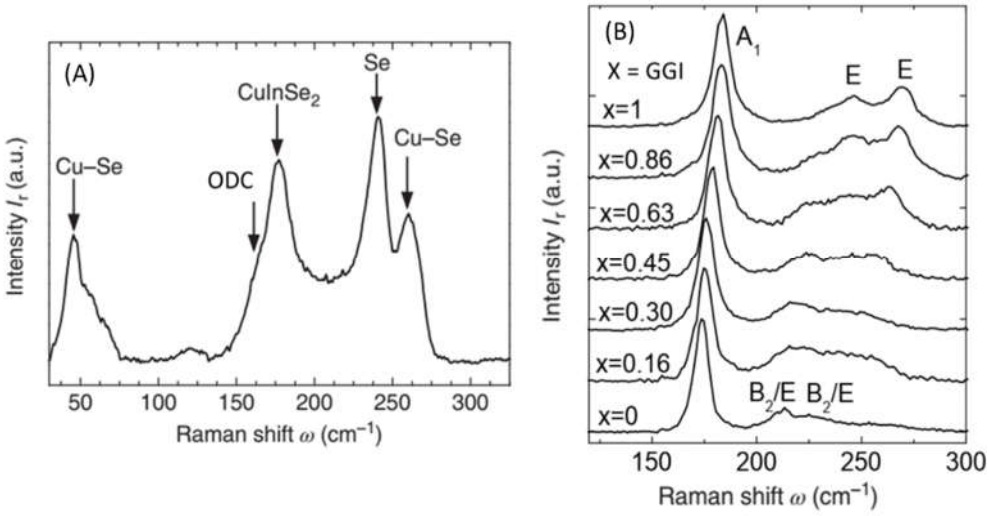


Figure 73 Images illustrating the suitability of Raman spectroscopy to distinguish different phases (A) and obtain compositional variations with depth (B). In (B), A1 corresponds to a vibrational mode of the Se atoms, while B2

and E correspond to mixed vibrational modes of the anions with cations. B_2/E indicates mixing of the B_2 and E modes. Figures adapted from [131] (a) and [132](b)

For this thesis, Raman results were used to confirm presence of ODC-phase material in LTPED devices, which is observed from a shoulder appearing at ~150-160 cm^{-1} next to the chalcopyrite peak at 174-184 cm^{-1} [132] (see Chapter 5). The setup used for Raman at IMEM-CNR consisted of a Horiba Jobin–Yvon Labram micro-Raman system equipped with a Olympus BH-4 confocal microscope used at 100X magnification. The spectrometer in the Raman setup contained a 623.8 nm, 20 mW He-Ne laser incident on a 256x1024pixel CCD detector through a 1800 grooves/mm grating and density filter wheel. The spectrometer was calibrated using a Si reference before each measurement.

OPTICAL MICROSCOPY

The optical microscopy results shown in Chapter 5 were obtained at Solliance using a Leica Laborlux 12 Me.

Appendix B. CIGS/Mo interface

The ohmic contact between the CIGS-absorber layer and Mo back-contact in CIGS-based devices is usually attributed to presence of a thin $MoSe_2$-layer formed during absorber depositions for which the substrate temperature exceeds 410°C, (see Chapter 3 and reference [13]). Since the substrate temperatures used in LTPED-deposition are significantly lower (i.e. 250°C-300°C rather than 410°C), the formation of a (near) ohmic contact at the CIGS/Mo interface in LTPED devices is apparently achieved by a different mechanism [1]. It is suspected that in this case, deposition of the NaF precursor directly at the CIGS/Mo interface results in a highly conductive P^+ CIGS-layer leading to formation of a kind of tunnel junction.

In a number of low performance LTPED-devices rectification opposite to that of the main diode was observed. Following the above hypothesis, formation of such a non-ohmic contact might be an effect due to insufficient Na-doping. The experiments presented in here were intended to test

the role of Na for obtaining a good ohmic contact at the CIGS/Mo interface in LTPED devices. This was done by investigating samples with and without Na precursor, as explained in more detail below.

EXPERIMENTAL APPROACH AND RESULTS

Two samples with slightly different architectures were used for the investigations, as shown in Figure 74. Both samples were prepared using the commercial SLG/Mo substrates also used for standard LTPED devices. One sample was prepared without the standard NaF precursor layer (sample A), the other (sample B) was prepared with NaF precursor layer. For both samples, a CIGS layer was deposited using the standard approach for LTPED (see Chapter 4). Au was chosen as front contact, and deposited in each case by thermal evaporation. In sample A the Au deposition was performed directly after finishing the CIGS layer, i.e. without any pre-treatment applied to the CIGS surface. After the observation of rectification on this sample in both forward and reverse bias direction (see Figure 74) for sample B it was decided to apply treatments of the sample either before or after the Au deposition. To achieve this, the sample was cut into two parts, B1 and B2, with a different treatment applied for each sample. On sample B1 the Au-contacts were evaporated directly after the CIGS deposition, after which the sample was annealed in N_2 atmosphere at 150 °C, 200 °C and 250 °, for 30 seconds, 1 minute and 1 minute respectively. This approach was aimed at achieving a better diffusion of Au into the CIGS layer to promote formation of an ohmic contact. Sample B2 was subjected to a 10-minute NH_3 bath at 80 °C before Au-deposition to remove possible contamination from the CIGS surface. No further treatment was performed on sample B2 afterwards.

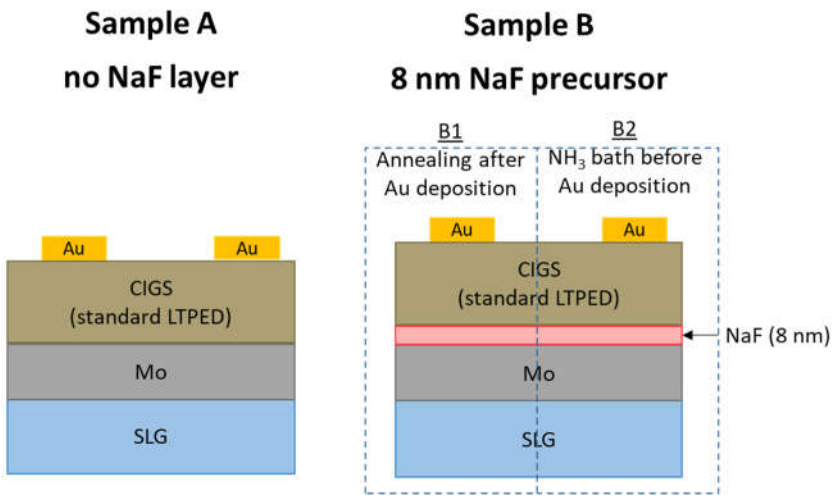


Figure 74 Architectures of samples A and B used for investigating the role of Na on the ohmicity at the CIGS/Mo contact. Sample A wans't treated before or after Au deposition, which resulted in non-ohmic contacts (see text). Sample B1 was annealed in N_2 atmosphere (30 seconds 150°C, 1 minute 200°C and 1 minute 250 °C) after Au deposition, and sample B2 was pre-treated in an NH_3 bath (10 min at 80°C) before Au deposition.

To study the behaviour of the contacts IV measurements in the dark and under illumination for different temperatures were performed on each sample. On sample A rectification was observed both in the dark and under illumination, as shown in Figure 75. The polarization was found opposite to the forward direction of a standard CIGS based solar cell, indicating a back-contact barrier at the CIGS/Mo interface. At room temperatures a high series resistance ($R_S \sim 30\ k\Omega$) was observed at forward biases in the range of $0.2 \leq V \leq 0.7$ V. The dark current became strongly inhibited at lower temperature, dropping to $I < 1$ µA for $T < 255$ K. Under illumination a photovoltaic effect was observed, with $V_{OC} \sim 80$ mV and $I_{SC} \sim 1.5$ µA at room temperature. A rollover effect was observed for temperatures $T < 265$ K under illumination. The very low current observed in this sample indicates a high back-contact barrier. From the photovoltaic effect it follows that a depletion layer with non-negligible width is formed at the interface. The roll-over effect indicates an additional barrier at the opposite contact (i.e. CIGS/Au interface) which can be overcome at room temperature but starts to limit the current at lower. As explained above, this barrier at the CIGS/Au interface in sample A was suspected to originate from contamination of the CIGS surface before Au contact deposition.

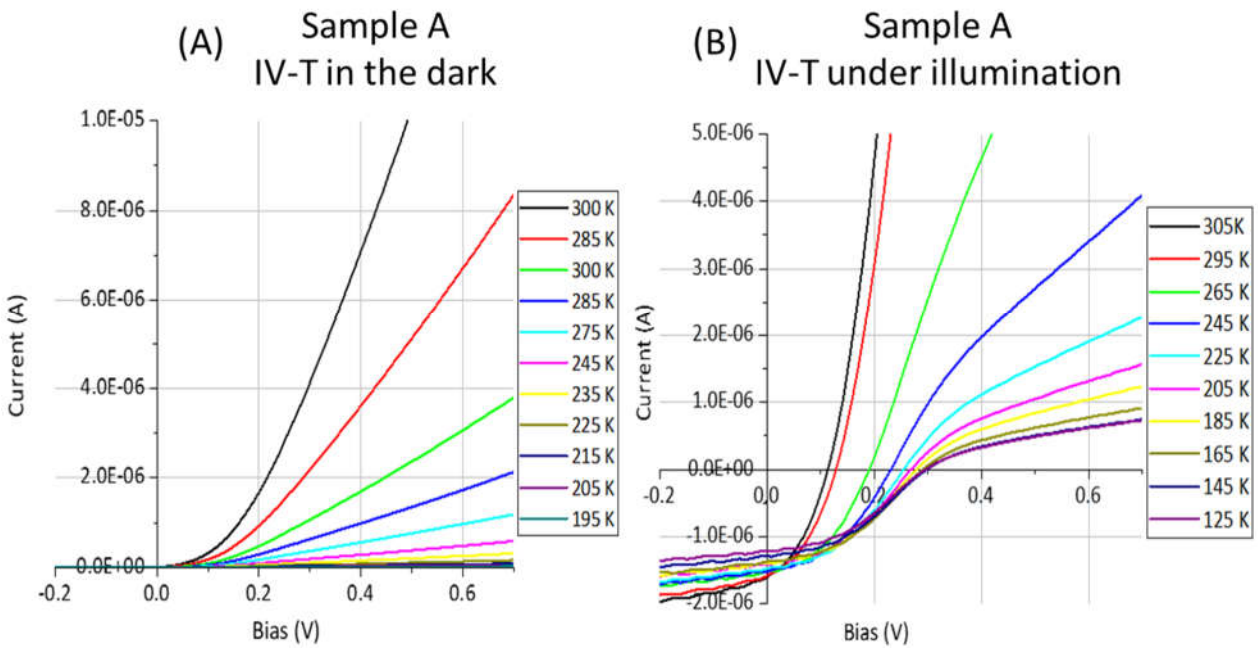


Figure 75 IV characteristics measured on sample A (SLG/Mo/CIGS/Au without NaF precursor and no pre-treatment before evaporation of the Au contact contacts). (A) Dark IV-T characteristics. (B) IV-T characteristics under illumination (AM 1.5 G, 1 sun).

On sample B1 (SLG/Mo/NaF/CIGS/Au architecture with annealing applied after evaporation of the Au contacts) significant non-uniformity was observed across the sample, with some contacts showing ohmic behaviour at first measurement while other contacts initially showed highly rectifying behaviour, as shown in Figure 76. At some contact the rectifying behaviour disappeared and turned into ohmic behaviour after application of a sufficiently high bias ($V >$ 1.5 V). The highest amount of rectification on sample B1 was in the same direction as for sample A, i.e. opposite to the forward direction of a standard CIGS-based device, indicating again a barrier at the CIGS/Mo interface at some points. A slight photovoltaic effect was also present, but much smaller than what was observed in sample A (see Figure 76(A)).

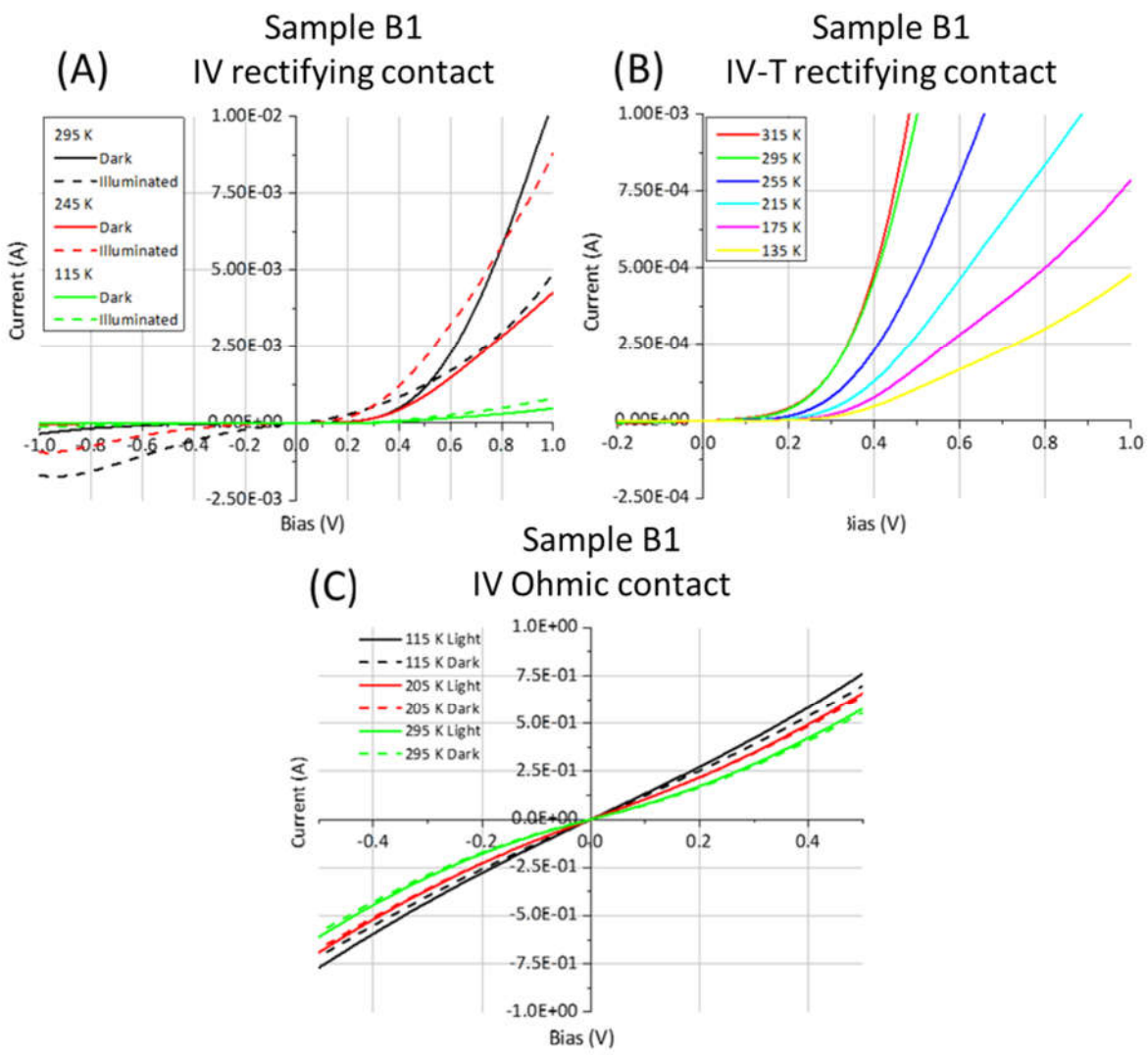


Figure 76 IV characteristics measured on sample B1 (SLG/Mo/NaF/CIGS/Au, annealed after evaporation of the Au contacts) (A) I-V characteristics measured in the dark and under illumination on one of the rectifying contacts. (B) Dark IV-T characteristics for the same contact as for which IV curves are reported in (A). (C) I-V characteristics for a nearly ohmic contact on the same sample.

The non-rectifying contacts showed series resistances ranging from ~5-60 Ω. The contacts on sample B1 showing lowest R_S (in the range 5-7.5 Ω) showed hardly any dependence on light and temperature (Figure 76(B)). Observation of ohmic contacts on the sample B1 suggested addition of the NaF precursor layer and the annealing after Au deposition did significantly improve the contacts at the CIGS/Mo interface and CIGS/Au interface respectively. Absence of a significant

roll-over effect in the dark IV-T curves (Figure 76(B)) was considered as an indication that in particular the Mo/Au interface barrier had been greatly reduced. The non-uniformity observed across the sample in contact quality could be related to of non-uniform diffusion of both Na and Au into the absorber layer during the short annealing times. Possibly, at the contacts where ohmicity was observed after application of a high forward bias, the barrier at the back-contact was negligible while a barrier was still present at the front contact due to the inability of the Au to diffuse through the contamination on the CIGS surface (e.g. a thin oxide layer). By application of high forward bias the layer causing a barrier at the CIGS/Au interface might be damaged due to the high electric field, resulting in (nearly) ohmic contacts. Observation of contacts where rectification and a photovoltaic effect were still present might be explained due to insufficient Na-diffusion into the CIGS layer, leading to a lowering but not to disappearance of the back-contact barrier.

The IV characteristics of sample B2 (SLG/Mo/NaF/CIGS/Au, with 10-minute NH_3 bath at 80°C before Au deposition) are shown in Figure 77. As clear from the figure, on this sample the most ohmic behaviour was observed. Still non-uniformity in the characteristics were found, as clear from comparison of Figure 77(A) and (B), where the contacts appear ohmic with very low R_S, and Figure 77(C) where a barrier is observed in both reverse and forward directions. However, upon comparison of Figure 77(C) with Figure 75(B), the series resistance in forward direction is clearly reduced on sample B2 with respect to that on sample A. This indicates the etching in NH_3 did lead to a reduced barrier between at the CIGS/Au interface. No clear photovoltaic effect was observed, but illumination was seen to cause a reduction in the R_S at higher forward bias.

For the contacts showing highest ohmicity, R_S values in the range of 2-16 Ω were found. The very low values of R_S, similar to typical values of the Mo back-contact, suggested in this case the CIGS layer had become shunted.

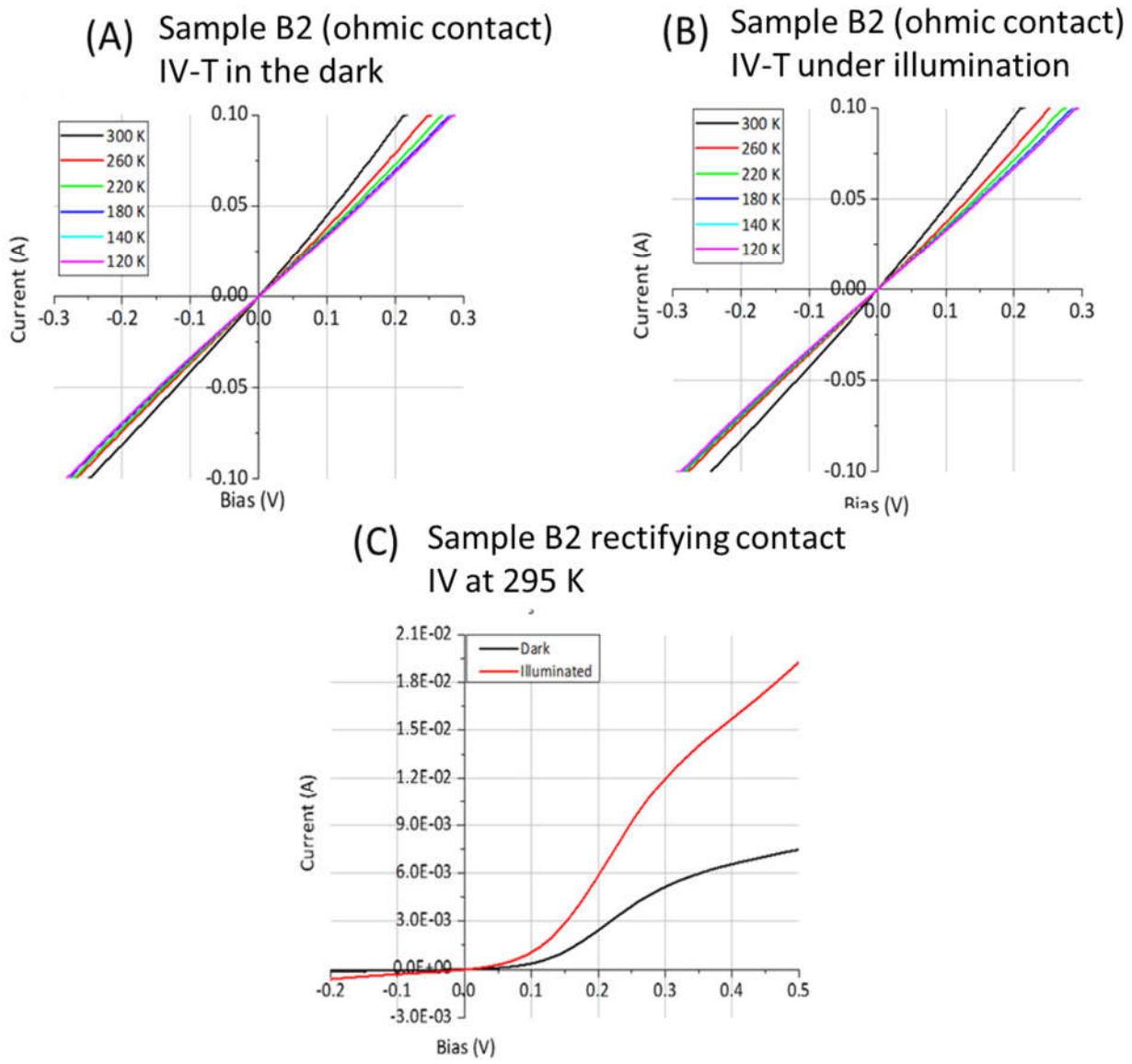


Figure 77 Different IV-characteristics observed across sample B2 (SLG/Mo/NaF/CIGS/Au, with 10-minute NH_3 bath at 80°C before Au deposition). (A) Dark IV-T on an ohmic contact. (B) IV-T under illumination on the same contact for which results are reported in (A) contact. (C) IV performed at 295 K in the dark and under illumination.

CONCLUSIONS

In the presented results the occurrence of a barrier at the Mo/CIGS interface with photovoltaic effect (opposite to in samples without NaF precursor was clearly observable. The deposition of the NaF precursor was observed to lead to non-uniform effects across the sample, with only a

reduction in the photovoltaic effect of the barrier in some cases, and a complete disappearance of the barrier in other cases. Such non-uniformity of the effects of the deposition of a NaF precursor at low temperature could explain the high non-uniformity in the performance of typical LTPED devices, where often low performance corresponds to low doping (see Chapter 4). Although no strong conclusions can be drawn from these results due to the small number of samples used and the additional effects of non-ohmic contacts at the CIGS/Au interface, it would appear that in absence of an NaF layer a diode is formed at the CIGS/Mo interface which would be detrimental to device performance. The application of an NaF precursor layer appears to be beneficial to allow better contact at the CIGS/Mo interface, although an ohmic contact isn't guaranteed, possibly due to inhomogeneous diffusion into the CIGS absorber.

Appendix C. CdS photoconductivity

Various metastable effects occurring in CIGS-based devices are related to the application of illumination causing changes in the conductivity properties in the device, attributable to various effects [133] as also discussed in Chapters 2 and 3. In Chapters 4 and 5 the resulting temperature dependence of the series resistance and shunt resistance in LTPED devices was shown.

A common explanation found in literature for the origin of the 'red-kink effect' (referring to a loss in FF under red light illumination, see Chapter 2) is the presence of deep acceptors in the CdS buffer which compensate the donors and result in a low conductivity in the dark [122]. At application of white light illumination the ionized acceptors would capture holes, thus leading to a reduction in the compensation of the CdS buffer, and increased carrier collection from the solar cell. This was also found to be a feasible explanation from simulations [74]. In this appendix, some results from experiments are presented in which the occurrence of photoconductivity in CdS layers was investigated, to obtain an indication of whether such effects would be likely to play a role in finished LTPED devices.

EXPERIMENTAL APPROACH

The sample architecture used for the investigations is shown in Figure 78.

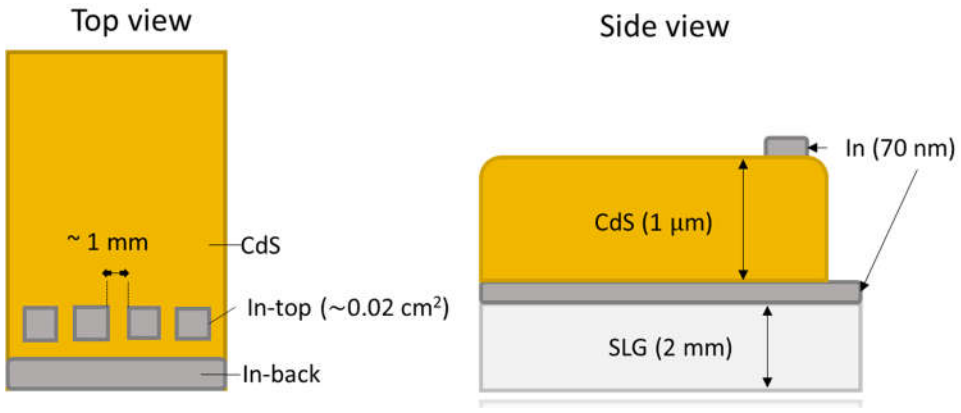


Figure 78 Architecture used for investigation of the dark and illuminated currents of CdS deposited by standard CBD as performed at IMEM-CNR. As front and back-contacts for CdS Indium (In) was found to be a suitable material, as suggested in [134]**.**

The Indium (In) back- and front-contacts were deposited by thermal evaporation. The thick (~ 1 μm) CdS layer was deposited through multiple steps of the standard CBD approach used at IMEM-CNR (see Chapter 4). The square front-contacts were evenly spaced by ~1 mm and had an area of ~0.02 cm^2. As reported in literature for the case single crystal CdS [134], In allowed to achieve good ohmic contacts. The current between front and back contacts was measured both in the dark and under illumination as function of time, under application of 0.5 V bias.

RESULTS

In Figure 79 the results of two consecutive dark measurements on the sample are reported, performed between one of the small square front-contacts and larger In back-contact. The measurements show the apparent high resistivity of the CdS, with the lowest resistance observed as ~180 Ω, indicating resistivities in the range of ~10-100 kΩ cm. Application of 0.5 V bias in the dark was found to lead to a very moderate increase in the current by less than 0.5% in 70 seconds, with no sign of saturation within the period of measurement. Also shown in Figure 80 are the current transients obtained when measuring the current as function of time under illumination. The first measurement was performed directly after the final dark measurement shown in the top graph of **Error! Reference source not found.**, and shows a clear response to illumination.

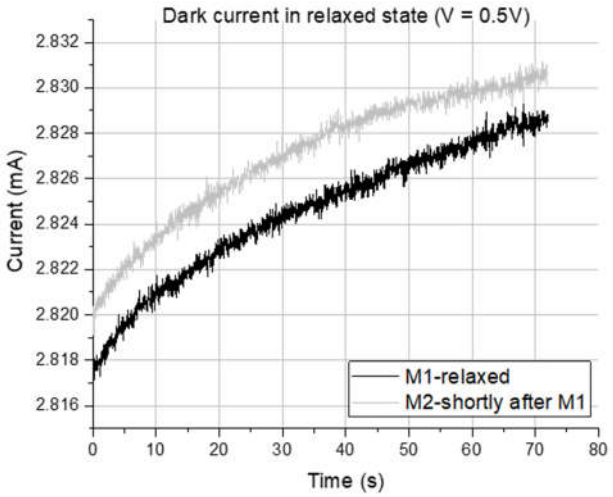


Figure 79 Dark currents measured in sample A (In/CdS/In) in the relaxed state (black line) and shortly after the first measurement (red line).

In the dark current in the relaxed state shown in Figure 79 is compared to two additional measurements during which illumination was applied for 50 seconds and ~250 seconds, with the sample left in the dark again for approximately 1 min in between. No saturation was reached in either case, while the current gradually increased by ~5% in 50 seconds and 9% in 250 seconds. Notably, the dark current in the second illuminated measurement is still higher than in the first, without showing signs of further relaxation.

In **Figure 81**, the dark current measured very shortly after the 250 seconds illumination still clearly shows a decreasing trend. After 10 minutes, the dark current is observed to increase again at application of the 0.5 V bias but is still higher than the current in the relaxed state. Also shown in **Figure 81** is the current measured during 10 minutes of illumination. Here, no stabilization was achieved within the time-frame of measurement.

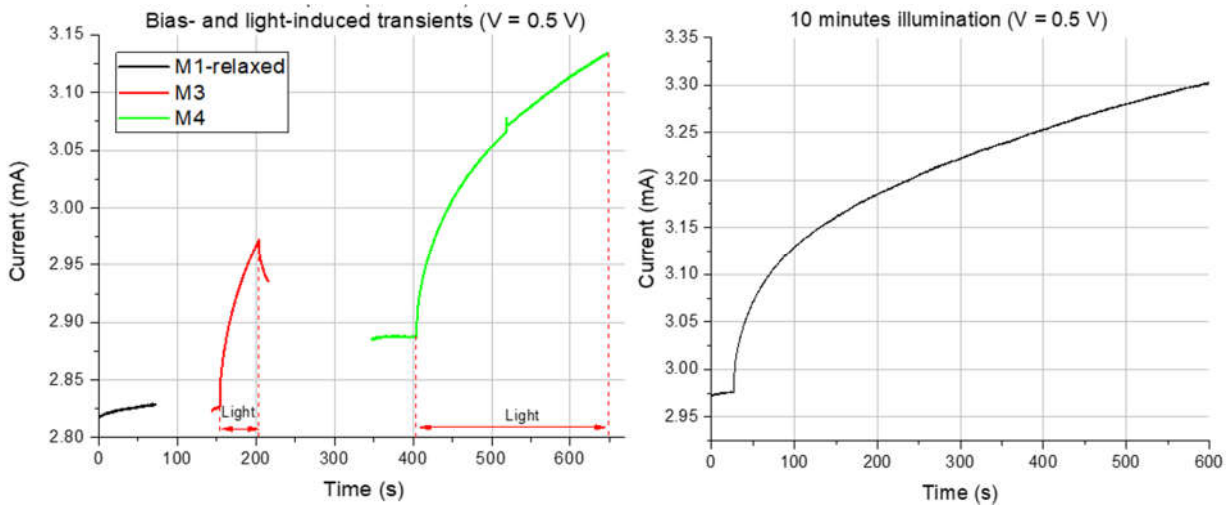


Figure 80 Currents measured for sample A (In/CdS/In). On the left, comparison between the dark current measured in the relaxed state (black line), during 50 seconds of illumination (red line) and during 250 seconds of illumination (green line). On the right, the current measured during 10 minutes of illumination.

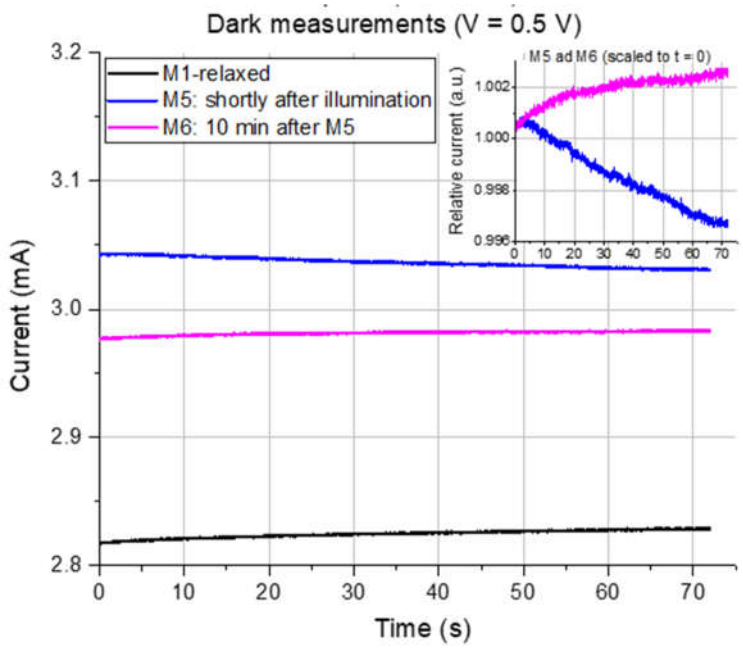


Figure 81 Currents measured in sample A (In/CdS/In). Comparison of the dark current in the relaxed state (black line), dark current shortly after the final illuminated measurement shown in Figure 80 (blue line) and 10 minutes later (cyan line). The inset shows both dark measurements M5 and M6 relative to their initial value at t = 0, to indicate the different trend with time.

CONCLUSIONS

The reported sample has much higher resistivity than would be expected for normal CdS used in LTPED devices. Hence, the observed effects of the slow transients in current increase at application of bias and illumination might be expected to be amplified in comparison to the behaviour in standard devices. The strong effect of illumination and bias most likely indicates the response of high defect concentrations, leading to the compensation of this particular sample and hence the high resistivity. Assuming that the same type of defects are also present in much lower concentrations in good quality CdS, these results suggest they might indeed play an important role in slow metastable behaviour observed in the LTPED devices studied during this thesis.

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Like many people I decided to go abroad for my PhD, like not so many people I chose Italy as my destination. During these past three years of performing my thesis at the IMEM-CNR in Parma I experienced a lot of challenges that I suppose are typical for foreigners living in Italy. But all the while I kept being amazed by the amount of hospitality, helpfulness and friendliness I encountered from the people I met. This quickly made Parma feel like home to me, and I feel very thankful to so many people for this, which is why these acknowledgements are perhaps a bit long.

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