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**Advanced Modelling, Optimized Design and Innovative Control
Strategies for Dual Active Bridge DC-DC Converters for Efficient
Electric Vehicle Fast Charging**

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Electric Vehicle Fast Charging**

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*Dedicated to God Almighty and to my wonderful parents MR/MRS NKEMBI.
Also, this work is dedicated to all those who will find it useful in one way or the
other*

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Abstract

The rapid rise in Electric Vehicles (EVs) as a viable solution for reducing greenhouse gas emissions necessitates the development of robust, efficient, and versatile fast-charging infrastructure. Charging infrastructures are typically comprised of power converters that enable efficient and safe energy transfer. The AC-DC converters are responsible for rectifying grid voltage into a stable DC output while ensuring power quality and grid compliance. Following this, the DC-DC converters manage the charge and discharge currents and voltages of the EV batteries, ensuring they meet the specific requirements of the batteries and maintain safety, reliability, and performance throughout the charging process.

This thesis specifically delves into the design, control, and optimization of Dual Active Bridge (DAB) DC-DC converters, which are pivotal for high-power EV charging stations due to their soft-switching capabilities and adaptability to various battery chemistries and power requirements. A central challenge in this domain, however, is ensuring smooth transitions between different charging stages, such as Constant Current (CC) and Constant Voltage (CV) modes, which are essential for maintaining optimal battery health and charging efficiency.

The initial investigation explores the dynamic operation of DAB converters, introducing an improved Fourier series-based Generalized Average Model (GAM) that incorporates the effects of parasitic resistances in the output filter capacitors. This model enhances the accuracy of simulations by providing a more realistic depiction of the converter's dynamic response. Complementing this model, a novel control strategy combining feedforward and feedback mechanisms is proposed. This strategy employs Single Phase Shift (SPS) modulation to facilitate a seamless transition between CC and CV charging modes, crucial for maintaining performance during the different stages of battery charging, mitigating the typical issues of undershoot and overshoot during mode transitions.

Building on this foundation, the research introduces an innovative control method that integrates droop-based techniques with a sophisticated Linear Active Disturbance Rejection Control (LADRC) system. This combination is again applied to a single-phase shift-modulated DAB converter, addressing the critical issue of seamless transition between charging stages. The LADRC system enhances the converter's robustness against input voltage fluctuations and load variations, thereby stabilizing the charging process. Additionally, the proposed control method reduces the peak input current, allowing for the use of lower-rated components, which contributes to a reduction in the overall cost and complexity of EV charging stations.

The thesis further explores the use of advanced modulation techniques, specifically Dual-Phase Shift (DPS) modulation, which enhances the soft-switching capabilities of DAB converters. DPS modulation is particularly effective in optimizing power conversion efficiency, yet it requires

complex optimization of internal and external phase shift angles. To address this, a three-loop LADRC control system featuring decoupled dq vector control of the inductor current is proposed. This innovative control architecture not only facilitates optimal phase shift determination but also lowers the peak input current, making it feasible to use lower-rated switches and reducing system costs.

Moreover, a comprehensive modelling, control and performance comparison of various modular DAB topologies under different performance metrics such as power conversion efficiency, system losses, circulating currents and ripple characteristics is conducted. The results indicate that modular input parallel output parallel DAB converters provide superior efficiency, especially under conditions of variable load. This modular approach also allows for reduced voltage and current stress on power switches, promoting the use of lower-rated, more cost-effective components.

Addressing the challenges of ensuring power balance among modules and minimizing the number of sensors required, the thesis proposes an improved extended state observer. This observer mitigates the inaccuracies introduced by traditional observers and enhances the system's transient performance. Furthermore, an adaptive module-shedding technique is also developed to dynamically adjust the number of active converter modules based on real-time power demands, significantly improving power transfer efficiency across a wide range of operating conditions during the battery charging process.

The innovations presented in this thesis offer a holistic approach to addressing the multifaceted challenges of fast EV charging, emphasizing the importance of efficient power conversion, system robustness, and cost-effectiveness. These advancements are expected to play a crucial role in supporting the global shift towards sustainable transportation solutions.

Keywords: *Electric Vehicles (EVs), Dual Active Bridge (DAB) Converter, High-Power Charging Infrastructure, Dynamic Operation, Generalized Average Model (GAM), Constant Current (CC)-Constant Voltage (CV) modes, Single Phase Shift (SPS) Modulation, Feedforward and Feedback Control, Linear Active Disturbance Rejection Control (LADRC), Dual-Phase Shift (DPS) Modulation, Decoupled dq Vector Control, Modular DAB Topologies, Power Conversion Efficiency, Adaptive Module-Shedding Technique, Extended State Observer, Input Voltage Fluctuations, Load Variations, Cost-Effective Components, Soft-Switching, Power Balance, Numerical Simulations, Battery Charging.*

Sommario

Il rapido aumento dei veicoli elettrici (EV) come soluzione valida per ridurre le emissioni di gas serra richiede lo sviluppo di infrastrutture di ricarica rapida robuste, efficienti e versatili. Le infrastrutture di ricarica sono tipicamente costituite da convertitori di potenza che consentono un trasferimento di energia efficiente e sicuro. I convertitori AC-DC sono responsabili della raddrizzazione della tensione di rete in un'uscita DC stabile, garantendo la qualità dell'alimentazione e la conformità alla rete. Successivamente, i convertitori DC-DC gestiscono le correnti e le tensioni di carica e scarica delle batterie dei veicoli elettrici, assicurando che soddisfino i requisiti specifici delle batterie e mantengano la sicurezza, l'affidabilità e le prestazioni durante l'intero processo di ricarica.

Questa tesi approfondisce in particolare la progettazione, il controllo e l'ottimizzazione dei convertitori DC-DC a doppio ponte attivo (DAB), che sono fondamentali per le stazioni di ricarica EV ad alta potenza grazie alle loro capacità di soft-switching e all'adattabilità a diverse chimiche di batterie e requisiti di potenza. Una sfida centrale in questo campo, tuttavia, è quella di garantire transizioni fluide tra le diverse fasi di carica, come le modalità a corrente costante (CC) e a tensione costante (CV), che sono essenziali per mantenere la salute della batteria e l'efficienza di carica ottimali.

L'indagine iniziale esplora il funzionamento dinamico dei convertitori DAB, introducendo un modello medio generalizzato (GAM) migliorato basato sulla serie di Fourier che incorpora gli effetti delle resistenze parassite nei condensatori del filtro di uscita. Questo modello migliora l'accuratezza delle simulazioni, fornendo una rappresentazione più realistica della risposta dinamica del convertitore. A complemento di questo modello, viene proposta una nuova strategia di controllo che combina meccanismi di feedforward e feedback. Questa strategia impiega la modulazione SPS (Single Phase Shift) per facilitare una transizione senza soluzione di continuità tra le modalità di carica CC e CV, cruciale per mantenere le prestazioni durante le diverse fasi di carica della batteria, attenuando i problemi tipici di undershoot e overshoot durante le transizioni di modalità.

Partendo da queste basi, la ricerca introduce un metodo di controllo innovativo che integra tecniche basate su droop con un sofisticato sistema di controllo attivo di reiezione dei disturbi (LADRC). Questa combinazione viene nuovamente applicata a un convertitore DAB monofase a modulazione di sfasamento, affrontando la questione critica della transizione senza soluzione di continuità tra gli stadi di carica. Il sistema LADRC aumenta la robustezza del convertitore rispetto alle fluttuazioni della tensione di ingresso e alle variazioni del carico, stabilizzando così il processo di carica. Inoltre, il metodo di controllo proposto riduce la corrente di picco in ingresso, consentendo l'uso di componenti di classe inferiore, che contribuiscono a ridurre il

Content

Acknowledgement	i
Abstract	iii
Sommario	v
List of Figures	xv
List of Tables	xvii
Symbols	xix
List of Abbreviations	xxi
List of Publications	xxvii
1 Introduction	1
1.1 Background of Studies	1
1.1.1 The Evolution of Electric Vehicles	1
1.1.2 The Role of Charging Infrastructure	1
1.2 Motivation	2
1.2.1 Challenges in DAB DC-DC Converter Technology for EV Charging	2
1.2.2 The Need for Innovative Battery Charging Solutions	3
1.3 Research Objectives	4
1.4 Organization of the Thesis	4
2 State of the Art of Storage Systems for EVs	7
2.1 Introduction	7
2.2 Types of Energy Storage Systems	8
2.2.1 Batteries	8
2.2.2 Supercapacitors	11
2.2.3 Flywheels	11
2.2.4 Hydrogen Tank Storage	12
2.3 Energy Storage Systems Models for Power Electronic Applications	16
2.3.1 Battery Models	16
2.3.2 Supercapacitor Models	18

2.4	Hybrid Energy Storage Systems for Electric Vehicles	21
2.4.1	Battery and Ultracapacitor Hybrid System	21
2.4.2	Battery-Flywheel Hybrid System	23
2.5	Energy Management Strategies (EMS) in EVs in the Presence of HESS	24
2.5.1	Rule-Based (RB) EMS	25
2.5.2	Optimization-Based (OB) EMS	26
2.5.3	Learning-Based (LB) EMS	28
2.6	Battery Charging Strategies	29
2.6.1	Model-free Charging Techniques	29
2.6.2	Model-Based Charging Techniques	34
2.7	Conclusion	35
3	Power Converters for Electric Vehicle Charging Stations	37
3.1	Introduction	37
3.2	Charging Strategies and Methods for Electric Buses	40
3.3	Architectures for Fast Charging of Electric Vehicles	41
3.4	Converter Topologies for EV Charging Systems	44
3.4.1	Front-end AC-DC Converters Topologies	44
3.4.2	Back-end DC-DC Converters	48
3.5	DC-DC Converters Based on Partial Processing of Power	54
3.6	Multiport Converters for EV Charging Stations	57
3.7	Conclusion	60
4	Non-Modular DAB Dynamic Modeling and Robust Control Strategies	63
4.1	Introduction	63
4.2	DAB Converter Principles of Operation under SPS Modulation	68
4.2.1	Steady State Operation	68
4.2.2	Soft Switching Limits (Soft Switching vs Reactive Current)	73
4.3	System Modeling	76
4.3.1	Thevenin Model of EV battery	76
4.3.2	Enhanced Generalized Average Model (GAM) of DAB Converter	78
4.4	Control Strategies for DAB Converter	85
4.4.1	PI Controller Design for DAB Battery Charger	85
4.4.2	LADRC for DAB: Design and Implementation	92
4.4.3	NLADRC for DAB: Design and Implementation	104
4.5	Conclusion	109
5	Advanced Modulation Techniques and Vector Control for DAB Converters	111
5.1	Introduction	111
5.2	Unified Harmonic Analysis of DAB Converter under Three-level Modulated Phase Shift Control	114
5.2.1	Operational Principle of Three-level Phase Shift Modulation	114
5.2.2	Fourier Series Based Harmonic Analysis of HFL Voltage and Current	116
5.3	Vector Control based on LADRC	119

5.3.1	DPS Modulation	119
5.3.2	Extraction of Inductor Current Orthogonal Components	120
5.3.3	LADR-based Inductor Current Control	124
5.3.4	Phase Angle Determination for Reactive Power and RMS Inductor Current Minimization	124
5.3.5	LADRC-based Output Current Loop Control	126
5.3.6	Battery Voltage Loop Control Based on LADRC	127
5.3.7	Proposed Feedforward for Dynamic Performance Enhancement	127
5.4	Numerical Verifications	128
5.5	Conclusion	132
6	Modular DAB System Design, Modelling and Control	135
6.1	Introduction	135
6.2	Performance Evaluation of Various Modular DAB Topologies	139
6.2.1	Electro-thermal Modelling for Efficiency Determination	139
6.2.2	Power Balance Decouple Control Strategy of Modular DAB Based on GAM	144
6.2.3	Comparative Results Through Numerical Simulations	146
6.3	Dynamic Phase Shedding and Interleaving Approach for Modular DAB Converters	150
6.3.1	Fundamental Interleaving Concept in Modular DAB Converters	150
6.3.2	Functioning of the Proposed Adaptive Phase Shedding and Interleaving Strategy	151
6.3.3	Numerical Validation	154
6.4	Sensor Reduction Technique in Modular DAB Battery Charging System	158
6.4.1	Proposed Control Strategy	158
6.4.2	Numerical Validation	161
6.5	Conclusion	162
7	Conclusions	165
7.1	Introduction	165
7.2	Summary of Findings and Main Contributions	165
7.2.1	Comprehensive Modeling of the DAB Converter System	165
7.2.2	Innovative Control Strategies	166
7.2.3	Dynamic Optimization in DAB Control	166
7.2.4	Modular Converter Efficiency and Reliability	166
7.2.5	Practical Implications for EV Charging	167
7.3	Possible Improvements and Future Directions	167
7.3.1	Controller Optimization	167
7.3.2	DAB Converter Scalability and Modularity	167
7.3.3	Enhanced Thermal Management	167
7.3.4	EV Battery Cell Balancing and Integration to BMS	167
7.3.5	Experimental Validation	167
7.4	Final Remarks	168
	Bibliography	169

List of Figures

2.1	Specific energy density and volumetric energy density of various battery types. .	10
2.2	Schematic representation of a FESS.	12
2.3	The operational principle of a fuel cell.	13
2.4	Battery equivalent circuit models: (a) zero-time-constant model (b) 1 st order model with self-discharge effect (c) simplified 1 st order model (d) 2 nd order model (e) 1 st order PNGV model (f) modified Rint model with path selection (g) 1 st order Thevenin model with path selection (h) 2 nd order model with path selection (i) runtime-based model (j) NREL RC battery model.	17
2.5	Example of HPPC test profile for battery parameterization.	18
2.6	SC equivalent circuit models (a) classical equivalent circuit model (CECM) (b) first-order model (c) SC model using a Debye polarization (d) integer-order dynamic electrical circuit model (e) modified CECM (f) ladder circuit model (g) two-branch model (h) transmission line model (i) Zubieta Model (j) Rafik model (k) Faranda model (l) High-frequency model considering the temperature-dependency. . . .	19
2.7	Battery and UC HESS (a) Passive parallel (b) Parallel semi-active topology (c) Battery-UC semi-active (d) UC-battery semi-active (e) cascaded battery-UC topology (f) cascaded UC-battery topology (g) multiple parallel-connected hybrid topology (h) multiple input converter topology.	22
2.8	Flywheel-based hybrid energy storage system.	24
2.9	Classification of EMS used in EVs.	25
2.10	Battery charging strategies-I (a) CC charging (b) CV voltage (c) CC-CV charging. .	30
2.11	Current (blue) and voltage (red) profiles verses time during MSCC charging strategy for transition criteria from one stage to the next stage.	30
2.12	CT-CV charging strategy (a) Current profile (b) Temperature profile.	31
2.13	(a) CL-CV charging profile (b) CP-CV charging profiles.	32
2.14	Pulse charging method (a) PPC (b) NPC.	33
2.15	Battery Charging current with (a) ripple current and (b) dc charging current. . .	33
2.16	BC charging profile.	34
3.1	On-board and off-board charging system.	38
3.2	E-bus charging methods.	40
3.3	Different types of pantographs (a) downward; (b) upward; (c) horizontal; (d) underbody.	41

3.4	Fast charging stations configurations with: (a) AC-bus coupling; (b) DC-bus coupling (c) Hybrid architecture.	42
3.5	DC-bus configurations (a) unipolar DC-bus (b) bipolar DC-bus.	44
3.6	Front-end rectifier topologies-I (a) Vienna boost rectifier; (b) Voltage source 6-switch boost rectifier; (c) Bidirectional interleaved converter; (d) NPC converter.	45
3.7	Front-end rectifier topologies-II (a) Three-phase cascaded H-bridge rectifier circuit (b) Three-phase 3-level flying capacitor MLC (c) Modular Multilevel converter (MMC) (d) Current source 6-switch buck type PFC rectifier.	46
3.8	Front-end rectifier topologies-III (a) Swiss buck rectifier; (b) 12-pulse diode rectifier.	47
3.9	Isolated DC-DC converters-I (a) phase shift full-bridge ZVS converter (b) dual active bridge (c) cascaded dual active bridge (d) interleaved full-bridge with voltage doubler.	49
3.10	Isolated DC-DC converters-II (a) full-bridge isolated LLC resonant converter (b) half-bridge LLC resonant converter (c) full-bridge CLLC resonant converter (d) full-bridge CLLLC resonant converter.	50
3.11	Non-isolated DC-DC converters-I (a) Interleaved buck converter (b) Three level NPC boost converter; (c) Three level flying capacitor boost converter (d) Cascaded buck-boost converter.	52
3.12	Non-isolated DC-DC converters-II (a) split-pi converter (b) interleaved split-pi converter; (c) Cuk converter (d) combined SEPIC/zeta converter.	53
3.13	Power flow diagram (a) FPP (b) PPP.	55
3.14	PPC topologies requiring isolated DC-DC converters (a) IPOS step-up (b) ISOP-I step-up (c) ISOP-II step-up (d) ISOP step-down (e) IPOS-I step-down (f) IPOS-II step-down.	55
3.15	PPC topologies that do not require isolated DC-DC converters (a) step-up (b) step-down.	56
3.16	DC-DC converter based on DAB for fast charging station (a) FPP-DAB (b) PPP-DAB.	57
3.17	Comparison of DAB-FPP with DAB-PPP (a) processed power ratio (K_{pr}) vs SoC (b) efficiency vs SoC.	57
3.18	Multiport converter systems (a) two-stage multiport grid-connected system (b) single-stage multiport grid-connected system.	58
3.19	Classification of multiport converters.	59
3.20	(a) Non-Isolated Multiport Converter (b) Isolated Multiport Converter (DIDO) (c) Partially Isolated Multiport Converter (DIDO).	59
4.1	Typical DC-DC DAB topology.	63
4.2	Battery voltage and current regulations: (a) two single feedback loops (b) one cascaded feedback loop.	66
4.3	Typical theoretical waveforms of DAB converter under SPS modulation (a) buck mode ($V_g > V_o/n$) (b) boost mode ($V_g > V_o/n$) (c) gainless mode ($V_g = V_o/n$).	68
4.4	Operational modes of DAB converter under SPS modulation for forward power flow.	69
4.5	Detailed representation of inductor voltage and current.	70

4.6	(a) Input current of DAB converter (b) Output current of DAB converter.	71
4.7	Variation of power flow with phase shift under SPS.	72
4.8	Current paths in the converter during commutation from interval I-b to II.	74
4.9	ZVS regions under SPS modulation (a) variation of converter gain with phase shift ratio (b) variation of converter gain with normalized output power for different inductor values.	75
4.10	Thevenin second-order equivalent circuit battery model.	77
4.11	Battery current and voltage from pulse discharge test.	77
4.12	MATLAB/Simulink implementation of the second order Thevenin equivalent circuit battery model.	79
4.13	DAB equivalent circuit for GAM.	80
4.14	Visualization of the Fourier series representation of S_1 and S_2	80
4.15	GAM validation through PLECS simulation.	84
4.16	Open loop Bode plots of the control to output transfer function ($G_{V\phi}$) for different values of capacitor ESR.	85
4.17	Schematic diagram of the proposed control system for DAB-based battery charging system.	86
4.18	Battery voltage (top) and average battery current (bottom) without (left) and with (right) proposed feedforward.	89
4.19	Comparison of current and voltage waveforms with and without the proposed feedforward control	89
4.20	Effect of variation of current loop integral gain constant on system performance.	90
4.21	Effect of PI controller integral constant variation on disturbance rejection performance.	90
4.22	closed loop small signal model with feedforward of the converter system.	91
4.23	Bode plot of (a) current loop gain and (b) voltage loop gain with and without feedforward.	91
4.24	Schematic of the LADRC principle.	92
4.25	Bode diagram of $G_{ry}(s)$ when control BW (ω_c) varies.	95
4.26	Bode diagram of $G_{fy}(s)$ when (a) control BW varies (b) observer BW varies.	96
4.27	Proposed two-loop LADR-based battery charging control system.	96
4.28	Normalized output current curve showing variations in α and β for different normalized output voltage values.	99
4.29	Relationship between (a) input current and output voltage; (b) input current and output current.	100
4.30	Battery voltage (top) and average battery current (bottom) with (left) and without (right) feedforward.	102
4.31	Input and inductor current transient waveforms with and without the proposed feedforward technique.	102
4.32	Comparing the transient performance of the proposed three approaches.	103
4.33	Comparing the conventional feedforward approach with the proposed approaches.	104
4.34	Structure of NLADRC.	104
4.35	Some examples of selected sigmoid functions.	105

4.36	Curves of $\tanh(\beta_1 x)$ with variation in β_1 .	106
4.37	Comparison of converter battery current (top), battery voltage (middle) and average input current response (bottom) with LADRC and NLADRC.	109
5.1	(a) DAB converter AC equivalent circuit (b) Illustrative waveforms depicting the three-level modulation technique applied to a DAB converter under unified phase-shift control.	114
5.2	DAB waveforms under different DPS operating conditions: (a) $0 < \theta_3 < \gamma < 1$ (b) $0 < \gamma < \theta_3 < 1$.	115
5.3	Normalized active power harmonic contributions as a function of external phase shift (b) Variation of normalized reactive power with external phase shift.	117
5.4	(a) Variation of power factor with internal and external phase shift angles (b) variation of power factor with external phase shifts under different modulation schemes.	118
5.5	Proposed battery charging control system with three-loop configuration.	119
5.7	Block diagram showing the extraction of the inductor current active and quadrature components.	120
5.6	DPS power flow modulator: (a) Schematic diagram; (b) Some waveforms produced by the modulator.	121
5.8	BPF response for various Q values: (a) Frequency response; (b) unit step response.	122
5.9	LPF response for various Q values: (a) Frequency response; (b) unit step response.	123
5.10	Phasor diagrams for DAB positive power flow in DPS: (a) control objective is controlling magnitude and phase of inductor secondary voltage (b) control objective is controlling magnitude and phase of inductor primary voltage with 90° axis rotation.	125
5.11	Relationship between: (a) input current and output voltage; (b) output voltage and output current.	128
5.12	Inductor current and its decoupled components.	129
5.13	Battery voltage (top) and average battery current (bottom) with (left) and without (right) feedforward.	129
5.14	DQ-axis inductor current control with and without the proposed feedforward technique.	130
5.15	Input and Inductor current transient waveforms with and without the proposed feedforward technique.	131
5.16	Effect of acceleration factor on dynamic performance.	131
5.17	Comparison of PI and LADRC: Battery voltage (top) and average battery current (bottom) without (left) and with (right) feedforward.	132
6.1	Different connection schemes for modular DC-DC converters..	136
6.2	Switching power losses: (a) Turn-on losses (b) Turn-off losses	140
6.3	Foster type (Pi model) thermal network.	141
6.4	Block diagram of electro-thermal model for determining efficiency.	143

6.5	Thermal model comparative results: (a) Switching losses (b) Conduction losses (c) MOSFET junction temperature (d) Diode junction temperature.	144
6.6	Generalized power sharing control scheme for modular DAB converters (a) Decoupled triple-closed loop control strategy (b) Triple closed loop equivalent control strategy.	147
6.7	Average output current (top) and average input current (bottom) per module without (left) and with (right) PBS.	148
6.8	Output current (top), input current (middle) and inductor current (bottom) per module without (left) and with (right) PBS.	149
6.9	RMS inductor current in various modular DAB topologies.	149
6.10	Total power losses (top) and efficiency (bottom) of various modular converters.	150
6.11	Modular IPOP DAB converter.	150
6.12	Interleaving principle in modular DAB converter.	151
6.13	(a)Power losses and (b) Efficiency of IPOP DAB converter with different number of modules in operation.	152
6.14	(a) Static phase shedding technique (b) Rotational phase shedding technique.	153
6.15	Schematic diagram of proposed module shedding and interleaving control along-side power balance and battery charge control.	153
6.16	Phase enabling control logic	154
6.17	Output current per module with and without module shedding and interleaving.	155
6.18	Battery current and voltage with and without module shedding and interleaving.	155
6.19	Overall system efficiency with and without module shedding and interleaving.	155
6.20	Average battery current (top) and battery voltage (bottom) during RPS&I	156
6.21	Average output current per module during RPS&I.	156
6.22	Inductor current per module during RPS&I.	157
6.23	Junction Temperature evolution across modules with RPS&I and SPS&I schemes.	157
6.24	Equivalent circuit of output stage of IPOP DAB converter.	158
6.25	Bode diagram of first, second and third order Carlson approximation of $s^{0.5}$	160
6.26	Proposed Sensor reduction technique for modular IPOP DAB converter.	161
6.27	(a) Battery current with proposed and conventional observer (b) Inductor currents with proposed and conventional observer.	162

List of Tables

2.1	Technical comparison of various energy storage technologies	15
3.1	Main characteristics of EV battery chargers.	39
3.2	Comparison Between DC and AC Connected EV Charging Architecture	43
3.3	K_{pr} for different PPC configurations of Figure 10.	56
4.1	RMS current of switching devices in primary and secondary full bridges (buck mode)	73
4.2	Average current of switching devices in primary and secondary full bridges (buck mode)	73
4.3	Conditions for ZVS under SPS for positive power flow	75
4.4	Parameters of the second-order Thevenin equivalent model	78
4.5	DAB converter specifications.	84
4.6	DAB converter specifications.	88
4.7	Controller parameters.	101
4.8	A list of some selected sigmoid functions	105
4.9	NLADRC parameters	108
5.1	Active devices during each interval in DPS	115
5.2	DAB converter specifications.	120
5.3	Bandpass filter specifications.	122
5.4	Low pass filter specifications.	123
5.5	Vector Control parameters.	129
6.1	Control Signal Representation for Modular DAB Systems	146
6.2	Modular DAB converter System specifications	148
6.3	DAB converter specifications for single module.	152

Symbols

Symbol	Description	Unit
ϕ	Phase shift angle	rad
T_s	Switching period	s
f_s	Switching frequency	Hz
V_g/V_{in}	Converter input voltage	V
V_o	Converter output voltage	V
V_c	Capacitor voltage	V
V_{ds}	Mosfet drain-source voltage	V
i_g/i_{in}	Converter input current	A
i_o	Converter output current	A
i_b	Battery current	A
i_L	Inductor current	A
E_L	Inductor energy	J
E_C	Capacitor energy	J
ω_s	Angular switching frequency	rad s ⁻¹
ω_o	Observer bandwidth	rad s ⁻¹
ω_c	Controller bandwidth	rad s ⁻¹
G_{Load}	Load Conductance	Ω^{-1}
C	Capacitance	F
L	Inductance	H
r_x	parasitic resistance	Ω
θ_1	Internal phase shift between parallel legs of primary full-bridge	rad
θ_2	Internal phase shift between parallel legs of secondary fullbridge	rad
θ_3	External phase shift between primary and secondary fullbridges	rad
P	Active power transfer	W
Q	Reactive power transfer	VAR
S	Apparent power	V A
V_1/V_p	Inductor primary voltage	V
V_2/V_s	Inductor secondary voltage	V
P_m	Total Mosfet power losses	W

Symbol	Description	Unit
P_d	Total diode power losses	W
T_m	Mosfet Foster network node temperatures	K
T_d	Diode Foster network node temperatures	K

List of Abbreviations

Notation	Description
1D	One-Dimensional
ADM	asymmetric duty cycle modulation
ADRC	active disturbance rejection control
A-ECMS	Adaptive-ECMS
A-PMP	Approximate-PMP
AFC	Alkaline Fuel Cell
ANN	Artificial Neural Network
AZI	Aqueous Zinc-Ion
BC	Boost Charging
BCM	Boundary Conduction Mode
BEV	Battery Electric Vehicle
BLDC	Brushless DC
BMS	Battery Management System
BPF	bandpass filter
BW	Bandwidth
CACF	Constant Amplitude - Constant Frequency
CAVF	Constant Amplitude - Varying Frequency
CC	Constant Current
CC-CV	Constant Current - Constant Voltage
CCM	Continuous Conduction Mode
CCS	Combined Charging System
CHB	Cascaded H-Bridge
CL-CV	Constant Loss - Constant Voltage
CP	Convex Programming
CP-CV	Constant Power - Constant Voltage
CPS	common phase shift
CT-CV	Constant Temperature - Constant Voltage
CV	Constant Voltage
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DDP	Deterministic Dynamic Programming
DIRECT	Divided Rectangular

Notation	Description
DMFC	Direct Methanol Fuel Cell
DMPC	Deterministic Model Predictive Control
DoD	Depth of Discharge
DPS	Dual-Phase Shift
DTC	Direct Torque Control
ECM	Equivalent Circuit Model
ECMS	Equivalent Consumption Minimization Strategies
EDLC	Electric Double Layer Capacitor
EIS	Electrochemical Impedance Spectroscopy
EMI	Electromagnetic Interference
EMS	Energy Management Strategy
ES	Extremum Seeking
ESD	Energy Storage Device
ESO	Extended State Observer
ESR	equivalent series resistance
ESS	Energy Storage System
EV	Electric Vehicle
FCC	Flying Capacitor Converter
F-ES	Fractional Order Extremum Seeking
FC	Fuel Cell
FCEV	Fuel Cell Electric Vehicle
FESS	Flywheel Energy Storage System
FOC	Field Oriented Control
FOD	fractional-order derivative
FOM	Full Order Model
FPP	Full Power Processing
G2V	Grid-to-Vehicle
GA	Genetic Algorithm
GAM	Generalized Average Model
GT	Game Theory
GWO	Grey-Wolf Optimization
HCC	Hysteresis Current Control
HESS	Hybrid Energy Storage System
HFT	High-Frequency Transformer
HM	hybrid modulation
HPPC	Hybrid Pulse Power Characterization
HSC	Hybrid Supercapacitor
ICE	internal combustion engine
ICS	input current sharing
IPOP	input-parallel-output-parallel
IPOS	input-parallel-output-series

Notation	Description
ISOP	input-series-output-parallel
ISOS	input-series-output-series
IVS	input voltage sharing
LA	Lead Acid
LADRC	Linear Active Disturbance Rejection Control
LB	Learning-Based
LESO	Linear Extended State Observer
LFT	Low-Frequency Transformer
Li-ion	Lithium-ion
LP	Linear Programming
LPF	low pass filter
LSEF	Linear State Error Feedback
LVS	low voltage side
MCC-CV	Multistage Constant Current - Constant Voltage
MCFC	Molten Carbonate Fuel Cell
MLC	Multilevel Converter
MMC	Modular Multilevel Converter
MOGA	Multi-Objective Genetic Algorithm
MPC	Model Predictive Control
MV	Medium Voltage
NiCd	Nickel-Cadmium
NiFe	Nickel-Iron
NiMH	Nickel-Metal Hydride
NiZn	Nickel-Zinc
NLADRC	Non-Linear Active Disturbance Rejection Control
NLC	Nearest Level Control
NLESO	Non-Linear Extended State Observer
NLSEF	Non-Linear State Error Feedback
NNL	Neural Network Learning
NPC	Negative Pulse Current
NPC	Neutral Point Clamped
NREL	National Renewable Energy Laboratory
OB	Optimization-Based
OCC	One Cycle Control
OCS	output current sharing
ODE	Ordinary Differential Equation
OVS	output voltage sharing
P2D	Pseudo Two-Dimensional
PAFC	Phosphoric Acid Fuel Cell
PBS	power balancing scheme
PC	Pulse Charging

Notation	Description
PDE	Partial Differential Equation
PEMFC	Proton Exchange Membrane Fuel Cell
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PM	Phase Margin
PMP	Pontryagin's Minimum Principle
PPC	Positive Pulse Current
PPP	Partial Power Processing
PsC	Pseudo Capacitor
PSFB	Phase-Shift Full Bridge
PSO	Particle Swarm Optimization
PWM	Pulse-Width Modulation
QP	Quadratic Programming
RB	Rule-Based
RBS	Regenerative Braking System
RDC	Reduced Dissipation Converter
RES	Renewable Energy Source
RL	Reinforcement Learning
ROI	Return On Investment
RPC	Reactive Power Compensation
RPS&I	rotational phase-shedding and interleaving
SA	Simulated Annealing
SC	Supercapacitor
SDP	Stochastic Dynamic Programming
SHE	Selective Harmonic Elimination
SISO	Single Input Single Output
SL	Supervised Learning
SMC	Sliding Mode Control
SMPC	Stochastic Model Predictive Control
SoC	State of Charge
SOFC	Solid Oxide Fuel Cell
SoH	State of Health
SP	Single Particle
SP2D	Simplified P2D
SPS&I	static phase-shedding and interleaving
SP-SDP	Shortest Path SDP
SPS	Single-Phase Shift
SQP	Sequential Quadratic Programming
SRC	Sinusoidal Ripple Current
SVM	Space Vector Modulation
TD	Tracking Differentiator

Notation	Description
THD	Total Harmonic Distortion
TPS	Triple-Phase Shift
TRM	triangular modulation
TZM	trapezoidal modulation
UC	Ultracapacitor
UL	Unsupervised Learning
UPS	Uninterruptible Power Supplies
V2G	Vehicle-to-Grid
VACF	Variable Amplitude - Constant Frequency
VLA	Vented Lead Acid
VRLA	Valve-Regulated Lead Acid
VSFM	variable switching frequency modulation
XFC	Extreme Fast Charging
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Publications

Journal Publications

- [1] **A. A. Nkembi**, D. Santoro, F. Ahmad, I. Kortabarria, P. Cova, E. Sacchi, and N. Delmonte, "Novel droop-based techniques for dynamic performance improvement in a linear active disturbance rejection controlled-dual active bridge for fast battery charging of electric vehicles," *Energies*, vol. 17, no. 20, p. 5171, 2024, doi: [10.3390/en17205171](https://doi.org/10.3390/en17205171).
- [2] **A. A. Nkembi**, D. Santoro, F. Ahmad, I. Kortabarria, P. Cova, E. Sacchi, and N. Delmonte, "A novel feedforward scheme for enhancing dynamic performance of vector-controlled dual active bridge converter with dual phase shift modulation for fast battery charging systems," *Electronics*, vol. 13, no. 19, p. 3791, 2024, doi: [10.3390/electronics13193791](https://doi.org/10.3390/electronics13193791).
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Conference Publications

- [1] **A. A. Nkembi**, F. Ahmad, I. Kortabarria, P. Cova, N. Delmonte, D. Santoro, and E. Sacchi, "Performance comparison of different modular dual active bridge converter topologies for fast battery charging applications," in *2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*. IEEE, 2024, pp. 960–965, doi: [10.1109/speedam61530.2024.10609166](https://doi.org/10.1109/speedam61530.2024.10609166).
- [2] **A. A. Nkembi**, P. Cova, I. Kortabarria, E. Sacchi, N. Delmonte, and M. Portesine, "A reduced-sensor modular dual active bridge-based battery charging system for electric vehicles using an improved linear extended state observer," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2024, pp. 2464–2472, doi: [10.30420/566262347](https://doi.org/10.30420/566262347).
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Chapter 1

Introduction

This chapter introduces the critical role of DC-DC converters, particularly the Dual Active Bridge (DAB) converter, in supporting the growing demand for efficient Electric Vehicle (EV) charging infrastructure. It outlines key challenges, including maintaining efficiency across varying loads and ensuring smooth transitions between battery charging modes. The chapter also presents the research objectives, which focus on enhancing modeling, improving control strategies, and optimizing system designs. Finally, it provides an overview of the thesis structure, detailing how each chapter addresses these objectives.

1.1 Background of Studies

1.1.1 The Evolution of Electric Vehicles

EVs are increasingly recognized as a cornerstone in the transition towards a more sustainable and environmentally friendly transportation system. Unlike traditional internal combustion engine vehicles, EVs produce zero tailpipe emissions, significantly reducing their environmental footprint [1,2]. This shift is driven by growing concerns over climate change, air quality, and the finite nature of fossil fuel resources. Governments worldwide are implementing stringent emission regulations and offering incentives to accelerate the adoption of EVs, resulting in a rapid increase in the number of EVs on the road [3,4].

However, the success of EVs is closely linked to the development of an efficient and reliable charging infrastructure [5]. As the EV market grows, so does the need for fast-charging solutions that can accommodate the diverse battery profiles of various EV models. The primary challenge lies in designing charging systems that not only provide rapid charging but also ensure safety, efficiency, and cost-effectiveness [6].

1.1.2 The Role of Charging Infrastructure

The charging infrastructure for EVs is a complex ecosystem comprised of several components, including charging stations, power converters, and intelligent control systems. Charging stations serve as the critical interface between the grid and the EV, delivering electrical energy to the vehicle's battery. These stations vary widely in terms of power capacity, charging speed, and connector types, catering to the diverse needs of different EV models [7].

Central to the charging process is the power converter typically made up of two key conversion stages. The first stage is the AC-DC converter, responsible for rectifying the grid voltage into a stable DC voltage while ensuring high power quality and compliance with grid standards. The second stage is the DC-DC converter, which efficiently regulates the power flow between the charging station and the vehicle's battery, ensuring precise control of the charging current and voltage to meet the battery's requirements and optimize its performance and lifespan. These converters operate under demanding conditions, requiring high efficiency, fast response times, and robust performance [8,9]. Key performance metrics include conversion efficiency, power density, voltage and current ratings, and thermal management capabilities. Additionally, advanced control strategies are essential to optimize charging time, minimize energy losses, and ensure battery health.

Furthermore, the integration of renewable energy sources, such as solar and wind power, into the EV charging infrastructure is gaining significant attention. This integration not only supports the transition to cleaner energy systems but also enhances the sustainability of EV charging networks [10,11]. In addition, bidirectional charging capabilities, where EVs can both receive (charge) and supply (discharge) energy, are emerging as a transformative technology. These capabilities enable EVs to act as mobile energy storage units, providing flexibility in energy management.

Bidirectional charging facilitates Vehicle-to-Grid (V2G) applications, where EVs can discharge excess stored energy back into the grid. This process helps balance supply and demand, particularly during peak load periods or when renewable energy generation is variable [12]. By allowing EVs to return power to the grid, V2G technology can support grid stability, reduce energy costs, and enhance the overall efficiency of the energy system. Additionally, this approach can provide financial incentives to EV owners through grid services like demand response or frequency regulation [13]. As renewable energy sources become more integrated with charging infrastructure, the potential for V2G applications to contribute to a more resilient and sustainable energy grid becomes increasingly important.

Among the various types of bidirectional DC-DC converters, the DAB converter has gained prominence due to its high-power handling capability and soft-switching characteristics. DAB converters are particularly well-suited for high-power charging applications because they can efficiently convert high voltage DC from the grid to the appropriate voltage levels required by EV batteries [14,15].

1.2 Motivation

1.2.1 Challenges in DAB DC-DC Converter Technology for EV Charging

Despite the considerable efforts made towards the advancement in the DAB converter topology, several key issues and challenges must be addressed to optimize their performance for rapid EV charging. These challenges include:

- **Transition Between Charging Modes:** EV batteries typically require different charging modes, such as Constant Current (CC) and Constant Voltage (CV), during different stages of the charging process. Smoothly transitioning between these modes is crucial for

maintaining battery health and optimizing charging time. Conventional control systems may struggle with maintaining performance during these transitions, leading to potential inefficiencies and system instability [16, 17].

- **Efficiency Across Load Ranges:** DAB DC-DC converters must maintain high efficiency across a wide range of load conditions. At light loads, traditional modular topologies suffer from reduced efficiency mainly because switching losses are significantly higher than conduction losses, while core losses remain relatively constant regardless of load conditions, impacting overall system performance [18–20]. This issue necessitates innovative control strategies to enhance efficiency and reduce power losses.
- **Modular Topology Design:** Modular DAB converters offer the advantage of reducing voltage and current stress on individual power switches, allowing for the use of lower-rated components. However, managing power balance among modules and ensuring effective communication between them is complex [21, 22]. Additionally, the need for multiple sensors increases system costs, significant processing time and introduces potential inaccuracies [23–26].
- **Advanced Modulation Techniques:** To enhance the performance of DAB converters, advanced modulation techniques such as Dual-Phase Shift (DPS) modulation, Triple-Phase Shift (TPS) Modulation, Trapezoidal modulation, Triangular modulation are employed [27, 28]. These techniques improve soft-switching capabilities and overall efficiency but require sophisticated optimization and control strategies [29–31]. Ensuring optimal phase shift angles while minimizing system complexity is a significant challenge [32–34].

1.2.2 The Need for Innovative Battery Charging Solutions

To address the aforementioned challenges and enhance the performance of DAB converters, several areas of innovation are critical:

- **Advanced Modeling:** Accurate modeling of DAB converters that accounts for generally neglected factors such as parasitic resistances and dynamic behavior is essential for optimizing performance. Improved models help predict system behavior more accurately and guide the design of control strategies.
- **Enhanced Control Strategies:** Integrating advanced control systems that combine feedforward and feedback mechanisms can significantly improve system performance, especially during mode transitions. Moreover, advanced control techniques like Linear Active Disturbance Rejection Control (LADRC) offer increased robustness and stability in the face of varying input and load conditions.
- **Cost-Effective System Designs:** Reducing the cost of EV charging infrastructure involves minimizing the reliance on expensive components and reducing the need for numerous sensors. Techniques such as phase-shedding, interleaving and extended state observers can help achieve these goals while enhancing system efficiency.

- **Practical Validation:** Validating proposed solutions through numerical simulations and practical testing is crucial for demonstrating their effectiveness. Tools like MATLAB/Simulink provide valuable insights into system performance and help refine designs to meet real-world requirements.

1.3 Research Objectives

This research aims to address the aforementioned challenges and contribute to the advancement of DAB converters for high-power EV charging applications. The specific objectives are:

1. ***To Develop an Enhanced Model for DAB Converters***
Create a Fourier series-based Generalized Average Model (GAM) that incorporates parasitic resistances and provides a more accurate representation of the converter's dynamic behavior.
2. ***To Improve Control Strategies for EV Charging***
Propose novel feedforward and feedback control systems utilizing Single-Phase Shift (SPS) modulation to ensure smooth transitions between CC and CV charging modes.

Integrate both a Linear Active Disturbance Rejection Control (LADRC) and Non-Linear Active Disturbance Rejection Control (NLADRC) system to enhance robustness and stability against input voltage and load disturbances.
3. ***To Explore and Optimize Advanced Modulation Techniques***
Investigate DPS modulation to improve soft-switching capabilities and power conversion efficiency. Develop a three-loop control system with decoupled dq vector control to optimize phase shift angles and reduce peak input current.
4. ***To Design and Validate Innovative Modular System Approaches***
Conduct a comparative analysis of various modular DAB topologies to identify configurations that offer superior performance and efficiency.

Introduce an adaptive module-shedding technique and an improved extended state observer to address power balance and sensor requirements in modular DAB systems.
5. ***To Demonstrate Practical Impact Through Simulations***
Perform extensive numerical simulations using MATLAB/Simulink to validate the proposed models, control strategies, and system designs. Assess the practical benefits in terms of efficiency improvements, cost reduction, and system robustness.

1.4 Organization of the Thesis

The thesis is structured to provide a comprehensive exploration of the research topic, from theoretical modeling and control strategies to practical system design and validation. The organization is as follows:

- **Chapter 1: Introduction**

Provides the background, motivation, research objectives, and organization of the thesis.

- **Chapter 2: State of the Art of Storage Systems for EVs**

This chapter reviews the current state of storage systems used in EVs, including their models, characteristics, and performance metrics. It discusses various battery technologies, such as lithium-ion, and other emerging chemistries, and their implications for EV charging infrastructure. The chapter also covers advancements in battery modeling and the impact of these technologies on charging efficiency and system design. Finally, different battery charging profiles are also discussed.

- **Chapter 3: Power Converters for Electric Vehicle Charging Stations**

Reviews relevant literature on different AC and DC side power converters for EV charging, EV charging strategies/methods. In particular, the DAB converter control strategies for dynamic performance enhancement, and different modulation techniques are all presented. This chapter establishes the context and highlights gaps addressed by this research.

- **Chapter 4: Non-Modular DAB Dynamic Modeling and Robust Control Strategies**

Details the development of the Fourier series-based GAM and the novel feedforward and feedback control strategies using SPS modulation and a combination of Proportional-Integral (PI) controller, LADRC and NLADRC. A comprehensive overview of numerical simulations conducted using MATLAB/Simulink is presented with discussions on the obtained results, system robustness, and practical implications.

- **Chapter 5: Advanced Modulation Techniques and Vector Control for DAB Converters**

Explores the DPS modulation, the three-loop control system with decoupled dq vector control based on LADRC as well as the optimum phase shift angle determination approach based on Fourier series analysis. Furthermore, a novel droop-based feedforward performance enhancement technique is presented to enable seamless transition between battery charging modes. Moreover, a detailed analysis of simulation results obtained using MATLAB/Simulink is presented, focusing on system performance, robustness, and practical implications. Finally, the impact of this modulation on converter performance and efficiency is analyzed.

- **Chapter 6: Modular DAB System Design, Modelling and Control**

This chapter analyzes various modular DAB topologies, evaluating their performance, cost-effectiveness, and system efficiency comparisons. Moreover, a novel adaptive module-shedding and interleaving technique is presented here for efficiency improvement together with an enhanced Luenberger-based Extended State Observer (ESO) having minimal estimation error for sensor reduction in modular DAB systems.

- **Chapter 7: Conclusions**

Summarizes the key findings of the research, discusses the contributions to the field, and outlines potential directions for future research and development.

Chapter 2

State of the Art of Storage Systems for EVs

2.1 Introduction

EVs are at the forefront of the transition to sustainable transportation, offering significant environmental benefits and the potential to reduce dependency on fossil fuels. Central to the operation and efficiency of EVs is their energy storage system [35]. The energy storage system is not only crucial for powering the vehicle but also plays a key role in determining the driving range, performance, and overall reliability of EVs. They perform other functions such as air conditioning, navigation lighting etc. As the demand for EVs grows, the importance of developing advanced, efficient, and cost-effective energy storage solutions becomes increasingly critical for overcoming the range anxiety often associated with EVs [36,37].

Some of the most commonly used Energy Storage Systems (ESSs) in EVs include Supercapacitors (SCs), flywheels, batteries, and hydrogen tanks [38]. ESSs for EVs must meet several stringent requirements, including high energy density for longer driving ranges, rapid charging capabilities to minimize downtime, and durability to withstand numerous charge-discharge cycles over the vehicle's lifespan. Consequently, each energy storage system has distinct attributes, including its power rating, discharge duration, power and energy density, response time, self-discharge rates, lifespan, and cycle count. These characteristics must be taken into account when assessing their appropriateness for different support applications [39,40]. To perform these functions effectively, power electronic converters play a vital role in controlling the power flow between the AC grid, EV electric motors, and ESSs. Furthermore, various bidirectional converters, such as DC-DC, DC-AC, and AC-AC types, are employed to improve system performance metrics like efficiency, reliability, output harmonic distortion, and power density [41].

In addition, there is a growing interest in Hybrid Energy Storage Systems (HESSs) that combine two or more ESSs, thus aiding in overcoming the shortcomings of each energy storage device. There has been a lot of research into the best architecture for HESSs, and solutions vary depending on system complexity, flexibility, and cost [42]. Batteries and SCs are the most common HESS, and numerous works in literature explain their operation, sizing, and control principles [43,44]. Combining batteries with SCs leverages on the high energy density of batteries with the rapid charge-discharge capabilities of SCs thus enhancing the overall performance and

longevity of the ESS, particularly in managing peak power demands and regenerative braking energy in EVs. For instance, [45] introduces a novel Regenerative Braking System (RBS) for EVs utilizing a Brushless DC (BLDC) motor in combination with a HESS comprising battery and SC. They implement an appropriate switching algorithm to elevate the DC-link voltage and facilitate the transfer of energy to either the battery or the SC through the inverter. This approach enhances vehicle acceleration and prevents the battery pack from discharging during uphill driving.

Moreover, the integration of ESSs with V2G technologies is becoming increasingly important. V2G enables EVs to interact with the power grid, allowing them to return excess energy to the grid during peak demand periods or store renewable energy during off-peak times. This capability not only enhances grid stability but also provides economic incentives for EV owners, further promoting the adoption of electric vehicles [46].

In this chapter, we will explore the various types of ESSs used in EVs, examining their technological foundations, performance characteristics, and the challenges they face. We will also discuss their electric models and different schemes for connecting them in hybrid with particular attention to battery and SC. Energy Management Strategys (EMSs), which are critical for improving the efficiency, safety, and affordability of EVs are also presented. Finally, we will explore the various battery charging strategies, including both traditional profile-based methods and advanced methods, which utilize equivalent circuit and electrochemical models to enhance charging efficiency, safety, and battery longevity.

The remainder of this chapter is structured as follows: Section 2.2 outlines the characteristics of the most commonly used ESSs that can be integrated into EVs. Section 2.3 explores the various power electronic models employed to simulate the behavior of these storage systems. Section 2.4 discusses the different hybrid topologies suitable for integrating multiple ESSs, while Section 2.5 addresses the various EMSs employed in EVs to optimally distribute power. In Section 2.6, we present the different battery charging strategies and finally, Section 2.7 concludes the chapter.

2.2 Types of Energy Storage Systems

In EVs, a range of devices are used to store energy in various forms. The most prevalent among these are batteries and supercapacitors, which store energy in an electrical form, and flywheels, which store energy mechanically. Additionally, less commonly utilized storage options include hydrogen tanks for fuel cells, which store energy chemically, and compressed air systems, which store energy in a mechanical form.

2.2.1 Batteries

Batteries are the predominant energy storage devices used in both power systems and automotive applications, as they convert stored internal chemical energy into electrical energy. In automotive contexts, the primary types of batteries include lead-acid, nickel-based, and lithium-ion batteries. Other less common varieties in the market, such as sodium-sulfur, metal-air, and flow batteries, are not covered in this chapter [47]. A notable emerging technology is Aqueous Zinc-Ion (AZI) batteries, which utilize water-based electrolytes instead of organic ones. Although still in the

experimental stage, AZI batteries have garnered significant attention from both scientific and industrial sectors due to their non-flammable nature, excellent thermal stability, robust cycling performance, cost efficiency, and environmental benefits compared to other organic-based batteries. These batteries can achieve energy densities of up to 361 Wh/kg, thanks to zinc metal anodes that offer high gravimetric and volumetric capacities of 820 mAh/g and 5855 mAh/cm³, respectively, with a low redox potential of -0.762 V [48–50].

Lead Acid (LA) batteries are among the most established rechargeable electrochemical devices, widely used in both residential and commercial applications. The two primary types of lead-acid batteries are Vented Lead Acid (VLA), commonly referred to as "flooded," and Valve-Regulated Lead Acid (VRLA), known as "sealed." Flooded batteries are generally more affordable but require regular maintenance, including monthly checks and topping up with distilled water, as well as adequate ventilation due to the emission of flammable gases [51]. LA batteries are utilized in various applications, such as vehicle starting batteries, Uninterruptible Power Supplies (UPS), mobile power applications like forklifts, and small PV systems [52]. They are favored for their low initial cost (ranging from \$60 to \$200 per kWh), high energy efficiency (between 63% and 90%), rapid response, and low self-discharge rates (approximately 2% per month at 25 °C). However, LA batteries exhibit limitations including low specific energy density (25–50 Wh/kg) and a limited cycle life (500–1500 cycles). Additionally, they pose environmental concerns due to the presence of hazardous materials and have issues related to weight, poor performance in low temperatures, and sensitivity to prolonged discharge [47, 51, 52]. These drawbacks constrain their broader commercial application.

Nickel-based batteries are categorized into four main types: Nickel-Cadmium (NiCd), Nickel-Metal Hydride (NiMH), Nickel-Iron (NiFe), and Nickel-Zinc (NiZn). These batteries are known for their durability and resilience, as they can remain in a discharged state for extended periods without sustaining permanent damage. They also perform well in both high and low ambient temperatures, although they require initial conditioning before use [53, 54].

NiCd batteries are often compared with lead-acid batteries due to their similar technical features but offer advantages such as higher cycling capabilities (over 3500 cycles), better power densities, and higher energy densities (40–75 Wh/kg) [55]. However, NiCd batteries have some drawbacks. They exhibit a memory effect, which leads to a reduction in capacity if not periodically fully discharged [54]. Additionally, they have higher self-discharge rates compared to LA batteries, necessitating recharging after periods of storage. Cadmium, a toxic metal used in these batteries, raises environmental concerns related to their disposal. Furthermore, NiCd batteries have a lower cell voltage of 1.20 V, requiring multiple cells to achieve higher voltages, and their manufacturing costs are relatively high, approximately 5–10 times more than comparable LA batteries [56].

NiMH batteries offer approximately 1.5 to 2 times the specific energy (70–100 Wh/kg) and a higher energy density (100–320 Wh/L) compared to NiCd batteries. They provide superior specific power (>200 W/kg) and power density relative to lead-acid batteries, although they are not as high as NiCd batteries [57]. NiMH batteries also exhibit tolerance to overcharge and over-discharge and are considered environmentally friendly and safe due to their minimal toxic content [58]. Additionally, they are less affected by memory effects compared to NiCd batteries and generally have a longer cycle life compared to lithium-ion batteries [55]. However, their major

drawback is their high cost. Other issues include high self-discharge rates due to active material degradation, poor performance at low temperatures, and significant cooling requirements. They also produce heat during rapid charging and high-load discharges, and their service life can be shortened by deep discharges [54].

NiFe batteries are durable, capable of withstanding overcharging and deep discharging, and can last over 20 years in standby applications. They are resistant to vibrations and high temperatures and can remain discharged for extended periods without damage. NiFe batteries are also environmentally safe and non-toxic. However, they have a low specific energy of around 50 Wh/kg and an energy density of approximately 30 Wh/L. They perform poorly at low temperatures and have a high self-discharge rate of 20–40% per month. Additionally, their manufacturing costs are high, nearly four times greater than lead-acid and lithium batteries [59], though they are less expensive than Ni-Cd batteries. NiFe batteries are also quite heavy and bulky, with a low coulombic efficiency, typically under 65%. The open circuit voltage of these cells is 1.4 V, with a discharge voltage of about 1.2 V, necessitating the use of many cells stacked together to achieve higher voltages [60].

NiZn batteries offer a higher cell voltage of 1.65 V compared to the 1.20 V provided by NiCd and NiMH batteries. Currently, NiZn batteries have specific energies ranging from 50–60 Wh/kg and energy densities between 80 and 120 Wh/L, depending on their design. They also demonstrate robust cycling performance, capable of delivering over 500 cycles at 100% Depth of Discharge (DoD) and several thousand cycles at lower DoD [61]. NiZn batteries are free from heavy toxic materials and are easily recyclable. Their chemistry supports high discharge rates due to low internal resistance while maintaining thermal stability and allowing for rapid recharging [62]. However, NiZn batteries are significantly more expensive than LA batteries.

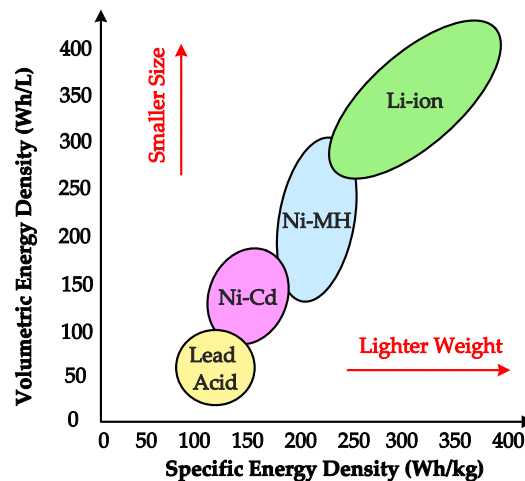


Figure 2.1: Specific energy density and volumetric energy density of various battery types.

Lithium-ion (Li-ion) batteries are highly favored in automotive applications due to their numerous advantages. They offer some of the highest specific energy (150–350 Wh/kg) and energy density (100–800 Wh/L) among battery technologies, as illustrated in Figure 2.1. Li-ion batteries can provide up to 3.6 V per cell, three times higher than NiCd and NiMH batteries, and feature a low self-discharge rate of about 1.5% to 2% per month. Unlike NiCd and NiMH, they do not suffer from memory effects and exhibit minimal charge loss when not in use [63,64].

Additionally, Li-ion batteries do not contain toxic cadmium, making them easier to dispose of than NiCd batteries. Despite these benefits, Li-ion batteries face several challenges, particularly concerning safety. They are prone to overheating, damage at high voltages, and, in extreme cases, thermal runaway and combustion. To mitigate these risks, safety mechanisms are required, which can add weight and potentially limit performance. Furthermore, Li-ion batteries are subject to aging, which reduces their capacity and reliability over time. Their high cost, approximately 40% greater than that of NiCd batteries, also poses a barrier to their broader adoption [64].

2.2.2 Supercapacitors

Supercapacitors (SCs), also known as Ultracapacitors (UCs), serve as an intermediate energy storage solution between conventional capacitors and batteries. They can be classified into three primary types based on their design, charge storage mechanism, and electrolytic materials used: Electric Double Layer Capacitors (EDLCs), Pseudo Capacitors (PsCs), and Hybrid Supercapacitors (HSCs) [65]. SCs offer greater energy storage compared to regular capacitors and deliver more power than batteries, with specific power ranging from 2–10 kW/kg and power densities from 40–120 kW/L. Their remarkable cyclability, typically exceeding 500,000 cycles, and long-term stability contribute to their appeal as energy storage devices [66].

For applications requiring pulse power, SCs need to feature high working voltages, substantial capacitance, and low resistance. However, the working voltage of most supercapacitors is generally below 3.5 V. To achieve higher voltages, SCs are often connected in series, which decreases the total capacitance and increases internal resistance, leading to higher power losses [67]. Connecting supercapacitors in parallel can improve capacitance and reduce internal resistance [52]. Additionally, supercapacitors charge and discharge rapidly, typically within seconds to minutes, and offer efficiencies between 90% and 94%. Despite these advantages, they are unsuitable for long-term storage due to their high self-discharge rate (approximately 20–40% per day) [34]. They also have a lower specific energy (2–5 Wh/kg) and energy density (10–30 Wh/L) compared to traditional batteries, making them ideal for hybrid applications where batteries handle long-term energy needs and supercapacitors address short-term power demands. Moreover, the high capital costs of SCs, around \$10,000 per kWh, present another challenge [68].

2.2.3 Flywheels

Flywheels are devices that capture energy in the form of rotational kinetic energy [69]. A Flywheel Energy Storage System (FESS), depicted in Figure 2.2, comprises five key components: the flywheel (a rotating disk), a set of bearings, a reversible electrical motor/generator, a power electronics unit, and a vacuum chamber [70]. This technology functions by using surplus electricity to power a motor that accelerates the flywheel to high speeds, thus storing kinetic energy. When electrical power is needed, the rotating flywheel drives the generator shaft to produce electricity [71,72]. The use of a vacuum chamber for the flywheel reduces aerodynamic drag, thereby enhancing the efficiency of the energy conversion process [73].

The energy stored in a flywheel is influenced by both its rotational speed and its moment of

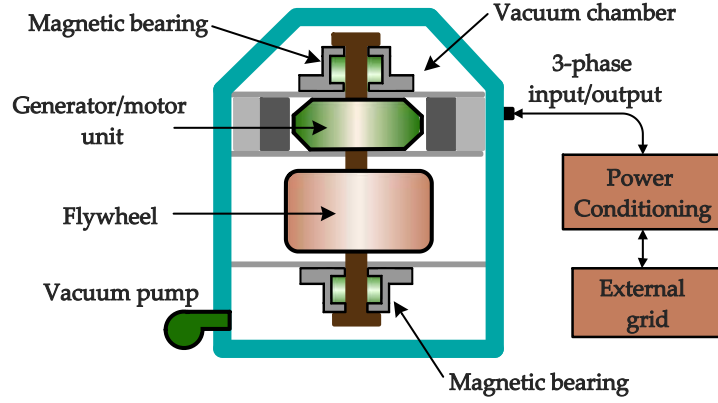


Figure 2.2: Schematic representation of a FESS.

inertia, as expressed by (2.1).

$$E_K = \frac{1}{2} I_m \Delta\omega_f^2 \text{ and } I_m = K m_f r_f^2 \quad (2.1)$$

where E_K is the amount of rotational energy stored in the flywheel, I_m is the flywheel's moment of inertia, m_f is the flywheel mass, ω_f is the flywheel speed, r_f is the radius of the flywheel, and K is the shape factor accounts for the flywheel's geometry.

FESS are categorized into two main types: low-speed and high-speed. Low-speed FESS, which typically use steel and operate below 6,000 RPM, have a specific energy of approximately 5 Wh/kg. Conversely, high-speed FESS utilize advanced composite materials like carbon fiber and can achieve rotational speeds of up to 100,000 RPM. These systems also employ non-contact magnetic bearings to minimize bearing wear and enhance efficiency, reaching a specific energy of around 100 Wh/kg. However, high-speed FESS generally incur higher costs compared to their low-speed counterparts [70].

FESS offers several benefits, including high roundtrip efficiency (90–95 %), an exceptionally long operational lifespan (15–20 years), low maintenance costs, and rapid response times [71, 74]. They are environmentally friendly as they do not produce greenhouse gases or toxic materials during operation [73]. Additionally, FESS can function across a broader temperature range compared to batteries [72]. Despite these advantages, they face challenges such as high capital costs (ranging from \$1,000 to \$5,000 per kWh) [41], significant self-discharge rates (3–20 % of stored capacity per hour) due to idling losses when not in use [70, 75], and limited storage capacities (3–130 kWh) [71]. Consequently, FESS is more suited for short-term energy storage and typically needs to be used in conjunction with other energy storage systems, such as batteries, for effective backup power solutions.

2.2.4 Hydrogen Tank Storage

The concept of using hydrogen as a fuel source for future vehicles has gained significant attention recently due to its abundance, environmental benefits, and impressive energy density of 120 MJ/kg, which is nearly three times higher than that of diesel or gasoline. Despite the global rise in popularity and sales of Battery Electric Vehicles (BEVs) over the past decade, the adoption

of hydrogen-based vehicles has been slower. One of the primary challenges is the difficulty associated with the onboard storage of hydrogen, which is highly flammable [76].

Compressed hydrogen storage technology has emerged as a leading solution for onboard storage due to its performance and practicality. This technology involves storing hydrogen gas in high-pressure tanks, which are categorized into five standard types: Type I, II, III, IV, and V. These types vary based on the tank material's weight, cost, ability to withstand high pressures, resistance to hydrogen diffusion, and durability against potential damage from the stored hydrogen. However, other storage methods, such as liquid and cryo-compressed hydrogen, are still being explored [77]. For hydrogen to be a viable alternative, advancements are needed to increase the energy density of storage systems, lower costs, and enhance compatibility with vehicle systems [44]. A comparative evaluation of various hydrogen storage systems considering factors like density, pressure, temperature, and cost is discussed by the authors of [78].

The stored hydrogen is then supplied to a Fuel Cell (FC), which converts it into low-voltage DC electrical energy. This energy can be used to power AC electric motors in vehicles through a high-step-up DC-AC power electronic converter. Unlike traditional engines, fuel cells operate without mechanical or thermal processes, requiring only air (oxygen) to function. The operational principle of the fuel cell is illustrated in Figure 2.3.

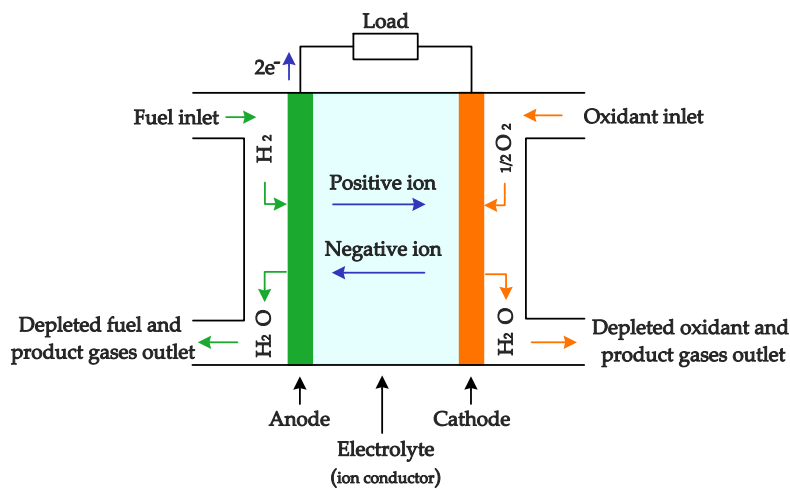
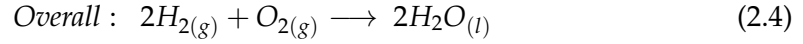
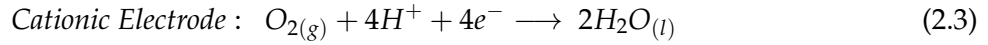
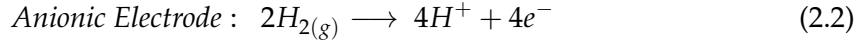


Figure 2.3: The operational principle of a fuel cell.

A FC, as depicted in Figure 2.3, consists of an anode, a cathode, and an electrolyte that allows ions, primarily positively charged hydrogen ions (protons), to migrate between the two sides of the cell. Hydrogen gas is introduced through channels to the anode, where it encounters a catalyst that facilitates the oxidation of hydrogen molecules. This process generates protons (hydrogen ions) and electrons. The protons move through the electrolyte from the anode to the cathode, while the electrons travel through an external circuit, generating direct current. At the cathode, another catalyst facilitates the reduction of hydrogen ions, oxygen from the air, and external electrons to form water [79]. The chemical reactions involved are summarized by equations (2.2) – (2.4).



A single FC produces a low voltage, typically less than 1.0 V, necessitating the use of a series stack of these cells to achieve a higher voltage suitable for practical applications. FCs are categorized based on the type of electrolyte used, which influences the cell's operating temperature and other characteristics. Higher operating temperatures enhance the cell's tolerance to impurities such as carbon dioxide and carbon monoxide but also increase the demands on system technology and materials, along with the startup time. Recent investigations into various FC types for onboard applications have shown promising results. These types include Proton Exchange Membrane Fuel Cells (PEMFCs), Solid Oxide Fuel Cells (SOFCs), Direct Methanol Fuel Cells (DMFCs), Alkaline Fuel Cells (AFCs), Molten Carbonate Fuel Cells (MCFCs), and Phosphoric Acid Fuel Cells (PAFCs). An overview of their major technical attributes, advantages, limitations, operational parameters, and efficiency is detailed in [80].

Table 2.1 gives a summary of the main merits and demerits of the ESSs spoken about in this section.

Table 2.1: Technical comparison of various energy storage technologies

Energy Storage Type		Energy Density (Wh/kg)	Advantages	Disadvantages
Battery	Lead Acid	25 – 50	- Technologically matured - Low material cost - No memory effect. - Low self-discharge rate - Investment costs are relatively modest. - Ease of maintenance	- Short cycle life - Low energy/power density. - Much charging time. - Environmentally unfriendly - Poor low-temperature properties - Not so reliability
	NiCd	40 – 70	- Long life - Recyclable - Wide temperature range	- Disposal issues due to cadmium toxicity - High memory effect - High cost
	NiMH	70 – 100	- Environmentally friendly - Long life cycle - High operating temperature range	- Service life reduces if deeply discharged - Very expensive. - Memory effect - Poor recycling
	NiFe	< 50	- Environmentally friendly - Resilient to overcharge and over-discharge	- High self-discharge - High production cost - Low open circuit voltage
	NiZn	50 – 60	- Environmentally friendly - Widetemperature range (-10° – 50° C) - Easily recyclable	- Very costly - Fast dendritic growth reduces life
	Li-ion	150 – 350	- Nearly 100% round-trip energy storage efficiency - Very high energy/power density - Relatively fast charging. - Long cycle life - Highly reliable - Low self-discharge - No memory effect - Lightweight	- High investment costs - Complicated charge management. - Safety issues due to thermal runaway. - Susceptible to damage at high voltages
Supercapacitor		2 – 5	- Wideworking temperature range (-40° – 60° C) - Quick charging time - High cycle efficiency - Eco-friendly - High number of charge and discharge cycles	- Very high self-discharge - High cost - Requires complex electronic control. - Low cell voltage - Voltage varies with the energy stored. - Low energy density
Flywheel	Low Speed	< 5	- High roundtrip efficiency - Long lifespan - Low maintenance cost - Fast response - Ecofriendly - Wide temperature range	- High self-discharge hence used only for short-term storage - Very costly - Limited capacity - Need for costly cooling devices
	High Speed	> 100		
Hydrogen Storage		33.3×10^3	- Almost emission-free hydrogen synthesis and processing. - Utilizing water to produce hydrogen. - Scalable solution via increased hydrogen tank capacity. - Long-term energy storage potential. - High energy density. - Possibility of using waste heat for utility purposes. - Commercial availability.	- Low efficiency of 25–45% - Expensive equipment costs for producing and processing hydrogen (fuel cells and electrolyzers). - Risk of gas explosion in the event of a system leak. - Low volumetric energy density hence needs large tanks. - Compressors and high-pressure hydrogen storage tanks are required. - Heat management required during charging.

2.3 Energy Storage Systems Models for Power Electronic Applications

Recently, there has been an increase in the use of ESSs especially batteries and SCs in the field of power electronics. To facilitate the accurate design and simulation of these systems, there is a need to make use of accurate and well-validated models.

2.3.1 Battery Models

Modeling batteries presents significant complexity and challenges. Accurate models are essential for developing Battery Management Systems (BMSs), which are crucial for monitoring and optimizing key performance indicators such as State of Charge (SoC), State of Health (SoH), temperature, and terminal voltage [81]. Three primary types of battery models are commonly used: empirical (or analytical), electrochemical, and equivalent circuit models. Among these, Equivalent Circuit Models (ECMs) are often favored for power management and BMS applications due to their straightforward linear structure, simple configuration, and relatively few parameters. These parameters are typically derived from experimental data and effectively represent the battery's dynamic behavior. Equivalent circuit models utilize electrical components like resistors and capacitors to simulate battery processes and can be applied across various battery types without needing specific chemical details [82]. However, the parameters of these models are influenced by operational conditions such as SoC, temperature, current direction, and aging. On the other hand, electrochemical models involve complex, non-linear partial differential equations with numerous unknown parameters, requiring extensive computational resources and time, often several hours or even days to perform simulations [83].

Figure 2.4a shows the Rint model, which forms the foundation for other equivalent circuit models. This basic model includes a variable voltage source and a series resistor. The voltage source represents the battery's open-circuit voltage (V_{OC}), which varies with SoC and temperature, while the internal resistance (R_i) simulates the battery's ohmic resistance, including the resistance of contacts, electrodes, and electrolytes [84,85]. This model, however, only addresses the static behavior of the battery and does not account for cell dynamics [86]. To address this limitation, the Thevenin model, shown in Figure 2.4b, introduces a parallel RC branch. This addition allows the model to capture the transient response of the cell during charging and discharging, as well as a parallel resistance to account for self-discharge at no load conditions [87]. Depending on the application, this leakage resistance may be omitted, as depicted in Figure 2.4c [88,89]. Further refinement is achieved with the dual-polarization model (DP) in Figure 2.4d, which incorporates a second RC branch to model both fast and slow cell dynamics [90]. Increasing the number of RC networks up to the fifth order can improve model accuracy but also raises computational complexity [91].

Another commonly used model is the PNGV model, illustrated in Figure 2.4e [92]. It resembles the model in Figure 2.4c but includes a large capacitance (C_b) to represent the variation in open-circuit voltage due to the accumulation and integration of load current over time during charging and discharging [93,94]. Adding more RC parallel branches can increase the model's order, enhancing its ability to reflect dynamic cell characteristics [95,96].

Models shown in Figures 2.4f–2.4h differ in that they feature different transient paths for

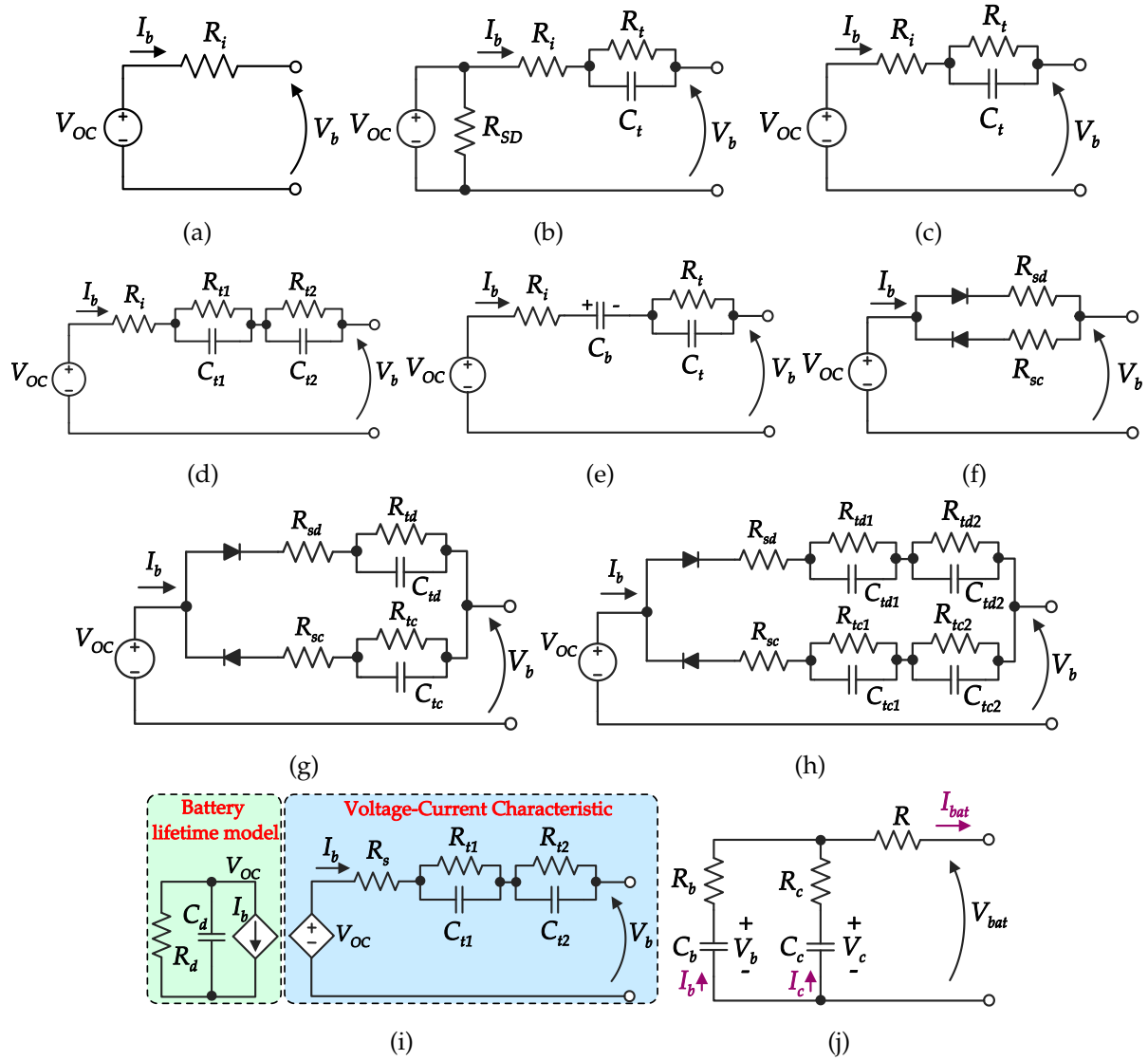


Figure 2.4: Battery equivalent circuit models: (a) zero-time-constant model (b) 1st order model with self-discharge effect (c) simplified 1st order model (d) 2nd order model (e) 1st order PNGV model (f) modified Rint model with path selection (g) 1st order Thevenin model with path selection (h) 2nd order model with path selection (i) runtime-based model (j) NREL RC battery model.

charging and discharging, controlled by two ideal diodes [81]. This setup allows for variable internal resistance and RC network values depending on the mode of operation (charging or discharging) [97]. As with other models, RC circuits in these paths are used to simulate dynamic responses to load current.

The runtime model, presented in Figure 2.4i and developed by [98] and further utilized by other researchers [99–101], consists of two separate circuits. The left circuit includes a capacitor (C_d) for storing total charge, a self-discharge resistor (R_d), and a current-controlled current source (I_b) to model battery capacity, SoC, and lifetime. The right circuit is similar to Thevenin-based models, with an RC network to represent transient responses. A voltage-controlled voltage source links the two circuits to depict the non-linear relationship between SoC and V_{OC} [99].

Lastly, Figure 2.4j illustrates a model developed by SAFT battery company for the National Renewable Energy Laboratory (NREL) and implemented in the Advisor software tool [92]. This model includes two capacitors (C_b and C_c) and three resistors (R_b , R_c , and R). The bulk capacitor (C_b) represents the main storage capacity, while the surface capacitor (C_c) captures fast charge/discharge behaviors ($C_c \ll C_b$). The terminal resistor (R) models internal resistance, R_b represents the surface propagation effects, and R_c reflects diffusion effects [102, 103].

For accurate modeling of these battery equivalent circuits, it is crucial that the component values (resistors and capacitors) are functions of SoC, SoH, current direction, and temperature. Moreover, to determine the parameters for the equivalent circuit models discussed, experimental testing is required. One widely used time-domain test for this purpose is the Hybrid Pulse Power Characterization (HPPC) technique. This method involves applying a series of current pulses to assess the battery's dynamic characteristics. During the test, the battery is subjected to controlled discharge and charge cycles while monitoring the terminal voltage, current, and temperature [104]. A typical HPPC current and voltage profile is illustrated in Figure 2.5.

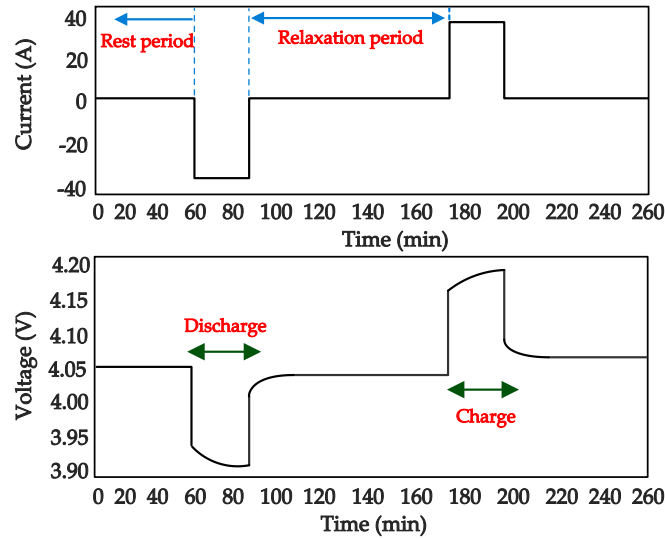


Figure 2.5: Example of HPPC test profile for battery parameterization.

2.3.2 Supercapacitor Models

With the growing use of SCs in EVs, accurately modeling their dynamic behavior is crucial. Such models can be used for performance evaluation, condition monitoring, estimating internal energy losses, SoC and SoH, and assessing overall efficiency. These elements are vital for developing an intelligent energy management system [105].

In literature, SC models are typically categorized into electrochemical models, ECMs, fractional-order models, thermal models, and intelligent models using Artificial Neural Networks (ANNs) and fuzzy logic [106, 107]. However, for power electronic system design and real-time energy management simulations, equivalent circuit models are particularly relevant. These models replicate the electrical dynamic behavior of SCs, such as voltage-current characteristics, using parameterized RC networks. They are straightforward and easy to implement since they are based on Ordinary Differential Equations (ODEs). Common equivalent circuit models for

SCs are depicted in Figure 2.6.

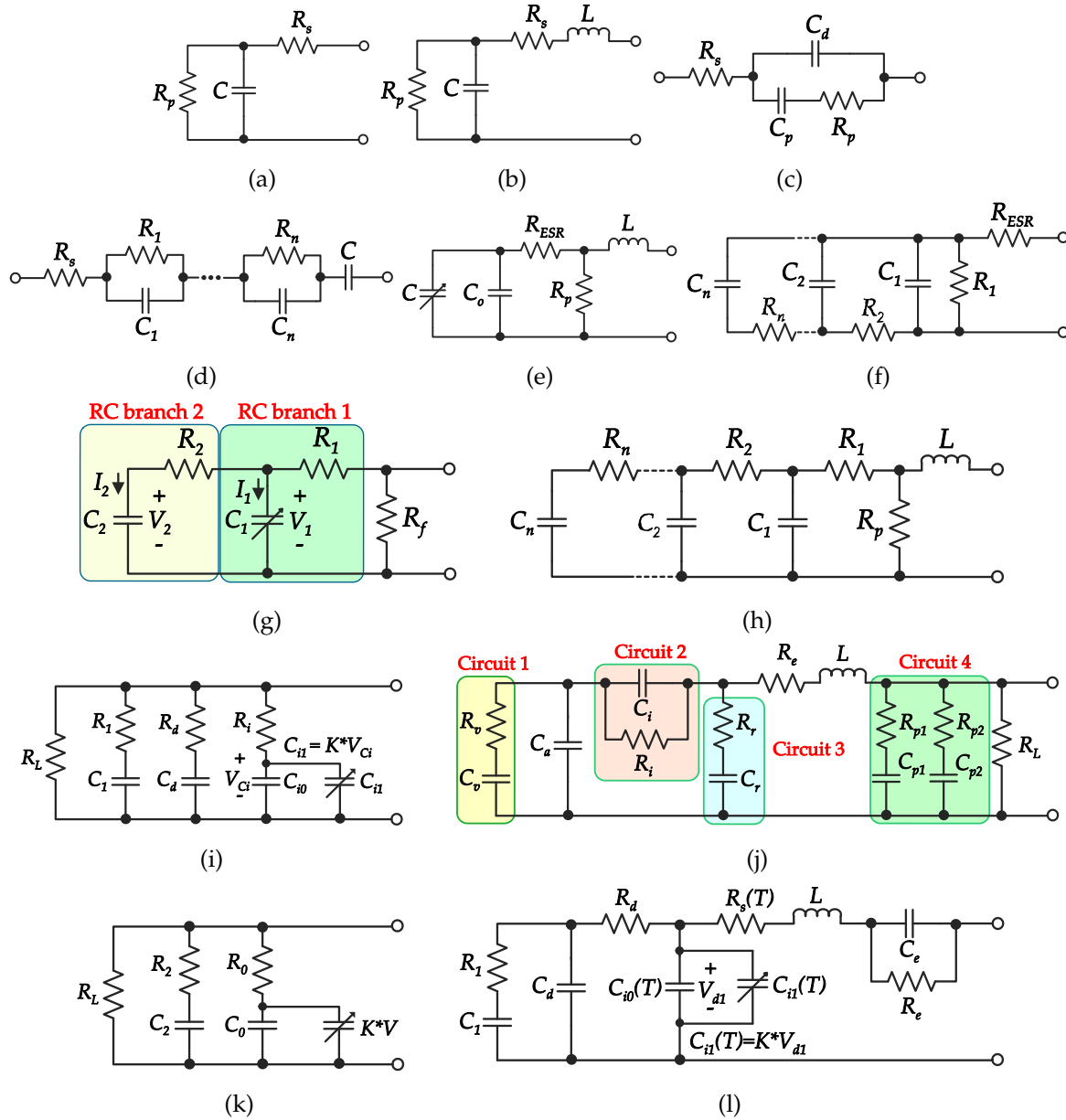


Figure 2.6: SC equivalent circuit models (a) classical equivalent circuit model (CECM) (b) first-order model (c) SC model using a Debye polarization (d) integer-order dynamic electrical circuit model (e) modified CECM (f) ladder circuit model (g) two-branch model (h) transmission line model (i) Zubieta Model (j) Rafik model (k) Faranda model (l) High-frequency model considering the temperature-dependency.

Figure 2.6a illustrates the classical equivalent circuit model, which consists of three main components: a capacitor (C), an equivalent series resistance (R_s) representing the ohmic losses during charge and discharge, and a parallel resistance (R_p) that accounts for long-term leakage currents. This model is widely used due to its simplicity and ease of parameter identification [108]. For short-term experiments, the parallel leakage resistance can often be disregarded because its value is significantly higher than that of the series resistance, further simplifying the model to just a series RC network [109].

A variation from the classical equivalent circuit model is the first-order model, or Randle model, shown in Figure 2.6b. This model includes an equivalent series inductance (L) to account for the inductance of the capacitor leads and current paths within the capacitor [110, 111]. This inductive effect becomes significant at high frequencies, typically above 100 kHz. Another approach, as modeled by the authors in [112], involves using a Debye polarization cell, depicted in Figure 2.6c. This is a modified version of the classical equivalent circuit, featuring a Faraday capacitance in series with the parallel resistance, termed charge transfer resistance in this context [113]. This model illustrates the chemical kinetics occurring within the EDLC.

The model shown in Figure 2.6d consists of a series resistance (R_s), representing the contact resistance at current collectors and the electrode and electrolyte resistances [114], along with a bulk capacitor (C) that represents the primary capacitance of the supercapacitor, and an unspecified number of RC networks. These RC impedance networks are designed to represent the distribution of capacitance and charge across double-layer interfaces [115]. Such models are particularly suitable for capturing high-frequency dynamics, such as fast charge/discharge cycles or significant power pulses [89].

Figure 2.6e presents another SC model proposed by [111], which is a variation of the classical equivalent circuit. This model can effectively describe the performance of the DLC in slow discharge applications, specifically characterizing the terminal behavior of the EDLC. The total cell capacitance (C_{cell}) is divided into a constant part (C_o) and a variable part that depends on the voltage across the cell (V_c), as described by equation (2.5), where K is a proportionality constant. In this model, the circuit parameters R_{esr} , R_p , and L retain the same interpretations as in the classical equivalent circuits.

$$C_{cell} = C_o + K V_c \quad (2.5)$$

The authors in [116] utilized a ladder circuit (Figure 2.6f) to model SCs. This circuit shares elements with the classical equivalent model, but the latter better predicts SC voltage under slow discharge due to the number of rungs in the ladder network.

Another popular model is the two-branch model (Figure 2.6g). The fast branch (RC branch 1) includes R_1 and a variable capacitor C_1 , capturing immediate SC response during brief charge/discharge cycles. C_1 consists of a constant component (C_o) and a variable component dependent on voltage V_1 ($C_1 = C_o + K V_1$) [117]. The slow branch (RC branch 2), with R_2 and C_2 , models energy distribution over longer periods. The parallel resistance R_f accounts for self-discharge, negligible in fast cycles [118, 119]. Including inductive effects can improve accuracy, especially at high frequencies.

The transmission line model (Figure 2.6h) represents the distributed nature of non-linear capacitances and electrolytic resistance in DLCs, essential for simulating both long-term and transient behaviors. However, it involves complex parameter determination and lengthy simulations due to numerous RC branches. Impedance spectroscopy typically derives its parameters, which may not fully account for high currents [120, 121].

Zubieta et al. [122] introduced a model (Figure 2.6a) with three RC branches to capture different time constants during SC charge and discharge, alongside a large parallel leakage resistance for self-discharge [123]. The last RC branch (R_i , C_{i0} , and C_{i1}) manages SC behavior in the initial seconds of operation, the second branch (R_d and C_d) handles responses from a few

seconds to about 10 minutes, and the first branch (R_1 and C_1) addresses longer periods [124]. These RC networks simulate ion diffusion and redistribution over time.

Rafik et al. [125] enhanced the Zubieta model (Figure 2.6j) by including frequency, voltage, and temperature-dependent parameters. This model contains four subcircuits, a high-frequency inductance (L), connection resistance (R_e), and principal capacitance (C_a). Circuit 1 models low-frequency voltage with R_v and C_v (a variable capacitance increasing linearly with voltage), Circuit 2 accounts for temperature-dependent electrolytic resistance at low frequencies, Circuit 3 adjusts capacitance C_a for average frequencies, and Circuit 4, similar to Zubieta's intermediate and long-term RC branch, describes temperature-dependent self-discharge. However, it requires extensive Electrochemical Impedance Spectroscopy (EIS) testing for parameter determination, which can be time-consuming [126, 127].

Faranda et al. [128] proposed a simplified version of the Zubieta model (Figure 2.6k), omitting one RC branch. This version simplifies parameter estimation and reduces required measurements, lowering error potential. The first RC branch includes two capacitors for main energy storage, while the second branch captures medium- and long-term response [108]. Faranda et al. also suggested a measurement-based parameter determination method, providing sufficient accuracy and ease compared to the complex Zubieta model [123].

Lastly, the model in [129] (Figure 2.6l) accurately represents SC dynamics up to 1 kHz, considering self-discharge, charge redistribution, and thermal effects. Similar to the Rafik model, it has a more complex parameter determination process, which is a major limitation [130].

2.4 Hybrid Energy Storage Systems for Electric Vehicles

2.4.1 Battery and Ultracapacitor Hybrid System

Battery-only ESSs often face limitations in providing sufficient power during peak demands and managing transient load variations inherent in electric vehicles and traction systems [131]. To address these challenges, oversized batteries are typically required, leading to increased weight, volume, cost, and accelerated degradation. Hybridizing battery systems with SCs offers a promising solution. This configuration effectively mitigates peak power demands, reduces battery stress, and extends battery lifespan [132]. Furthermore, the hybrid system excels at capturing regenerative braking energy, particularly during abrupt braking events, with the SC storing this energy for subsequent vehicle acceleration. The battery can then be dedicated to powering ancillary loads such as heating and air conditioning [100].

Numerous hybrid battery-supercapacitor topologies incorporating bidirectional DC-DC converters have been explored in literature to facilitate this integration, as illustrated in Figure 2.7 [131, 132]. The converter topologies for ESSs are primarily categorized into three types: passive parallel, semi-active, and fully active topologies.

The passive parallel topology (Figure 2.7a) is the simplest and most cost-effective, with the battery and SC connected directly in parallel to the DC-bus without power electronic converters. However, this configuration limits SC utilization as it mainly acts as a low-pass filter due to the battery's role in stabilizing the DC-bus voltage [133].

Semi-active topologies, depicted in Figures 2.7b– 2.7d, include a DC-DC converter to link

the battery or SC to the DC-link, allowing better control of energy and power flow based on current, voltage, or SoC [134]. Figure 2.7b extends the passive model by incorporating a DC-DC converter, which isolates the Energy Storage Device (ESD) from the load, thus preserving the ESD's operational voltage range. However, this setup still does not fully utilize the SC and lacks precise control over power distribution [135,136]. In Figure 2.7c, the SC is directly connected to the DC-link voltage, while the battery connects via a bidirectional DC-DC converter. This setup allows for flexible battery voltage adjustment and more efficient use of the SC, which functions as a low-pass filter [65,81]. The design facilitates effective power flow control by regulating battery current, enhancing the battery's lifespan and energy efficiency. However, the DC-link voltage experiences significant fluctuations during the SC's charge and discharge, potentially affecting the motor drive inverter's performance [133]. In Figure 2.7d, the positions of the UC and battery are swapped compared to Figure 2.7c. This setup allows full utilization of the SC's operational range, with the DC-link voltage, set by the battery, experiencing minor fluctuations but remaining more stable than in Figure 2.7c [137]. However, this design requires a large DC-DC

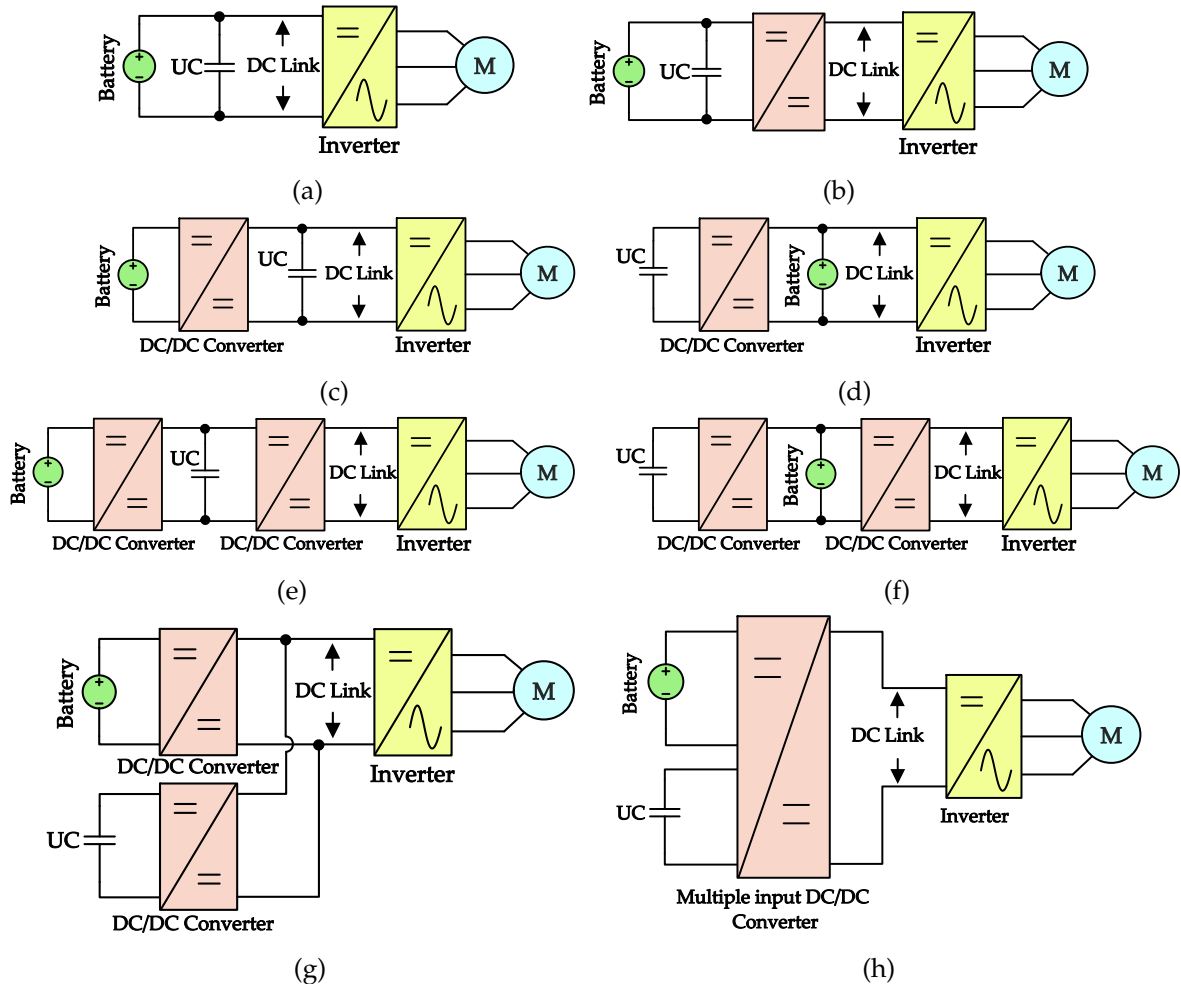


Figure 2.7: Battery and UC HESS (a) Passive parallel (b) Parallel semi-active topology (c) Battery-UC semi-active (d) UC-battery semi-active (e) cascaded battery-UC topology (f) cascaded UC-battery topology (g) multiple parallel-connected hybrid topology (h) multiple input converter topology.

converter to manage the SC's high power flows, increasing costs and reducing efficiency [138]. Additionally, the battery endures high charge/discharge current fluctuations, which can shorten its lifespan [139].

The configurations depicted in Figures 2.7e– 2.7h are referred to as fully active or fully decoupled topologies. Here, each ESD is connected to the DC-link via bidirectional DC-DC converters, enabling independent parameter control. This setup optimizes the use of each ESD based on their charge and discharge characteristics, thereby extending battery life. However, this comes with higher system complexity, cost, and increased losses compared to semi-active topologies [135].

Figure 2.7e features a DC-DC converter between the SC and the inverter, which extends the SC's operational range [140]. This setup allows the SC to handle sudden power demands, reducing stress on the battery, which can lead to a smaller, longer-lasting battery [141]. Placing the battery at low voltage terminals and the SC at an intermediate voltage level aids in balancing battery cell voltage [139]. The converter linking the battery to the SC is nearly the same size as the battery, while the converter from the SC to the DC link must handle peak power, making it larger and more expensive [141]. System instability can arise due to fluctuating DC link voltages, but this can be mitigated by swapping the battery and SC positions, as shown in Figure 2.7f, although this complicates battery cell voltage balancing. In this arrangement, the SC handles excess load currents beyond the battery's capacity. However, the converter connecting the battery to the DC link still needs to be large enough to manage peak loads, leading to high system losses due to the dual converters [142].

The fully active parallel-connected topology in Figure 2.7g offers the most flexibility among the configurations, as each ESD is connected to the DC-bus through individual DC-DC bidirectional converters, fully decoupling the power supply from the ESDs. This setup allows for the use of batteries and SCs with lower voltage ratings than the DC-link voltage and helps address the battery voltage balancing issue [143]. Additionally, this topology is fault-tolerant, able to function even if the battery or SC fails [140]. It also allows for precise control of key electrical variables like battery current, SC current, and DC-bus voltage. Unlike cascaded topologies, power flow to and from each ESD can be independently monitored and controlled, ensuring easy DC-bus stability. However, the use of two converters increases system size, cost, and control complexity. The multi-input configuration shown in Figure 2.7h, a more recent HESS alternative, shares these features with the fully active parallel topology.

Among these, the battery-SC active topology (Figure 2.7d) is most widely used due to its effective SC utilization, relatively low cost, high efficiency, and simpler control compared to fully active topologies [138].

2.4.2 Battery-Flywheel Hybrid System

Hybridizing flywheel storage systems with batteries or SCs can utilize the topologies shown in Figure 2.7. However, connecting the flywheel to the DC-bus requires a bidirectional 3-phase rectifier/inverter, as shown in Figure 2.8. During regenerative braking or other situations where excess energy needs to be stored, the flywheel's electric machine operates as a motor, and the power electronic converter functions as an inverter, increasing the flywheel's speed to store

rotational mechanical energy. Conversely, when energy is needed from the flywheel, the electric machine acts as a generator, and the power electronic converter serves as a rectifier to convert the generated three-phase AC voltage into DC voltage [144].

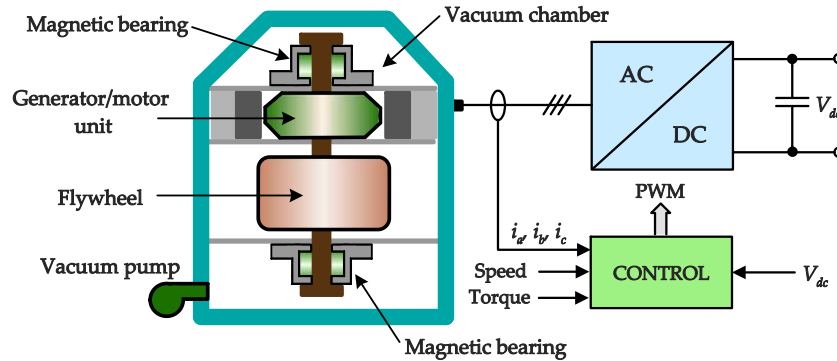


Figure 2.8: Flywheel-based hybrid energy storage system.

Figure 2.8 shows the flywheel control system black box, designed to regulate flywheel speed accurately and efficiently with a power electronic device [145]. The system inputs include flywheel speed, torque demand, engine power, DC bus voltage, and machine currents. These inputs allow control of the power to/from the flywheel. Common control strategies are Field Oriented Control (FOC) and Direct Torque Control (DTC). More advanced methods, like fuzzy logic, neural networks, and AI, are also available but are computationally intensive [146].

2.5 Energy Management Strategies (EMS) in EVs in the Presence of HESS

An effective EMS optimally allocates power across an EV's powertrain components, including the battery, electric motor, and auxiliary systems. This optimization enhances the longevity of these components, reduces operational and energy costs, improves overall system performance, boosts fuel efficiency, and lowers CO₂ emissions [147]. Beyond power distribution, the EMS monitors various HESSs, controls regenerative braking, and manages the thermal conditions of the ESS and motor using cooling and heating systems to maintain ideal operating temperatures and improve energy efficiency. Additionally, the EMS continuously assesses the SoH of powertrain components, detects faults, and provides diagnostic information and alerts to prevent damage and ensure safe operation. Advanced EMSs further enable bidirectional energy flow with the grid (V2G integration) and employ machine learning algorithms to anticipate and optimize energy needs [148].

In the last decade, extensive research has focused on EMSs for EVs. Despite the presence of several classification systems in literature, the most widely accepted categorization, as shown in Figure 2.9, divides EMSs into three main types: Rule-Based (RB), Optimization-Based (OB), and Learning-Based (LB) [149].

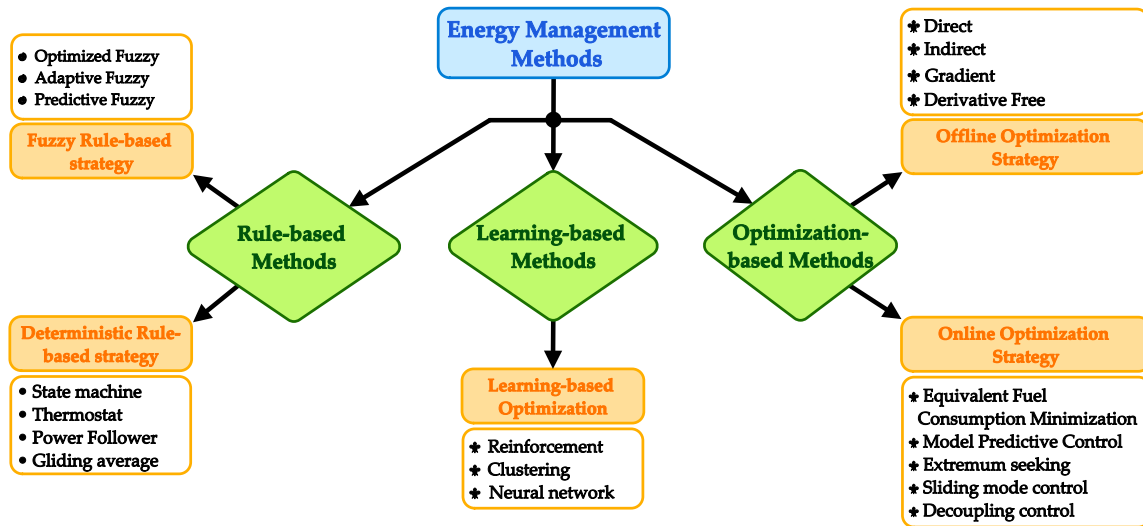


Figure 2.9: Classification of EMS used in EVs.

2.5.1 Rule-Based (RB) EMS

These strategies rely on predefined rules or heuristic algorithms and thresholds to manage energy flow in EVs. They are straightforward, require minimal computational resources making it ideal for real-time applications, and are the most implemented methods in EVs. They implement a simple set of *if-then-else* rules through look-up tables based on empirical data, expert knowledge or vehicle operating conditions such as battery SoC, acceleration, vehicle speed or driver power demand and are designed to optimize specific objectives like energy efficiency, performance, or battery life [150]. Despite their simplicity, RB strategies can be limited in handling complex or unforeseen scenarios. RB-EMSs can be further divided into two subcategories: deterministic EMSs and fuzzy-logic EMSs.

2.5.1.1 Deterministic RB EMS

Deterministic RB EMS for EVs utilize predefined rules to manage energy distribution efficiently. Key methods include State Machine Control, which uses a flowchart to manage powertrain operations by transitioning between states like charging and regenerative braking based on specific conditions such as SOC or speed [151]. The Thermostat Method, or on/off control, toggles system to maintain parameters such as battery SoC within a range, thus providing a straightforward control mechanism [152]. The Power Follower, or Baseline Control strategy aligns power output with the vehicle's instantaneous demand, particularly useful in Fuel Cell Electric Vehicles (FCEVs) for optimizing fuel cell efficiency [153]. The Gliding Average Strategy, or phlegmatising strategy, averages power demand requirement over time to smooth fluctuations, thereby reducing stress on batteries and other components [154]. Wavelet-Transform-Based Control analyzes energy consumption patterns using wavelets to optimize energy distribution, thus allowing the EMS to respond to transient events like rapid accelerations, improving overall system efficiency [155] while Low Pass Filtering reduces the impact of high-frequency variations in control signals, such as sensor noise, resulting in more stable and predictable EMS performance [156].

While these methods are valued for their simplicity and low computational needs, their lack of flexibility in adapting to dynamic driving conditions is a limitation, often necessitating the integration of advanced techniques like machine learning and optimization-based strategies for more comprehensive energy management.

2.5.1.2 Fuzzy RB EMS

Fuzzy RB EMS excel in handling complex and imprecise control tasks by merging numerical data with linguistic information through fuzzy logic. This approach is particularly useful in scenarios such as DC-link voltage control, where the system must adapt to varying conditions [157]. The operation of a fuzzy RB EMS follows a systematic three-step process: fuzzification, where precise input values are translated into fuzzy sets representing different degrees of truth; decision-making, where these fuzzy sets are evaluated according to predefined fuzzy rules to determine the appropriate control action; and defuzzification, which converts the fuzzy output into a specific control action or numerical value.

The effectiveness of fuzzy logic control is influenced by the design of its membership functions and the quality of the fuzzy rules. There are three primary fuzzy rule-based strategies: optimized, adaptive, and predictive. Optimized fuzzy methods improve performance parameters such as fuel efficiency, emission control, and state of charge by leveraging advanced optimization techniques like particle swarm optimization, genetic algorithms, bee algorithms, and proportion factor algorithms [158]. These methods focus on fine-tuning the system for specific performance goals. Adaptive fuzzy strategies incorporate self-adjusting mechanisms to enhance flexibility and adaptability. These often involve integrating fuzzy logic with neural networks, machine learning, and decentralized control approaches, allowing the system to learn and adapt to changing conditions in real-time [159]. Predictive fuzzy logic control anticipates future states and adapts control actions based on these predictions, enabling proactive adjustments to maintain optimal performance [160]. Each strategy is tailored to meet specific needs and challenges, contributing to more efficient and reliable performance in various operational contexts.

2.5.2 Optimization-Based (OB) EMS

These strategies use advanced mathematical models and computational optimization techniques to find the best control actions within a given set of constraints. They aim to optimize specific objectives, such as fuel efficiency or emissions reduction [161]. OB strategies can provide more efficient energy management compared to RB strategies but often require higher computational resources, making real-time implementation challenging. They are subdivided into two offline techniques or global optimization methods and online techniques which are real-time optimization methods.

2.5.2.1 Offline OB strategies

In EVs, offline-based optimization techniques are applied to enhance energy management and improve overall system efficiency. These techniques can be categorized into several distinct groups including direct, indirect, gradient and derivative-free techniques. Direct algorithms

like Deterministic Dynamic Programming (DDP) are used to optimize control strategies by breaking down the problem into stages, ideal for determining the optimal energy distribution across various known driving conditions [162]. Stochastic Dynamic Programming (SDP), which accounts for uncertainties such as varying road conditions and driver behavior, is employed to make robust decisions under uncertainty [163]. Shortest Path SDP (SP-SDP) can be utilized for route optimization, ensuring that energy consumption is minimized over a given path [164]. Indirect algorithms, such as Pontryagin's Minimum Principle (PMP), are used to derive optimal control laws for battery and SC management and power distribution [165], while Approximate-PMP (A-PMP) offers practical approximations when exact solutions are challenging [166]. Control Theory approaches, including Proportional (P), PI, and Proportional-Integral-Derivative (PID) controllers, are implemented for real-time adjustments in energy flow, ensuring stable operation and responsiveness but might not guarantee optimality [167]. The Newton-Raphson method is useful for solving nonlinear equations in battery charge models and optimizing power management systems.

Gradient-based algorithms like Linear Programming (LP) [168] and Quadratic Programming (QP) [169] are employed for optimizing battery/SC charge and discharge cycles based on linear or quadratic cost functions. Sequential Quadratic Programming (SQP) handles more complex, nonlinear optimization problems such as those found in advanced energy management scenarios [170]. Convex Programming (CP) ensures that solutions to optimization problems are globally optimal, crucial for managing energy distribution efficiently [171]. Derivative-free algorithms, or metaheuristic algorithms, are particularly beneficial in scenarios where gradient information is difficult to obtain, such as in complex battery management systems or dynamic driving conditions. Simulated Annealing (SA) and Genetic Algorithm (GA) help explore a wide range of possible solutions for optimizing energy consumption and vehicle performance [172, 173], while Multi-Objective Genetic Algorithm (MOGA) address scenarios where multiple performance metrics, like efficiency and range, need to be balanced [174]. Particle Swarm Optimization (PSO) [175] and Divided Rectangular (DIRECT) algorithms [176] offer robust search capabilities for finding optimal settings in energy management systems. Grey-Wolf Optimization (GWO) [177], inspired by the social hierarchy and hunting behavior of grey wolves, is used for optimizing complex energy management problems by simulating the process of hunting and tracking prey, effectively finding optimal solutions in dynamic and uncertain environments [178]. Finally, Game Theory (GT) can be applied in scenarios involving multiple vehicles, such as fleet management, where interactions and strategies among different EVs need to be coordinated for optimal collective performance [147]. Each of these techniques contributes to the efficient and effective management of energy resources in electric vehicles.

While these algorithms offer flexibility, they might not guarantee global optimality and often require careful parameter tuning. Hybrid approaches combining different techniques can leverage their strengths to achieve better performance.

2.5.2.2 Online OB strategies

An online strategy is considered a causal and local optimization approach because it does not need prior knowledge of the driving cycle and cannot guarantee an optimal solution in real-time

implementations. In contrast, the global optimization problem addressed by an offline EMS is formulated as an instantaneous optimization problem for real-time implementation, taking into account constraints related to computational time and memory resources [179].

Online OB EMS for EVs are categorized into two main approaches: instantaneous optimization and predictive EMS, each addressing different aspects of real-time energy management. Instantaneous OB EMS techniques focus on immediate decisions without considering future driving patterns. They include Equivalent Consumption Minimization Strategies (ECMS), which aim to minimize the equivalent fuel consumption by balancing energy use between the battery and fuel cell [180]. Adaptive-ECMS (A-ECMS) extends this by incorporating adaptive mechanisms to better handle varying driving conditions [181]. Robust Control techniques enhance system reliability by ensuring performance under uncertain conditions and disturbances. Extremum Seeking (ES) dynamically optimizes energy management in EVs by continuously adjusting control inputs to find the optimal performance point without requiring a precise model by continuously seeking the extremum (maximum/minimum) of a performance criterion [182]. Fractional Order Extremum Seeking (F-ES) enhances ES by using fractional calculus to better handle complex system dynamics and disturbances, providing more precise and responsive control [183]. Both techniques improve energy efficiency and system performance in real-time. Pseudospectral Optimal Control uses spectral methods to solve optimal control problems, offering high accuracy for real-time applications by discretizing the control problem into manageable segments [184].

Predictive EMS techniques focus on anticipating future driving conditions and making informed decisions based on these predictions. Driving Cycle Prediction involves forecasting the vehicle's future driving patterns to optimize energy management strategies in advance. Deterministic Model Predictive Control (DMPC) [185] uses a model of the vehicle to predict future states and control actions over a defined horizon, making real-time adjustments based on deterministic predictions. Stochastic Model Predictive Control (SMPC) incorporates uncertainty and probabilistic elements into the predictions, handling variations in driving conditions and improving robustness [186]. Sliding Mode Control (SMC) offers high robustness and resilience by employing discontinuous control actions to handle model uncertainties and external disturbances effectively [187]. Each of these online optimization strategies provides valuable tools for enhancing energy efficiency and performance in EVs by addressing real-time and predictive challenges.

2.5.3 Learning-Based (LB) EMS

LB EMS for EVs enhances energy management by employing adaptive and data-driven methods. These systems continuously improve their performance by analyzing real-time data and historical trends to make informed decisions. By dynamically adjusting to varying driving conditions, they optimize energy efficiency and system responsiveness. This approach allows EVs to adapt to diverse operational scenarios and improve overall performance even though requiring substantial data for training and validation [188].

Four main techniques can be used: Reinforcement Learning (RL), Supervised Learning (SL), Unsupervised Learning (UL) and Neural Network Learning (NNL). RL optimizes energy use by dynamically adjusting strategies based on performance feedback. The RL algorithm

learns from interactions with the environment, refining its actions to maximize efficiency and improve battery/SC life over time [189]. This approach adapts to varying driving conditions and user behaviors, enabling real-time optimization of energy consumption and overall vehicle performance. SL uses labeled datasets to predict energy needs, monitor battery SoH and manage power distribution, enabling precise forecasting and optimization based on historical data [190]. UL discovers patterns and anomalies in EV energy consumption data without predefined labels, revealing hidden insights to improve energy management [191]. NNL, including deep learning models, processes complex data to accurately predict and manage energy requirements, offering sophisticated and detailed control [192]. Each method enhances the adaptability and effectiveness of energy management in EVs through data-driven insights and continuous improvement.

2.6 Battery Charging Strategies

The increasing demand for lithium-ion batteries in EV has accelerated the development of novel optimal charging methodologies to enhance charging speed and reliability, reduce temperature rise during charging, improve charging efficiency while maintaining battery performance (extend battery life) [193]. Over the last decade, significant efforts have been made to create optimal charging procedures for commercial Li-ion batteries.

Generally, the various Li-ion battery charging strategies can be categorized into two classes based on internal mathematical models: model-free techniques, and model-based approaches.

2.6.1 Model-free Charging Techniques

These techniques are distinguished by predefined charging profiles with fixed current, voltage, and/or power limits, while neglecting battery dynamics responses. They include Constant Current (CC), Constant Voltage (CV), Constant Current - Constant Voltage (CC-CV), Multistage Constant Current - Constant Voltage (MCC-CV), Constant Loss - Constant Voltage (CL-CV), Constant Power - Constant Voltage (CP-CV), Constant Temperature - Constant Voltage (CT-CV), Pulse Charging (PC), Boost Charging (BC), and Sinusoidal Ripple Current (SRC) charging techniques.

The CC method shown in Figure 2.10a charges the battery while keeping the current constant at a predetermined threshold value throughout the charging procedure. This approach helps to prevent overcurrent even as the battery voltage rises [194]. When the SoC hits a certain threshold, the charging stops. The key issue here is the cumulative error present in the existing SoC estimation algorithms, which causes overcharging or undercharging, resulting in a shorter battery life cycle.

The CV charging technique (Figure 2.10b) uses a fixed voltage value to charge the battery. The charging process is complete when a predefined lower charging current limit is reached. This approach helps to avoid overvoltage and irreversible side reactions. This strategy, however, necessitates a high amount of current to maintain constant terminal voltage during the early stages of the charging process, which is extremely harmful to the battery crystal lattice as the battery temperature rises, potentially destroying the battery. Furthermore, this procedure is more time demanding than the CC method [195].

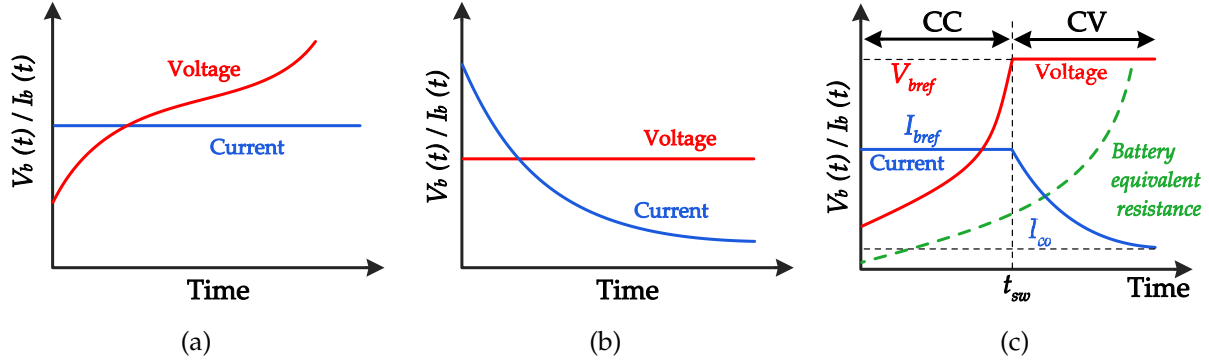


Figure 2.10: Battery charging strategies-I (a) CC charging (b) CV voltage (c) CC-CV charging.

The CC-CV method (Figure 2.10c) is the most used battery charging method. In the first phase, a fixed current is applied, causing the battery terminal voltage to steadily rise until it reaches a threshold/reference level. When this threshold is reached, the charging process progresses to the last phase, which involves constant voltage charging. During this phase, the battery current steadily falls, and charging ends when it reaches one-tenth of the reference current or a particular C-rating (usually between 0.05 C and 0.1 C). The equivalent resistance of the battery varies drastically during the charging process, posing a significant difficulty in control system design. The first phase allows for faster charging, while the second phase safeguards the battery from overvoltage. Moreover, the CV mode consumes a significant amount of charging time while contributing little to the amount of charged capacity (the CC mode accounts for more than 85% of the rated battery capacity) [196].

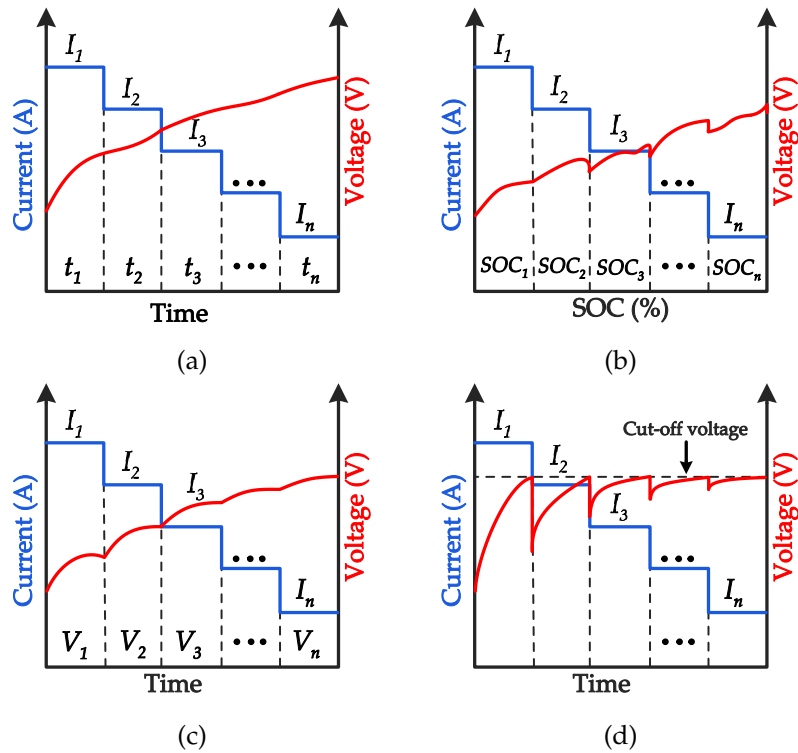


Figure 2.11: Current (**blue**) and voltage (**red**) profiles verses time during MSCC charging strategy for transition criteria from one stage to the next stage.

MCC-CV charging has been presented to overcome the time-consuming issue with the CC-CV approach, hence improving charging efficiency and extending battery life. It employs many CC stages (often two to five), followed by a final CV step. Higher current values are typically utilized for the early CC phases since the anode potential is less likely to become negative at the start of the charging process. However, some authors have taken the reverse approach, with current levels rising in later CC stages because of decreasing cell resistance. The transition from one stage to the next is determined by charging time, SoC, voltage threshold, or cut-off voltage, as seen in Figure 2.11 [197]. Time-based transitions are straightforward to execute, but there is no standard way for detecting when stages are switched from one to the next, while accurately estimating the SoC in SoC-based transitions is difficult. In a voltage threshold-based transition, different voltage thresholds are chosen to change the charging stage and current values. Moreover, there is no standard procedure for determining the threshold voltage at each level. Nevertheless, the voltage threshold-based transition is simpler to develop than the SoC-based transition. The cut-off voltage-based stage transition technique is the most widely used in literature. The battery manufacturer normally predetermines the cut-off voltage. When the cut-off voltage is reached when charging, the current is reduced (stage transitioning), and the charging process resumes until the cut-off voltage is reached again. This process is repeated until the predetermined number of phases is attained. Consequently, it is straightforward to set up.

CT-CV battery charging (Figure 2.12) is a technique that combines thermal regulation with CV charging to improve battery efficiency and safety. In this approach, the charging system initially adjusts the current to maintain a stable battery temperature, preventing overheating. When the battery reaches its set voltage, the charger maintains this constant voltage, while the current gradually decreases as the battery approaches its full charge. This method ensures proper charging, reduces the risk of overheating and overcharging, and helps extend battery life. Compared to the CC-CV method, the charging time is shorter, charging losses are lower but the implementation complexity is higher [198].

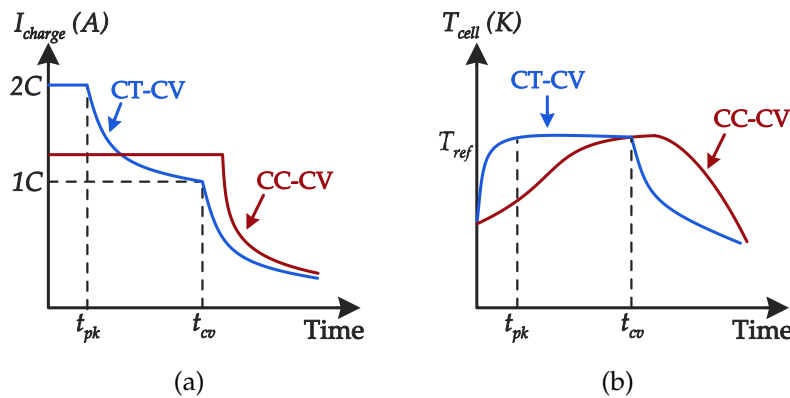


Figure 2.12: CT-CV charging strategy (a) Current profile (b) Temperature profile.

The CL-CV battery charging method (Figure 2.13a) optimizes the charging process by ensuring a constant power loss during the charging cycle, followed by a constant voltage phase. Initially, the charger regulates the current to ensure that the power losses inside the battery system remain consistent, which can aid in heat management and battery longevity [199]. When the battery hits a particular voltage threshold, the charging process switches to a constant

voltage mode, which keeps the voltage constant while progressively decreasing the current until the battery is fully charged. The power loss is calculated by squaring the current and multiplying it by the battery's equivalent resistance, which changes depending on the battery's SoC. This approach optimizes charging efficiency, safety, and battery life by carefully regulating electro-thermal stresses during the charging process.

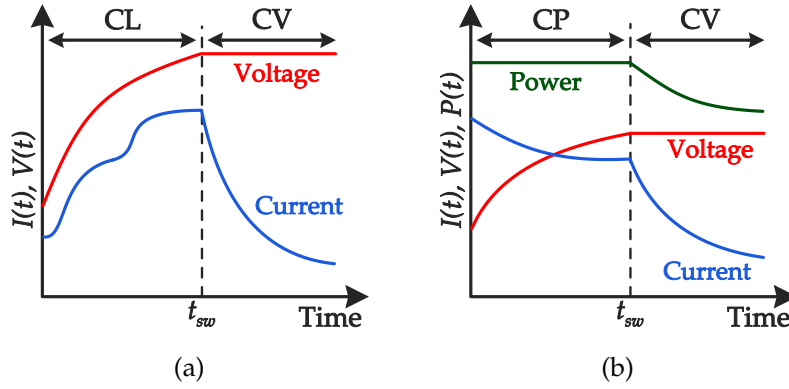


Figure 2.13: (a) CL-CV charging profile (b) CP-CV charging profiles.

The CP-CV charging method (Figure 2.13b) involves two separate phases. In the first stage, the charger supplies the battery with constant power, which means that the charging current decreases as the battery voltage increases, thus maintaining a constant power level. When the battery reaches its maximum charging voltage, the charging system switches to the CV phase. During this period, the voltage is maintained while the charging current gradually decreases as the battery continues to charge. This method improves charging efficiency, reduces charging time compared to CC-CV, and helps prevent overcharging [200].

PC can be interpreted as discontinuous CC or CV charging (for current and voltage pulses, respectively). The charging current is regularly interrupted by brief rest periods or discharge pulses. The primary characteristic of PC is the elimination or reduction of the battery's polarization voltage. Additionally, PC enhances safety by allowing relaxation periods between charge current pulses, giving the Li-ions time to properly intercalate and reducing the risk of dendrite formation. Current pulses can be classified into three categories based on current frequency, amplitude, and duty cycle: Constant Amplitude - Constant Frequency (CACF), Constant Amplitude - Varying Frequency (CAVF), and Variable Amplitude - Constant Frequency (VACF). CAVF-PC and VACF-PC have superior charging performance than CACF-PC [201].

The most common PC method is the Positive Pulse Current (PPC)-based CACF-PC shown in Figure 2.14a with some relaxation periods, where the design parameters are the peak charging current (I_p), the pulse's on-time (t_p), the relaxation time interval (t_r), and the pulse's total period (T). PPC can be used to increase battery life based on frequency of use, reduce charging time, and improve energy efficiency. Another pulse charging strategy is Negative Pulse Current (NPC), as shown in Figure 2.14b, with parameters such as peak charging current (I_p), peak discharging current (I_n), pulse on-time (t_p), relaxation time interval (t_r), negative pulse time (t_n), and pulse total duration (T). NPC can improve active material usage, leading to increased discharge capacity and extended lifetime. Furthermore, NPCs with lower frequency and amplitude have a larger charging capacity than NPCs with higher amplitude and frequency [197].

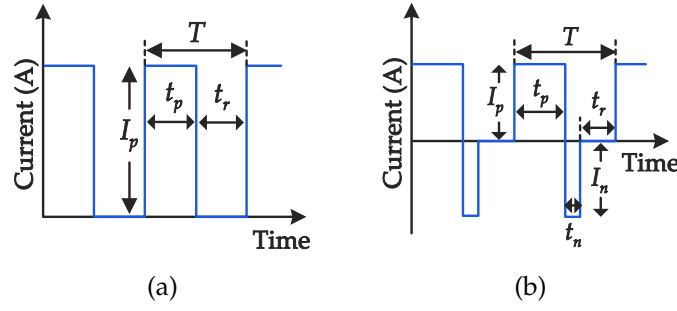


Figure 2.14: Pulse charging method (a) PPC (b) NPC.

The SRC charging method generates a charging current with two components: a DC component and a superimposed AC ripple one as seen in Figure 2.15. The frequency and magnitude of the ripple component are optimized such that the internal AC impedance of the batteries is minimized. The optimal frequency is typically obtained through Electrochemical Impedance Spectroscopy (EIS). Under the minimal internal impedance situation, heat generation during charge is reduced, potentially extending battery life and avoiding difficulties such as lithium plating, resulting in greater power and energy efficiencies as well as a shorter charging time [202]. Furthermore, the constant fluctuations in current can serve to condition the battery, making it a more efficient and safer charging method than standard CC-CV procedures. However, both PC and SRC charging methods have drawbacks, such as sophisticated implementation, large size, and high cost, preventing them from being widely used in real-world applications.

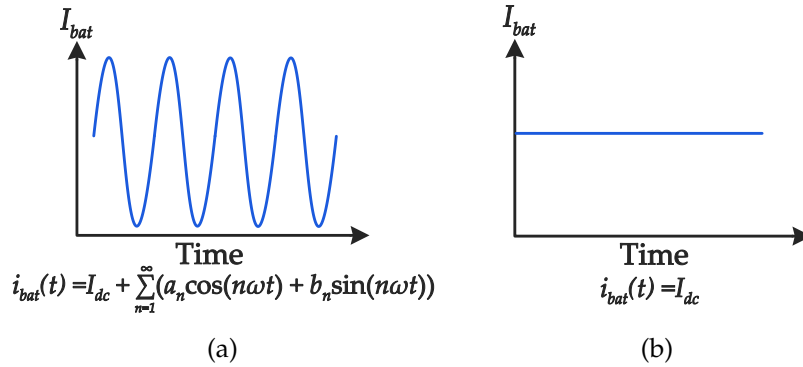


Figure 2.15: Battery Charging current with (a) ripple current and (b) dc charging current.

BC is an advanced technique designed to speed up battery charging, making it faster than the traditional CC-CV method. This approach starts with a high initial current during the early charging phase, which is then followed by a CC-CV phase with moderate currents. The initial boost phase can take different forms: it could use a simple CC profile (similar to MCC-CV), or a CV profile that quickly raises the battery to a maximum voltage using that high initial current (CV-CC-CV). Alternatively, it might involve a complete double CC-CV profile (CC-CV-CC-CV) as shown in Figure 2.16. Regardless of the method used, the boost charging stage should allow for higher currents (I_{boost}) or a higher maximum voltage (V_{boost}) compared to the following CC-CV phase. This results in significantly shorter charging times without negatively affecting the battery's lifecycle [203].

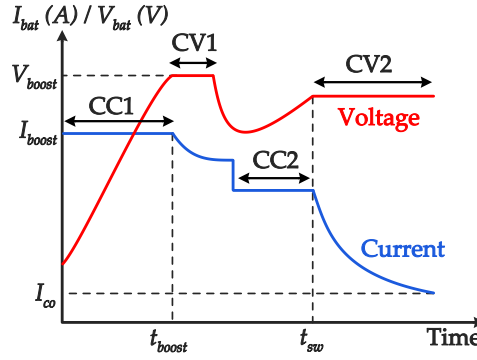


Figure 2.16: BC charging profile.

2.6.2 Model-Based Charging Techniques

Model-based charging methods calculate the optimal charging current of a battery by using its empirical or electrochemical model. They aim to optimize the charging process by controlling the polarization voltage.

2.6.2.1 Empirical Model-based optimized charging

To create optimal charging protocols, the empirical model-based charging technique based on the battery's ECM is combined with battery state estimators. The electrical elements of these ECMs are often generated from previous experimental data. Kalman filter family algorithms, particle filters, recursive least squares, sliding mode observers, and moving horizon estimators are the most used methods for estimating different battery states. The ECM parameters are reformulated and integrated into constrained optimization problems with one or more objectives. In these cases, first-order or high-order ECMs are utilized to characterize cell behavior, and various cost functions are selected to ensure maximum charging efficiency or minimum charging loss while fast charging. Charging loss is determined by internal resistance, current rate, and charging duration [204].

The thermal effect and battery aging produced by charging can be included into the basic ECM (which commonly includes a temperature model or a power loss model) using an electro-thermal-aging coupling model to reduce temperature rise or battery degradation during charging. Aside from the generally used lumped thermal model, which takes the cell as a whole, certain improved models that can distinguish between core and surface temperature or have better accuracy at higher speeds have also been presented. The aging impact is simulated using an expanded Arrhenius formula that takes into account the current rate, activation energy, total discharged capacity, temperature, and so on [205].

After establishing the framework for the optimization problem, an appropriate optimization algorithm should be utilized based on the cost functions and constraints. Conventional approaches include the Pontiac minimum principle, dynamic programming, the genetic algorithm, the Legendre-Gauss-Radau (LGR) pseudo-spectral method, and the minimum-maximum strategy. ECMs can capture the exterior properties of the battery, are computationally fast and simple, but do not account for the battery's internal potential change, internal chemical reactions, or Li-ion concentrations.

2.6.2.2 Electrochemical Models (EM)

Electrochemical model-based charging uses mathematical models to mimic critical internal chemical and electrochemical processes within the battery, such as ion transport, ion concentration distribution, electrode potentials, and temperature gradients. These models provide a complete picture of the battery's state, allowing the charging system to dynamically alter current, voltage, and temperature parameters to achieve peak performance [206]. The Pseudo Two-Dimensional (P2D) model is the most popular electrochemical model. However, solving the Partial Differential Equations (PDEs) in the full order model is computationally intensive. As a result, efforts have been undertaken to lower the order of the Full Order Model (FOM) in order to obtain quicker computational speed while maintaining comparable fidelity, allowing for realistic application. Following that, the One-Dimensional (1D) model, Single Particle (SP) model, Simplified P2D (SP2D), and SP-thermal model are some of the most well-known EM-based charging techniques developed to overcome the issues related to the P2D model. [207] provides a thorough analysis of the existing EMs found in literature.

2.7 Conclusion

In this chapter, we have explored the current state of the art in ESSs for EVs, providing a comprehensive overview of the technologies and strategies that underpin modern EV energy management. Beginning with an introduction to various types of energy storage systems, we examined the characteristics, advantages, and limitations of batteries, supercapacitors, flywheels, and hydrogen storage, highlighting their roles in EV applications. We then delved into ESS models used in power electronic simulations, focusing on the ECMs for batteries and supercapacitors, which are essential for accurate and efficient system design.

The chapter also covered the integration of HESSs in EVs, where the combination of different storage technologies, such as battery-supercapacitor and battery-flywheel hybrids, offers enhanced performance, particularly in terms of power density and energy efficiency. We then explored various EMS in the presence of HESS, discussing the strengths and applications of Rule-Based, Optimization-Based, and Learning-Based EMS approaches. Lastly, we reviewed battery charging strategies, comparing model-independent techniques with more advanced model-based methods, including those based on equivalent circuit models and electrochemical models.

Overall, this chapter has laid the foundation for understanding the complex interplay between different energy storage technologies, their modeling, hybridization, and management strategies within EVs. These insights are crucial for the development of more efficient, reliable, and sustainable EV systems, setting the stage for the subsequent chapters that will further investigate the design, optimization, and implementation of advanced battery charging and management solutions for EVs.

Chapter 3

Power Converters for Electric Vehicle Charging Stations

3.1 Introduction

EV charging stations are the backbone of the EV world/ecosystem, serving as a vital link between the AC grid and the vehicles. Charging stations assist in recharging EV batteries, allowing them to work constantly and hence increase driving range. The availability and accessibility of charging stations is critical to the broad adoption of EVs, as they have a significant impact on how easy and feasible it is to own and operate an EV [208].

Developing EV charging infrastructure offers a number of financial, organizational, and technological challenges that must be overcome in order to assure its effectiveness and reliability. Financially, the high initial capital costs for equipment procurement and installation, electrical grid upgrades, and site acquisition are significant barriers. Moreover, the Return On Investment (ROI) is uncertain, particularly during the early stages of charger deployment, when the utilization rate is low and unpredictable, hence discouraging investors. Furthermore, the high cost of modern fast charging stations, combined with a lack of government funding in many locations, makes charging infrastructure expansion even more difficult [209]. Finding a suitable location for the charging infrastructure remains a big organizational challenge [210]. Technically, there is a scarcity of sufficient charging infrastructure/stations capable of rapidly charging these vehicles/buses [211]. Therefore, territorial plans must be developed to establish battery charging stations capable of charging various types of EVs. In general, they should be placed along main routes at appropriate distances and strategic positions [212]. Some approaches have been developed to determine the optimal quantity and location of charging stations like the one proposed by authors of [213] for electrical mobility in airport regions.

Furthermore, the installation of these charging stations to give electrical power to the battery places significant stress on the power grid because these stations often require large amounts of power from the AC grid in a short time period. As a result, several grid operating metrics suffer, including voltage stability, reliability, power losses, and harmonics [214]. There are numerous publications in literature that analyze and propose various solutions to the negative effects of integrating EVs into the AC grid, some of which include including energy storage devices and using chargers as a source of Reactive Power Compensation (RPC) [215]. The authors of [214]

investigated the impact of charging stations on the distribution grid's reliability. A similar study was conducted in [216], in which the authors investigated the impact of charging stations on power quality in the Medium Voltage (MV) distribution network. The use of bidirectional power electronic converters, where the vehicle delivers power to the grid (V2G), can also increase grid stability, reliability, and power losses [217]. The V2G concept is based on the idea that when power demand is high, excess energy stored in EVs can be delivered back into the grid, but when demand is low, excess energy can be stored in EV batteries to avoid waste [218]. Thus, EV owners can purchase electricity from the grid at a cheap cost and resell it to the grid at a higher price, resulting in some gains for the EV owner. Finally, the standardization of charging protocols and connectors is essential to ensure compatibility across different vehicle models and charging networks.

Figure 3.1 depicts two types of EV battery chargers: on-board and off-board. On-board chargers are fitted in EVs alongside storage batteries; nevertheless, their power output is limited by weight, space, and cost constraints [219]. Off-board EV chargers have no size or weight constraints because they are situated in bus terminals and depots, garages, parking lots, and even on-route, where available space is usually greater [220].

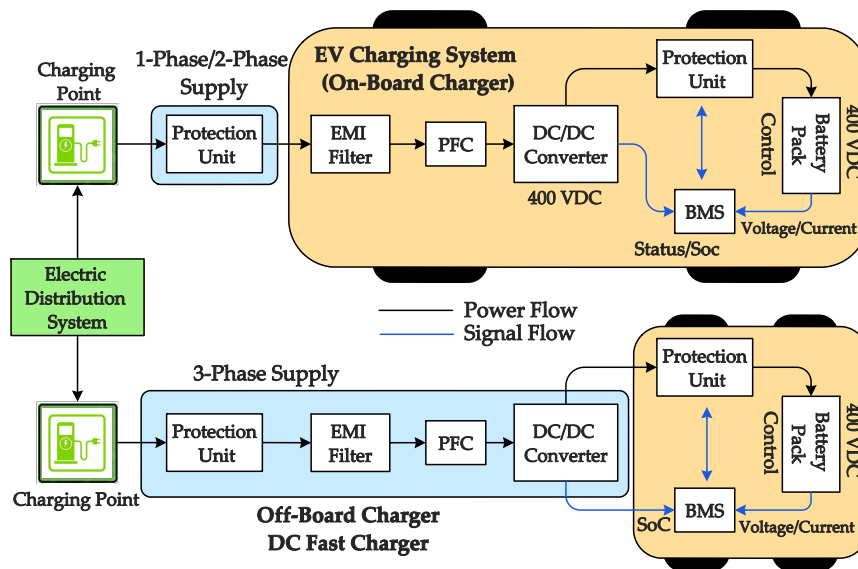


Figure 3.1: On-board and off-board charging system.

Battery chargers are categorized into three levels based on charging time, power level, and supply voltage. Level I chargers are slow, whereas level II chargers are semi-fast, and both use a single-phase grid power. They are typically utilized in on-board charging systems. Level III chargers, on the other hand, are designed for fast charging EVs and require a three-phase power supply. Off-board chargers are classified as Level III [221]. To further reduce EV drivers' range anxiety and to be really competitive with the internal combustion engine (ICE)-based refueling process, DC Extreme Fast Charging (XFC) has emerged as a potential option in which EV batteries are fully charged in less than 10 minutes with a power rating higher than 350kW. However, the significant amount of power transfer between the grid and the EV creates issues which need to be researched and mitigated [222]. Table 3.1 demonstrates several characteristics of these chargers, grouped according to their power levels [222, 223].

Table 3.1: Main characteristics of EV battery chargers.

Feature	Level 1	Level 2	Level 3	Extreme Fast Charging (XFC)
Grid voltage	120 VAC (US) 240 VAC (EU)	240 VAC (US) 400 VAC (EU)	300 – 600 VDC	800 VDC
Power range [kW]	≤ 3.7	3.7~22	50 - 350	350
Approximate charging time	11 – 36 hours	1 – 6 hours	0.2 – 1 hour	10 minutes
Charger topology	On-board	On-board	Off-board	Off-board
Grid supply type	1-phase	1 or 2 phase	3-phase	≥ 3-phase
Charging type	Slow charge	Semi-fast charge	Fast charge	Ultra-fast charge
Battery capacity [kWh]	15 – 50	15 – 50	15 – 50	20 – 50
Typical use	Charging at home or office	Charging at private or public outlets	Commercial, just like a filling station	Commercial
Connectors	SAE J1772 (US)	GB/T 20234.2 (CHINA), SAE J1772 (US), Mennekes (EU), CCS 1,2	CHAdeMO, Tesla superchargers, CCS Combo 1, 2, GB/T 20234.3	CCS Combo 1, 2, CHAdeMO, GB/T, SAE J2826/2 and SAE J2847/2

A crucial component of EV charging stations is the power electronic converter. They manage and control the flow of energy between the AC grid and the vehicle's battery, enabling the conversion of AC grid power into DC power stored in the battery and vice versa. By efficiently managing power flow, converters ensure safe and reliable charging while optimizing charging time and minimizing losses. Moreover, they control the voltage and current levels, protecting both the charging station and the battery from damage, thus extending battery life. Furthermore, the power electronic topologies for these EV chargers must be designed to have low Electromagnetic Interference (EMI), low Total Harmonic Distortion (THD), high power factor, and galvanic isolation with the grid [224].

In this chapter, we will look at the various EV charging strategies and methods, particularly those employed with electric buses. Furthermore, we examine cutting-edge EV charging infrastructure, appropriate power converter topologies for the AC-DC and DC-DC power stages of off-board DC fast chargers and their control systems. Partial Power Processing (PPP) converters will also be discussed as a means of minimizing converter losses thus improving system efficiency. Finally, we look at multiport EV chargers which are designed to integrate multiple energy sources and loads thus allowing for optimized energy flow management.

The remainder of this chapter is organized as follows: Section 3.2 outlines the various charging strategies for electric buses (overnight charging, in-motion charging, and opportunity charging). We also look at the various techniques that are commonly used to charge these buses:

pantograph charging, plug-in or conductive charging, and ground-based or inductive charging. In Section 3.3, we discuss the various EV charging station architectures, while the front-end and back-end power converter topologies and control algorithms utilized for fast conductive charging of electric vehicles/buses are provided in Section 3.4. In Section 3.5, we introduce PPP converters or Reduced Dissipation Converters (RDCs), which are a relatively new concept in electric transportation systems. Section 3.6 describes EV charging based on multiport converters, while Section 3.7 concludes the chapter.

3.2 Charging Strategies and Methods for Electric Buses

There are three primary strategies for charging e-buses: overnight or depot-only charging, in-motion or online charging, and opportunity or flash charging [215,225]. Buses that only charge overnight have large batteries with high capacity (usually 200-500 kWh), allowing them to be operated throughout the day without needing to be recharged. These buses typically run on shorter, less congested routes (less than 100 km) [226]. The buses are charged by slow DC chargers with a plug-in cable interface (usually 50-150 kW). Online charging, on the other hand, enables buses to charge while traveling. Opportunity charging refers to a scenario in which buses are charged not only at the depot, but also when they stop at a bus stop (terminal stops and on-route intermediate stops), which occurs throughout the day. On-route chargers (Opportunity and Online chargers) allow buses to complete their routes with less battery capacity (typically 50-90 kWh), resulting in a more efficient system [227]. However, due to their high power requirements (typically 150-450 kW), these chargers are more expensive than depot chargers [211].

Figure 3.2 shows the three main charging techniques available: conductive charging, induction (or wireless) charging, and battery switching [228–230]. Plug-in and pantograph charging are both classified as conductive charging because conductors are utilized to transfer energy from the charging infrastructure to the e-bus. In plug-in charging, a connector or cable from the charging infrastructure is manually connected into the bus to begin charging. Inductive charging generates an electromagnetic field between a transmitting coil on the road surface and a receiving coil at the bottom of the e-bus [231,232]. In contrast, pantograph charging charges the bus automatically via overhead connectors.

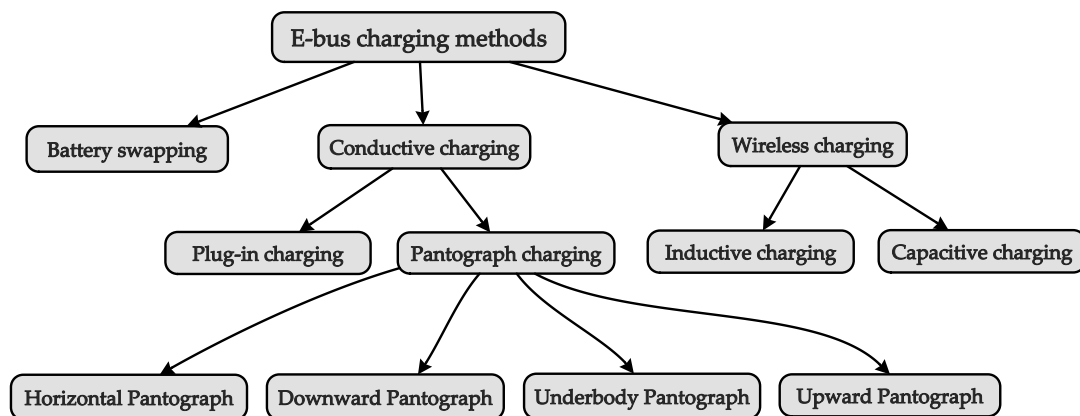


Figure 3.2: E-bus charging methods.

Pantographs are classified into four types: downward (infrastructure-mounted or top-down or inverted), upward (roof-mounted or bottom-up), side insertion (horizontal), and underbody pantograph, as illustrated in Figure 3.3 [233,234]. The upward pantograph is the easiest to install technically, and the charging process is controlled/initiated by the driver, eliminating the need for a WiFi connection for communication. It behaves similarly to a standard Combined Charging System (CCS) plug. The ISO 15118 and IEC 61851 protocols are used for communication [235]. However, the downward pantograph requires a WIFI connection to communicate with the bus, which is accomplished using the OppCharge standard. The advantage of this pantograph version is that the bus's height is reduced, allowing it to travel under low-clearance bridges, and the weight of the system is reduced, which is especially useful when the system is at its maximum weight limit. The horizontal pantograph operates similarly to an inverted pantograph, with the moving component on the charging infrastructure side. Communication can take place utilizing either the ISO 15118 standard, which is based only on a pure conductive system without WIFI, or the OppCharge standard, which includes WIFI. The underbody pantograph can be fixed underneath the bus and connected to the infrastructure, as with a roof-mounted pantograph, or it can be placed on the ground and moved upward onto the bus, as with an inverted pantograph.

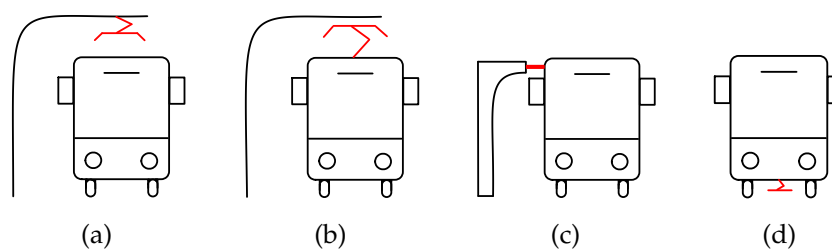


Figure 3.3: Different types of pantographs (a) downward; (b) upward; (c) horizontal; (d) underbody.

Battery swapping involves physically replacing a drained battery pack with a charged battery. When compared to the previously described conductive or wireless techniques, the swapping process is extremely quick, taking only a few minutes using automatic robotic arms. Furthermore, the batteries at swapping stations could serve as grid support units, delivering power to the grid during peak hours and charging during off-peak periods [236]. Currently, there are certain barriers to implementing battery switching, such as a relatively high initial setup cost and the necessity for huge storage space to store both depleted and fully charged batteries [237].

The optimal charging technique is determined primarily by the strategy you intend to employ. Depot-only solutions necessitate the fewest additional resources. The depot-only solutions are the most basic and primarily plug-in. Pantographs are more commonly used for opportunity charging. Induction charging is more expensive and complex to create and implement than the other two options.

3.3 Architectures for Fast Charging of Electric Vehicles

Generally, two types of DC rapid charging architectures may be identified [238]: AC-bus architecture and DC-bus architecture, as shown in Figures 3.4a and 3.4b. Figure 3.4a depicts

how the AC-bus system connects the distribution network to the three-phase AC bus via a step-down Low-Frequency Transformer (LFT). Each charging station requires a separate AC-DC rectifier, while connecting Renewable Energy Sources (RESs) and ESSs to the AC bus necessitates additional DC-AC inverters. This strategy, as a result, greatly increases the number of power electronic conversion stages that connect the various elements, increasing system complexity, cost, and power losses, and lowering overall efficiency [217]. The benefits of employing the AC-bus approach include rectifier and inverter technology availability and maturity, AC switchgear and protective devices availability, and well-established protocols/standards for AC power distribution systems.

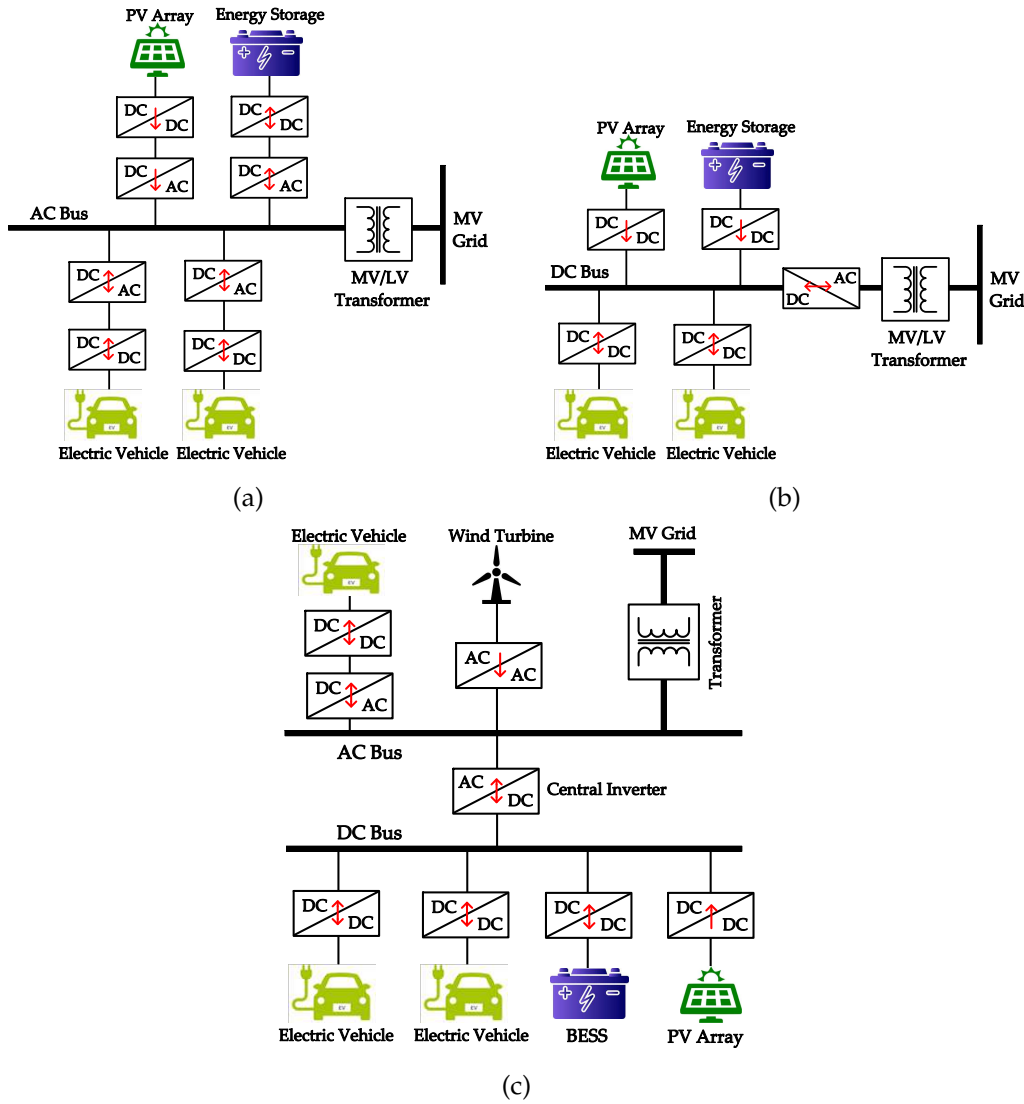


Figure 3.4: Fast charging stations configurations with: (a) AC-bus coupling; (b) DC-bus coupling; (c) Hybrid architecture.

An LFT is used in the DC-bus system to provide galvanic isolation and step down the distribution system voltage. The resulting low voltage is supplied into a central frontend AC-DC rectifier, which produces a common DC-bus voltage. As the number of power electronic conversion stages is reduced, this strategy becomes a more efficient means of connecting DC

ESDs and RESs. The fundamental issue with this technique is the absence of DC protection schemes and standards [239]. Table 3.2 provides a summary of the main differences between the AC and DC bus architecture.

Table 3.2: Comparison Between DC and AC Connected EV Charging Architecture

Architecture	Advantages	Disadvantages
AC Bus	• Highly available and mature technology with standards • The complexity of the protection devices is low • Able to direct usage for local loads • Stability and scalability are high • Reliable switching and control techniques • Ability to control active and reactive power	• A large number of converters reduce rated power and efficiency • High cost due to multiple converters • Additional conversion stages are required for fast chargers to avoid harmonics • Difficult to achieve high power quality and stability • Complex to integrated RESs and required additional DC/DC stage
DC Bus	• Provide high efficiency and power density due to low components • The control strategy is simple • Low cost and flexible configuration which can integrate ESS and RES easily • Helps to reduce the impact of high penetration of EV loads on the power grid • Reduction in frequency fluctuation	• Complexity may increase with the additional energy sources • Requires protection devices to withstand sudden changes • The central converter needs server conditions due to an increase in nominal power

In addition to the AC and DC bus architectures, Figure 3.4c depicts the hybrid architecture, which combines both AC and DC buses. As seen, an LFT offers galvanic isolation between the grid and the AC bus, and the EV, RESs, and ESSs are connected to both the AC and DC buses via separate converters. This arrangement allows both the AC and DC buses to operate simultaneously, eliminating the need for additional power conversion stages. The system uses a single bidirectional converter to connect the AC and DC buses, known as an interlink power converter, and corresponding buses can be utilized to connect AC and DC loads. The interlink converter can maintain an energy balance between both sides while operating according to load requirements. This architecture is more reliable, adaptable, and efficient than the standalone AC and DC bus systems [240].

Figure 3.5 depicts two types of DC-bus systems: unipolar and bipolar. The unipolar DC-bus system uses a two-wire configuration, resulting in a single DC voltage level, and is typically used with two-level voltage source converters like the Vienna converter. The bipolar DC-bus system uses a three-wire configuration, resulting in two DC voltage levels, and is compatible with three-level voltage source converters like the Neutral Point Clamped (NPC). Although the bipolar system has higher design and control complexity than the unipolar system and necessitates voltage balancing algorithms, it is more flexible, resilient, and fault tolerant [241].

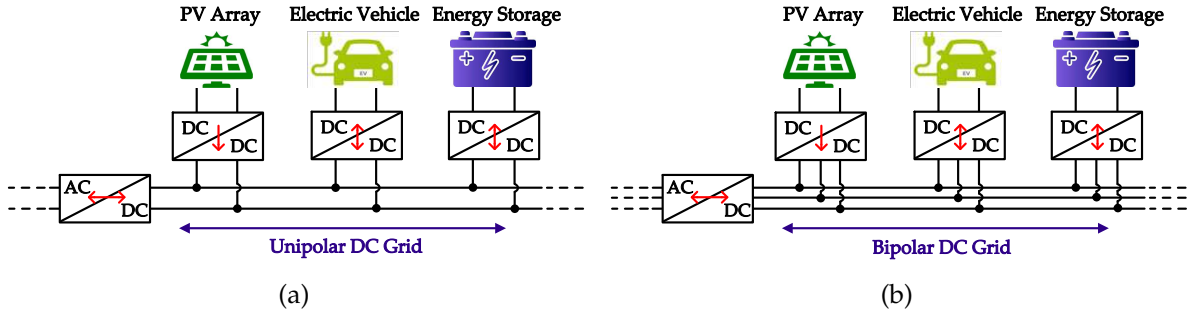


Figure 3.5: DC-bus configurations (a) unipolar DC-bus (b) bipolar DC-bus.

3.4 Converter Topologies for EV Charging Systems

Several AC-DC and DC-DC converter topologies for fast charging EVs have been presented in literature. To design the fast-charging station, we must select the AC-DC and DC-DC converters that offer the best results in terms of system requirements from a list of possibilities. The following subsections cover the various grid-connected AC-DC and DC-DC converters that are routinely used for battery charging.

3.4.1 Front-end AC-DC Converters Topologies

These topologies convert the three-phase AC grid voltage into DC bus voltage. They must meet certain performance requirements, including a high power factor, sinusoidal input current (low harmonic distortion), controlled output DC voltage, EMI compliance, minimal complexity and cost, and sustained operation if one phase fails [221, 242]. Figures 3.6, 3.7 and 3.8 show promising topologies for addressing the aforementioned requirements while running at high power densities.

Figure 3.6a shows the Vienna rectifier topology. Due to the presence of three-phase bridge diodes, it can only generate unidirectional power flows, rendering it unsuitable for V2G applications [243]. The bidirectional switches are organized in a star layout, with the neutral point connected to the center of two capacitors. Consequently, it functions as a three-level boost converter, yielding a smaller AC inductor. This converter provides a controlled output voltage, low EMI, and reduces voltage stress on power switches, which are stressed at half the output voltage. It does, however, have a high control complexity, requires DC-link capacitor voltage balancing algorithms, and has restricted reactive power regulation, which limits the power factor range [244, 245].

To achieve bidirectional power flow, the two-level voltage source, six-switch boost rectifier shown in Figure 3.6b can be employed. This converter is the most commonly used topology for grid interfacing because it features simple control, low THD, broad range of power factor control on the AC side, and DC-side voltage control [245]. It does, however, have some drawbacks, including a limited switching frequency, a large input inductor, high voltage stress on the semiconductor switches due to exposure to the full-scale DC-link voltage, and reduced reliability due to the possibility of a bridge leg shoot-through, resulting in DC bus short-circuiting [242]. Many control strategies have been proposed in literature, including sinusoidal Pulse-Width

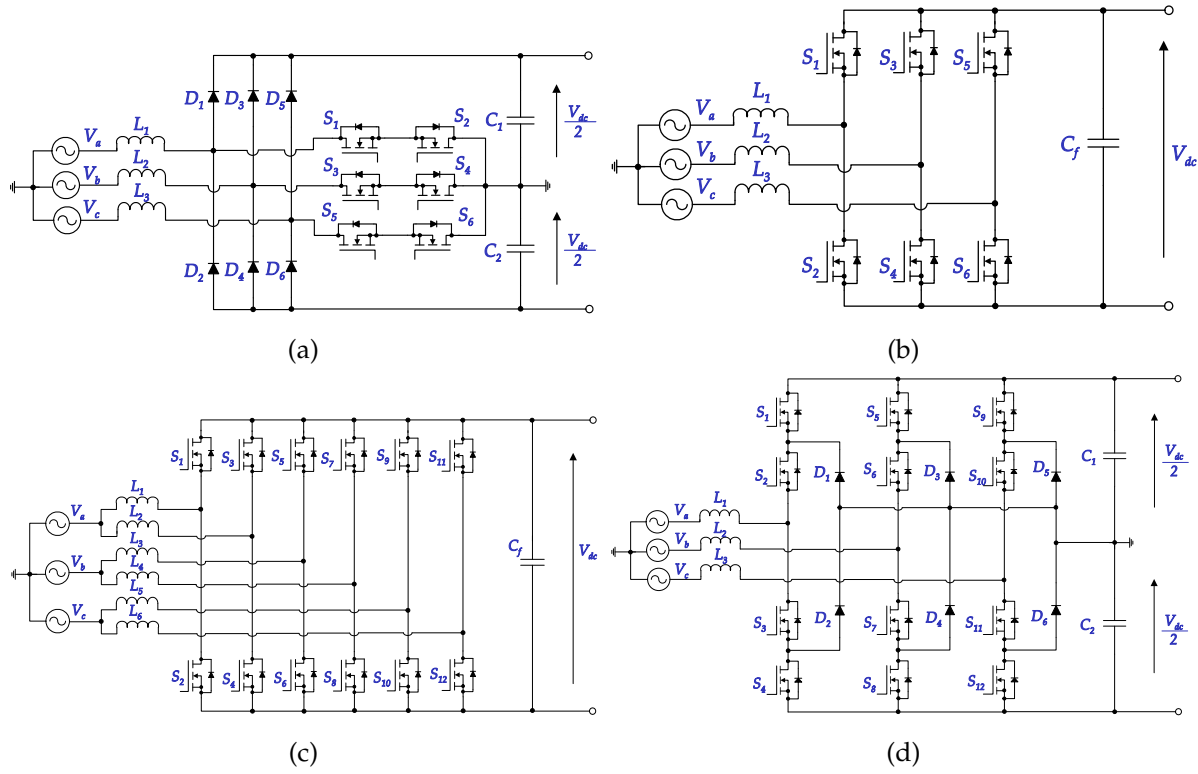


Figure 3.6: Front-end rectifier topologies-I (a) Vienna boost rectifier; (b) Voltage source 6-switch boost rectifier; (c) Bidirectional interleaved converter; (d) NPC converter.

Modulation (PWM), Space Vector Modulation (SVM), SMC, Hysteresis Current Control (HCC), and One Cycle Control (OCC), all with the goal of reducing input filter size and power switch stress [224]. As seen in the Figure, the maximum current through each semiconductor equals the maximum current in each phase of the AC grid. One method for reducing the maximum current through each power switch is to interleave the converters, as illustrated in Figure 3.6c, which shows a bidirectional interleaved converter constructed by connecting two of the converters from Figure 3.6b in parallel. This topology minimizes the maximum current going through each power switch by splitting phase currents into two pathways, but it requires additional hardware components [243]. Furthermore, interleaving both converters allows for harmonic elimination in the input current waveform and reduced DC side voltage oscillations [246]. Moreover, the interleaved converter's frequency doubling capabilities considerably reduces the size of the input boost inductance. Circulating currents between the two paralleled rectifiers are a big concern in this design because they create additional conduction routes when linked to the same DC bus and shared sources [247].

A Multilevel Converter (MLC) topology can be used to further reduce voltage stress on semiconductor voltage switches. Figure 3.6d shows a three-level NPC converter, which is the most used multilevel arrangement. This converter supports bidirectional power flow and produces a controlled DC voltage that is greater than the peak input voltage. It also facilitates the use of lower voltage semiconductor devices while working at lower switching frequencies [248]. Other features of this converter include its very low THD in input line current, low passive filtering requirements, and explicit creation of a bipolar DC-bus, which has been investigated

by [249] to implement a charging station, allowing DC-DC converters to connect to half of the DC-bus voltage [239]. The need for capacitor voltage balancing algorithms [250,251] is one of the most difficult challenges connected with using this converter. Unbalanced voltage drops across capacitors can result in poor output voltage quality, compromising control performance and even causing semiconductor devices to malfunction [252].

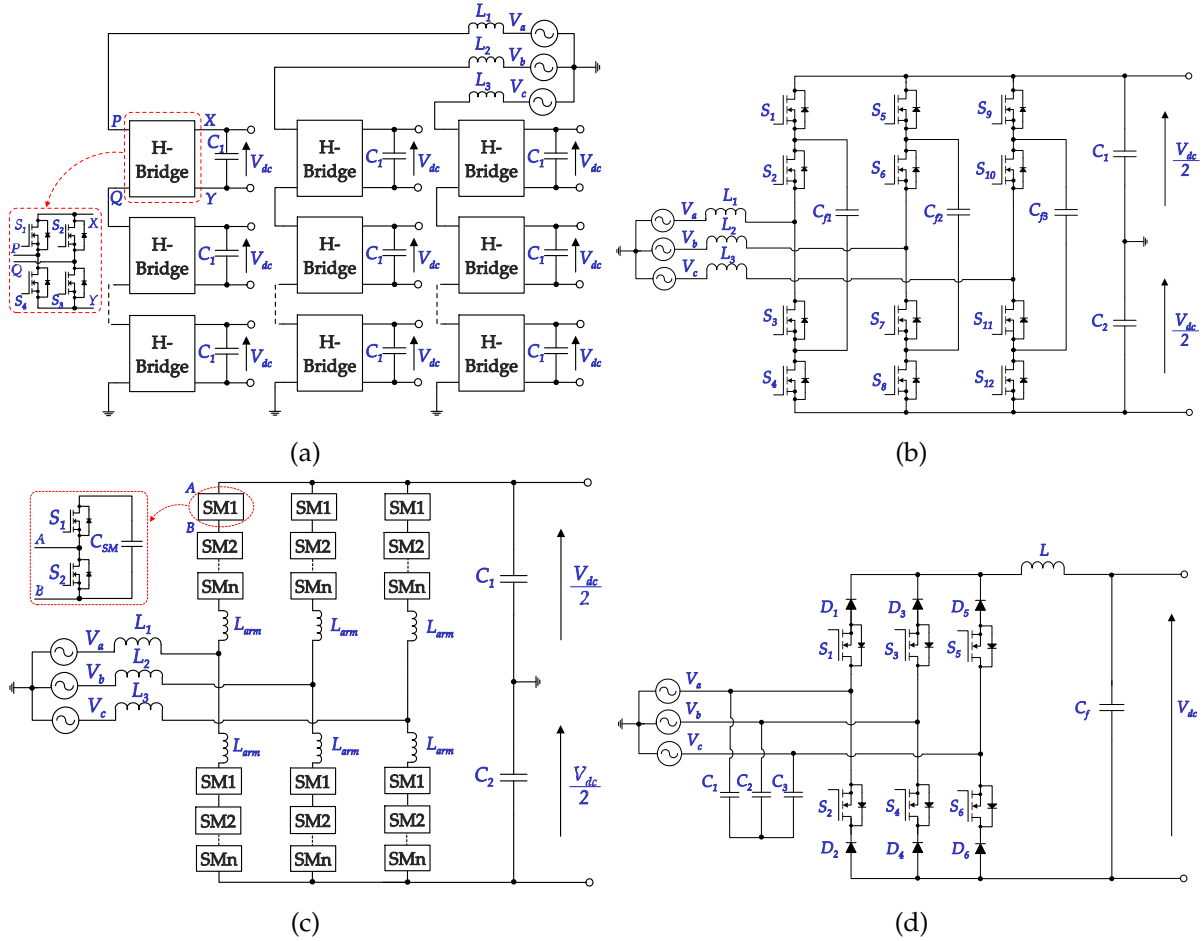


Figure 3.7: Front-end rectifier topologies-II (a) Three-phase cascaded H-bridge rectifier circuit (b) Three-phase 3-level flying capacitor MLC (c) Modular Multilevel converter (MMC) (d) Current source 6-switch buck type PFC rectifier.

Other prominent MLC topologies include the Cascaded H-Bridge (CHB) converter, the Flying Capacitor Converter (FCC), and the Modular Multilevel Converter (MMC) [222]. CHB converters (Figure 3.7a) are composed of numerous H-bridge cells that use phase-shifted PWM to generate high-quality, low-THD waveforms. They are scalable and have redundant operations. However, the CHB has several downsides, such as the necessity for complex control and modulation systems, particularly when multiple modules must be operated simultaneously. Furthermore, the requirement for many H-bridges might complicate system design and raise maintenance concerns. FCCs (Figure 3.7b), on the other hand, use various complex PWM and vector control approaches to pre-charge the flying capacitors before startup and give precise control of capacitor voltages, resulting in balanced operation across several levels. They have extremely low THD, low EMI, and great efficiency. They, however, necessitate a large number of components, which

raises system costs. MMCs (Figure 3.7c) use Nearest Level Control (NLC) or Selective Harmonic Elimination (SHE) for modulation for optimal output voltage and current control. They are well-known for their strong control capabilities, exceptionally low harmonic distortion, which reduces the need for significant filtering, and superior fault tolerance, scalability, and efficiency, making them perfect for large-scale EV charging stations [241]. However, controlling an MMC rectifier is extremely hard, necessitating advanced control algorithms to successfully manage the various submodules. They also require significantly more components than the CHB and FC topologies, resulting in greater initial costs. Furthermore, the requirement for numerous capacitors in submodules might cause problems with capacitor balancing and long-term reliability.

Figure 3.7d shows a six-switch current-source buck converter, another popular PFC rectifier used in charging stations. This converter can only provide unidirectional power flow when the polarity of the output DC voltage is fixed. However, if the polarity of the output DC voltage could be inverted or reversed, bidirectional power flow is possible [239]. Furthermore, unlike the Vienna rectifier, this converter lacks a central point, requiring no capacitor voltage balancing. Moreover, due to its buck nature, it can produce low semiconductor voltage stress while simultaneously offering short-circuit protection [242]. However, it has relatively significant conduction losses since there are more series-connected devices, pulsating input currents, requires EMI filtering, and provides limited power factor range control at the AC, which results in a lower output voltage control range [253].

Figure 3.8a shows a Swiss rectifier suggested by [254] and later by [255] as a potential contender for level 3 battery charging of electric vehicles and buses. It employs two buck converters to keep the output voltage lower than the peak input voltage, removing the requirement for AC filter inductors [256]. To generate a completely sinusoidal input current, it employs the third harmonic current injection concept. Other features of this converter include minimal current stress on the power transistors, which leads to excellent efficiency, low control complexity, and short circuit current limiting capabilities [242, 257]. It also contains more active power switches than the six-switch buck converter. Aside from that, the AC capacitor filters consume a substantial amount of reactive power. This converter can only generate unidirectional power flow; however, several researchers have worked on modifying it to achieve bidirectional power flow [258–261].

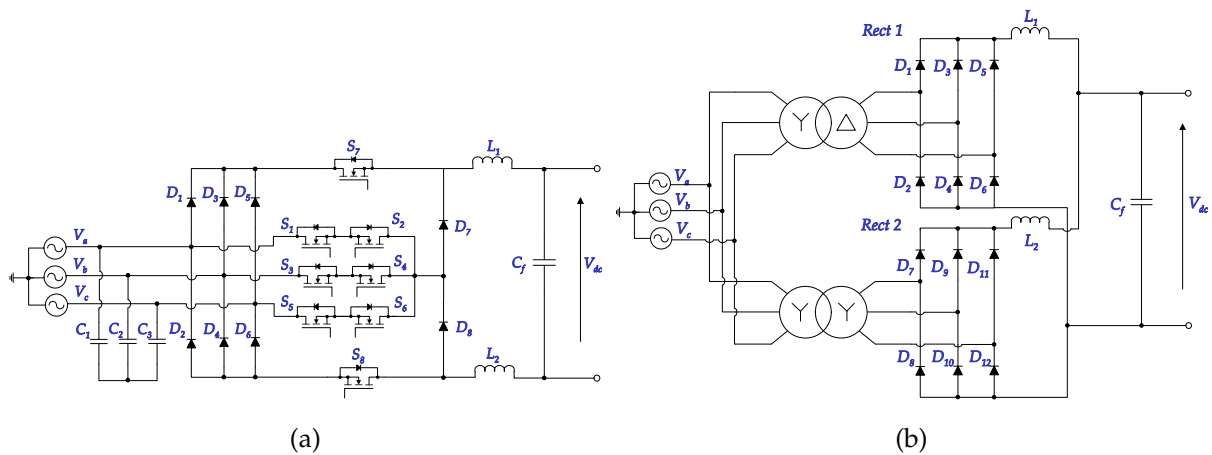


Figure 3.8: Front-end rectifier topologies-III (a) Swiss buck rectifier; (b) 12-pulse diode rectifier.

Figure 3.8b depicts a 12-pulse thyristor bridge rectifier, another grid-facing converter that may generate regulated DC voltage. The system uses a multi-winding transformer with Y-Y and Y- Δ connections and suitable turn ratios to create two three-phase voltage sources with the same amplitude and a 30-degree phase shift. By connecting two 6-pulse thyristor bridge rectifiers, the output can produce a total of 12 pulses per cycle [256]. This considerably decreases current harmonics, making the input current more sinusoidal. The disadvantage of this strategy is that it requires the use of a multi-winding transformer, which is large and heavy and provides only unidirectional power flow. Furthermore, because the classic 12-pulse rectifier does not fulfill the IEEE 519 standard for creating THD of less than 5%, extra passive or active filters at the input are required, which are often large and bulky and may impair the circuit's power factor [262]. Many studies have been reported in literature aiming to reduce the input current THD to less than 5% by altering the typical 12-pulse rectifier of Figure 3.8b [263–266]. The outputs of the two 6-pulse rectifiers could be connected in series or parallel, with the parallel connection favored for high-current applications due to lower thyristor forward voltage drop despite certain current sharing concerns [262]. This is the least used AC-DC converter for EV charging among the ones described thus far.

3.4.2 Back-end DC-DC Converters

The DC-DC converter's primary function is to control the output voltage of the front-end AC-DC converter to a level sufficient to charge the EV battery in the desired mode. It also serves as an interface for the connecting RESs and ESDs. DC-DC converters fall into two categories: isolated and non-isolated. The isolated DC-DC converters shown in Figures 3.9 and 3.10 have a High-Frequency Transformer (HFT) and must offer galvanic isolation between the grid and the battery or ESS. To offer protection, the non-isolated DC-DC converters depicted in Figures 3.11 and 3.12 must be interfaced with a large LFT on the grid side.

3.4.2.1 Isolated DC-DC Converters

The Phase-Shift Full Bridge (PSFB) converter, shown in Figure 3.9a, is the most commonly utilized topology for high power and high frequency applications. This converter has a simple control system, minimal current stress on the power switches due to Zero Voltage Switching (ZVS) that uses the transformer's leakage inductance in addition to the parasitic capacitance of the power switches, and a wide range of output voltages [267]. However, the converter has some drawbacks, including unidirectional operation, duty cycle losses in active switches, difficult to achieve ZVS at light loads (limited ZVS range), high conduction losses in output diodes, circulating current losses, and high voltage ringing on the secondary side rectifier diodes [268], which can be reduced using passive or active snubber circuits, but this reduces system efficiency [239].

To achieve bidirectional conduction capabilities, the Dual Active Bridge (DAB) schematic shown in Figure 3.9b could be employed, which involves replacing the diodes in the prior circuitry with MOSFETs. Similar to the preceding structure, this converter features a wide output voltage range and soft-switching capability. This architecture reduces voltage stress on the switches, gives higher power densities, and is more efficient than the converter in Figure 3.9a [242]. Despite the benefits, it has certain drawbacks, such as the presence of reactive current,

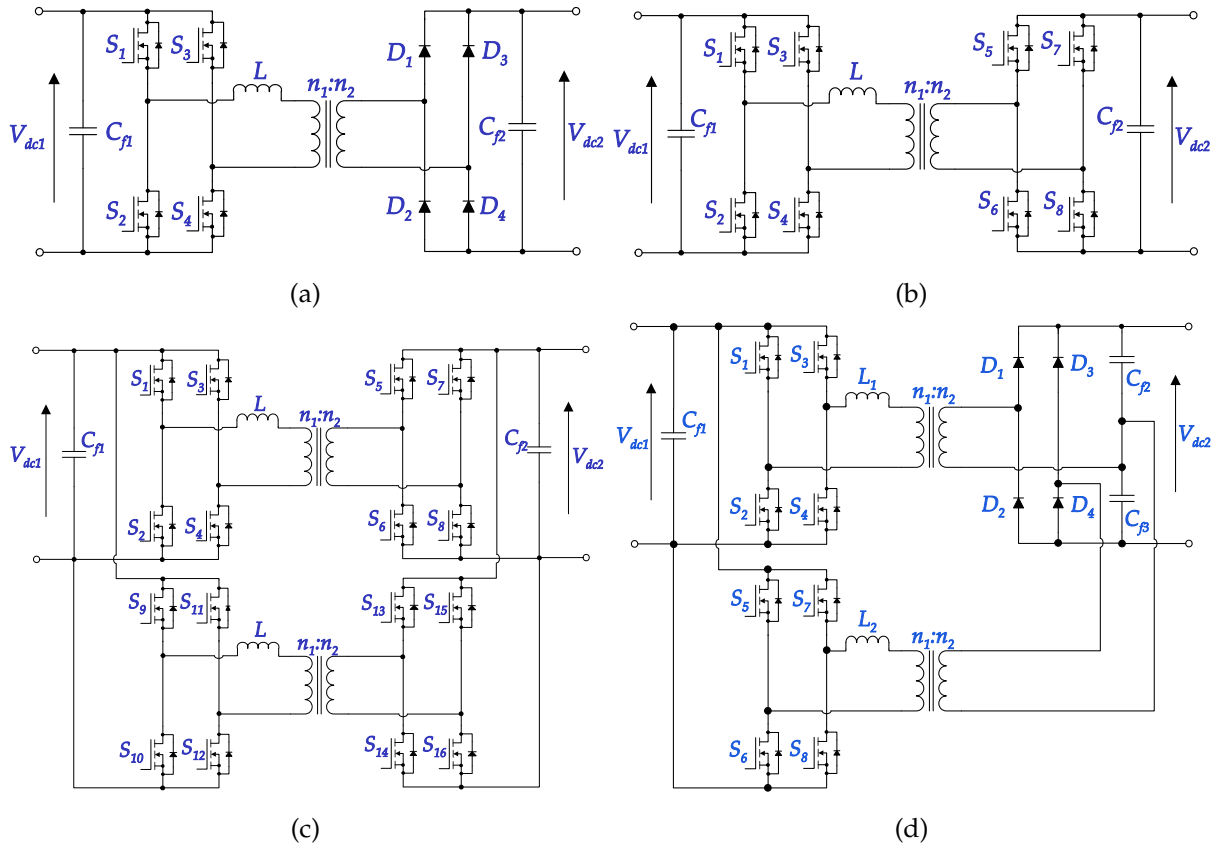


Figure 3.9: Isolated DC-DC converters-I (a) phase shift full-bridge ZVS converter (b) dual active bridge (c) cascaded dual active bridge (d) interleaved full-bridge with voltage doubler.

significant input and output ripple owing to switching, necessitating the use of large input and output filters [269], and hard switching at low loads [270]. Interleaving the DAB, as illustrated in Figure 3.9c, could improve its performance. This reduces each DAB's operating power [243], reduces voltage and current ripple in the input and output capacitors, and reduces input and output filtering needs, all at the expense of extra hardware and more control complexity.

Figure 3.9d shows an isolated interleaved DC-DC converter with a voltage doubler, another unidirectional converter proposed by the authors of [271] for battery charging. This converter has no reverse recovery losses in the secondary rectifier diodes and no high voltage ringing when operating in Discontinuous Conduction Mode (DCM) and Boundary Conduction Mode (BCM), which is typically caused by resonance between the diode parasitic capacitance and the transformer leakage inductance. The interleaving of converters decreases ripple current and voltage stress on the output filter capacitors [272]. Interleaving also offers the advantage of uniformly spreading heat losses between cells while sharing equal power. Furthermore, the input ripple is four times the switching frequency [273], the output voltage doubler rectifier reduces the number of secondary diodes significantly, and the diode voltage rating equals the maximum output voltage. This converter has the disadvantage of producing the lowest RMS currents when operating in Continuous Conduction Mode (CCM). Furthermore, while ZVS is possible for all switches, high di/dt causes significant reverse recovery losses in secondary side rectifier diodes as well as high voltage ringing. Furthermore, CCM functioning involves the use

of a large resonant inductor, which increases the transformer turns ratio, putting additional stress on the primary side switches [274].

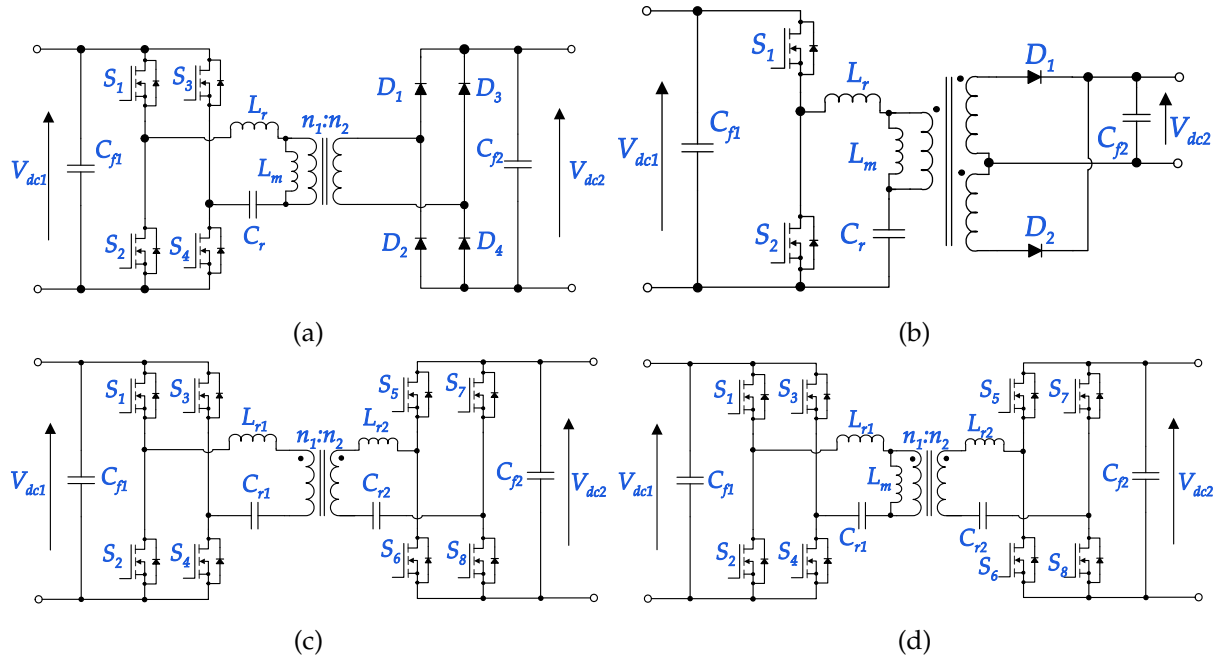


Figure 3.10: Isolated DC-DC converters-II (a) full-bridge isolated LLC resonant converter (b) half-bridge LLC resonant converter (c) full-bridge CLLC resonant converter (d) full-bridge CLLLC resonant converter.

Another popular type of DC-DC converter for fast charging is the LLC resonant converter, which is classified into two types: full-bridge LLC converters (Figure 3.10a) and half-bridge LLC converters (Figure 3.10b). On the secondary side, full-wave rectification might be accomplished with either a complete bridge rectifier (Figure 3.10a) or a center-tapped transformer (Figure 3.10b). In general, the choice between full-bridge and half-bridge on the primary side is determined by the power level, with full-bridge architecture being preferred for high power applications and half-bridge configuration being preferred otherwise, whereas the choice between center tap and full-bridge on the secondary side is determined by the current and voltage levels, with center tap being preferred for low voltage and high current applications and full-bridge being used otherwise [275]. In these converters, all semiconductors are soft-switching, which means that ZVS occurs at turn-on for primary MOSFETs and Zero Current Switching (ZCS) occurs at both turn-on and turn-off for secondary diode rectifiers [276]. These topologies outperform previous resonant converters in terms of efficiency at high input voltage, primary switches that can function at ZVS over a wide range of loads, no reverse recovery losses on secondary diodes, and minimal voltage stress on rectifying diodes. The fundamental issue with these converters is that they need a wide range of switching frequencies to adjust the output voltage [277, 278]. The wide range of switching frequencies complicates the design of circuit filters, transformer magnetics, and gate driver circuits, resulting in poor EMI performance, and causes loss of soft switching at certain frequencies of operation, resulting in low power conversion efficiency [279–282]. The converters presented only provide unidirectional power flow and so cannot be used in V2G applications. However, replacing the diodes with MOSFETs in a synchronous rectification process allows for

bidirectional power flow.

Although the LLC resonant converter can be designed to produce bidirectional power flow, this presents various challenges. During reverse power flow situations, the output voltage clamps the transformer's magnetizing inductance, preventing it from undergoing resonance. In this scenario, the LLC resonance circuit performs similarly to an LC series resonance circuit, with a maximum voltage gain of 1. As a result, ZCS is inhibited on the rectifier side, significantly reducing converter efficiency [283,284]. To address this issue, the full-bridge CLLC symmetric resonant circuit illustrated in Figure 3.10c is widely employed in bidirectional power flow applications. During reverse power flows, this converter can accomplish both ZVS on the primary side and ZCS on the rectifier side, lowering switching energy losses and enhancing overall circuit efficiency. Furthermore, the range of bidirectional DC gains is increased, allowing for better voltage regulation flexibility [285]. The performance of the CLLC resonant circuit can be increased by either interleaving the converter, as done in [286], which increases the design volume and cost, or by adding the transformer's magnetizing inductance to make a CLLLC resonant circuit [287–289], as illustrated in Figure 3.10d. However, this increases the converter's design complexity.

3.4.2.2 Non-isolated DC-DC Converters

For battery charging, a standard single-phase buck converter could be used to step down the DC-link voltage to a battery-acceptable value. However, in this design, either a large inductor is used to reduce the inductor current ripple to small values, increasing the cost and size of the converter, or the switching frequency is increased to improve the converter's dynamic performance, increasing switching losses [267,290]. One option is to interleave two or more converters to create a multi-phase interleaved buck converter [291–294]. Figure 3.11a displays a two-phase interleaved buck converter. Interleaving the converter causes current splitting, which leads to current ripple cancellation, improved thermal performance, reduced conduction losses, increased efficiency, and increased power density [272]. Furthermore, as the fundamental frequency of each inductor is multiplied by the number of phases, the size and rating of the inductor and filters reduce. The drive signals of the active switches in this converter must be phase-shifted by $360^\circ/N$, where N is the number of phases [295]. Boost and buck-boost converters can have similar interleaving designs.

Figure 3.11b shows a three-level NPC bidirectional converter operating in buck mode for Grid-to-Vehicle (G2V) and boost mode for V2G. It is used in high input voltage, high power, and high switching frequency applications because the switch stress is only half of the DC bus voltage, permitting switches of lower voltage rating to be used in comparison to two-level converters, which are rated for the full-scale DC-link voltage [296–298]. Consequently, the converter's switching frequency is doubled [299]. Furthermore, the filter inductance can be greatly lowered, resulting in a rapid dynamic response [300]. Moreover, this converter is compatible with any charging station with a bipolar DC-bus [301], and the authors of [302] took advantage of this feature. However, this converter has some disadvantages, including the inability to interleave due to the formation of circulating currents [303], the voltage conversion ratio being the same as that of a two-level buck/boost converter, and the input and output terminals not being commonly

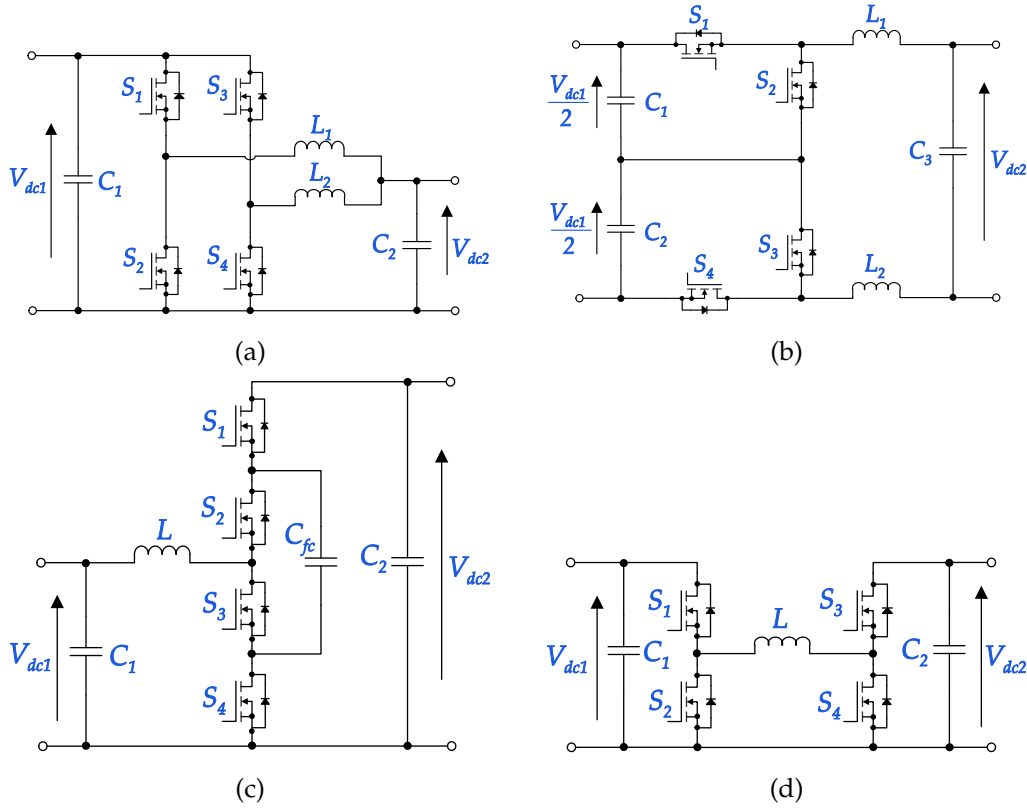


Figure 3.11: Non-isolated DC-DC converters-I (a) Interleaved buck converter (b) Three level NPC boost converter; (c) Three level flying capacitor boost converter (d) Cascaded buck-boost converter.

grounded, which increases Electro Magnetic Interference (EMI) [299].

To address the voltage gain and lack of common ground issues with the previous converter, [300] suggested the three-level flying capacitor bidirectional converter shown in Figure 3.11c. This converter has a high voltage conversion ratio with higher efficiency, low inductor core and copper losses, low input current ripple, which results in a smaller input filter, and low voltage stress on power switches [304]. The downside of this converter is that the voltage of each stage's flying capacitors must be balanced to their nominal value, which complicates circuit control [305]. If the flying capacitor voltage remains imbalanced, voltage stress on the switches grows, potentially leading to power loss [306]. In literature is mentioned several capacitor voltage balancing approaches, the most notable of which are active and passive voltage balancing (RLC filter) [307–309].

Figure 3.11d shows a cascaded buck-boost converter, another non-isolated bidirectional DC-DC converter introduced by [310], which is widely utilized in charging stations and ESSs. This converter supports four-quadrant operation and can work in both buck and boost modes [311,312]. The switches have less electrical and thermal stresses than conventional buck-boost converters, and they can achieve ZVS without the requirement of an additional or auxiliary soft switching circuit by using proper modulation schemes [313]. It does, however, have complex control techniques and has some turn-on losses due to the reverse recovery problem of transistor body diodes when the typical PWM strategy is utilized while running in CCM, lowering efficiency [314].

When running at light loads, hard switching further lowers efficiency [315].

The split-pi bidirectional converter architecture seen in Figure 3.12a is a relatively novel topology among DC-DC converters, having been patented by Timothy Richard Crocker in 2002 [316]. This converter is widely utilized in electric mobility, battery management, energy storage, and the integration of RESs. It consists of two interconnected DC-DC converters that share a common DC-link and have two independent DC interfaces utilized to generate an output voltage that can be greater, equal, or lower than the input voltage, resulting in a four-quadrant converter [317]. This converter offers a wide range of operating modes and uses small passive components. Furthermore, only one bridge switch is activated at a time, which reduces voltage stress on the switches [318]. Moreover, its topological arrangement helps reduce switching losses, distortions, and ripples on output current, resulting in efficiencies over 97% [319, 320]. One issue with this converter is that during operation, one of the stages' voltage gain is set to unity, causing the other converter stage to function as a second-order filter in the forward path, potentially producing phase delays and complicating the system's feedback control [321]. Paralleling this converter, as illustrated in Figure 3.12b, considerably lowers the ripples in the input and output currents [322].

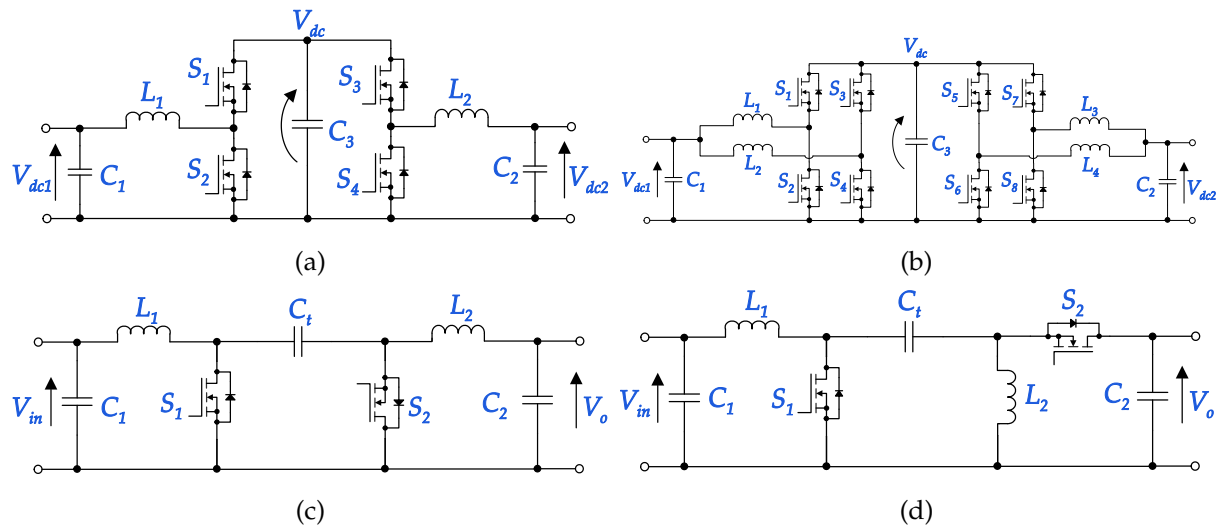


Figure 3.12: Non-isolated DC-DC converters-II (a) split-pi converter (b) interleaved split-pi converter; (c) Cuk converter (d) combined SEPIC/zeta converter.

Another popular converter is the bidirectional Cuk converter (Figure 3.12c), built from the typical unidirectional Cuk converter by replacing the primary diode with a MOSFET. This converter is effectively a boost converter followed by a buck converter; therefore it can step up or down the input voltage like a regular buck-boost converter [323]. Unlike other topologies that use inductors to store energy, the transfer capacitor (C_t) is the energy storage component. This converter is a superior alternative for connecting ESSs and charging EV batteries than cascaded buck-boost or regular buck-boost converters because it produces less current ripples at the input and output [324]. Moreover, Inductors L_1 and L_2 can be coupled to further decrease input and output current ripples [312]. This converter has some disadvantages, including reverse voltage polarity at the output, the necessity for large-sized inductors, and a high voltage stress ($V_{in} + V_o$) on the transfer capacitor [323, 325].

To address the shortcomings of the bidirectional Cuk converter, the SEPIC/zeta converter (Figure 3.12d), which is essentially a rearrangement of the Cuk converter, can be utilized. It can function as a buck or boost converter in both directions, producing an output voltage of the same polarity as the input [119]. For positive power flows, the converter acts as a SEPIC converter; for negative power flows, it acts as a zeta converter [312]. In this case, the voltage stress on the transfer capacitor is V_{in} . This converter accepts a broader range of input voltages than the Cuk converter and has smaller current and voltage ripples, which can be further decreased if the inductors are coupled [326]. With the addition of auxiliary circuits, this converter may achieve soft-switching [327]. The Zeta/SEPIC converter is the inverse of the SEPIC/zeta converter and has been employed in battery charging and energy storage systems [328,329].

Various control methods are stated in literature to control the converter power, and hence currents and voltages, that are utilized to successfully manage the battery charging of these EVs. Model Predictive Control (MPC) is utilized in [330] for current control, fault detection, and SoC balancing of all divided battery storage at the same time. Aside from MPC control, the standard PI control approach is commonly utilized, as seen in [331] and [332]. In [331], the authors implement a three-phase off-board charger and use PI controllers to perform decoupled dq grid current control, DC-link voltage control, independent battery current control with PI, and the integration of duty ratio feedforward control to achieve rapid dynamic control. [333] and [334] have also used advanced control techniques like SMC. The authors of [333] use SMC in aircraft battery charging to overcome the stability issues encountered by traditional PI controllers when used for multi-objective controls, whereas the authors of [334] use SMC in LLC converters to improve dynamic response and robustness at the expense of increased design and parameter tuning complexity. In [335], second-order LADRC is utilized for LLC resonant converters to improve dynamic performance and reduce the effect of internal and external disturbances on output battery voltage.

3.5 DC-DC Converters Based on Partial Processing of Power

So far, all of the DC-DC converters detailed in the previous section are designed to process the entire power input from the source, as illustrated in Figure 3.13a. They are known as Full Power Processing (FPP) converters. If only a portion of the source power can pass through these converters, as shown in Figure 3.13b, while the rest is sent directly to the load, conduction, switching, and magnetic losses will be reduced, and the converter's overall efficiency will be increased [336,337]. This is the underlying notion of power converters based on partial power processing, also known as Reduced Dissipation Converters (RDCs). Aside from increasing system efficiency, this architecture offers other advantages, such as reducing converter ratings due to lower voltage stress, allowing small-sized converters to be employed, and lowering overall system costs [338]. This concept is relatively new and has been implemented in a number of applications, including distributed PV systems [339], EV fast-charging stations [340–342], fuel cell-powered hybrid EVs [343], and current control in battery energy storage systems [344]. The disadvantage of this form of architecture is that the galvanic isolation between the source and load is bridged because power must go directly from the source to the load and is thus actively being explored.

PPP converter architectures are classified into two types: those that require isolated DC-DC converters (Figure 3.14) and those that do not (Figure 3.15) [345–348].

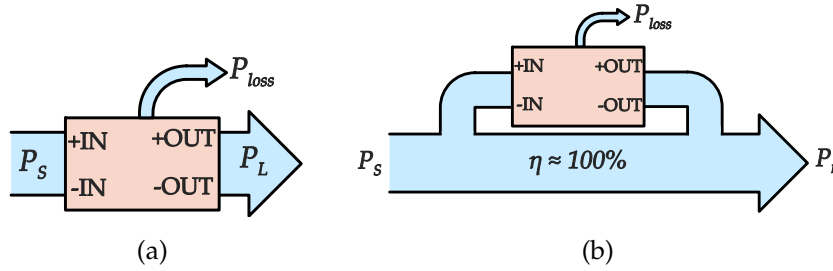


Figure 3.13: Power flow diagram (a) FPP (b) PPP.

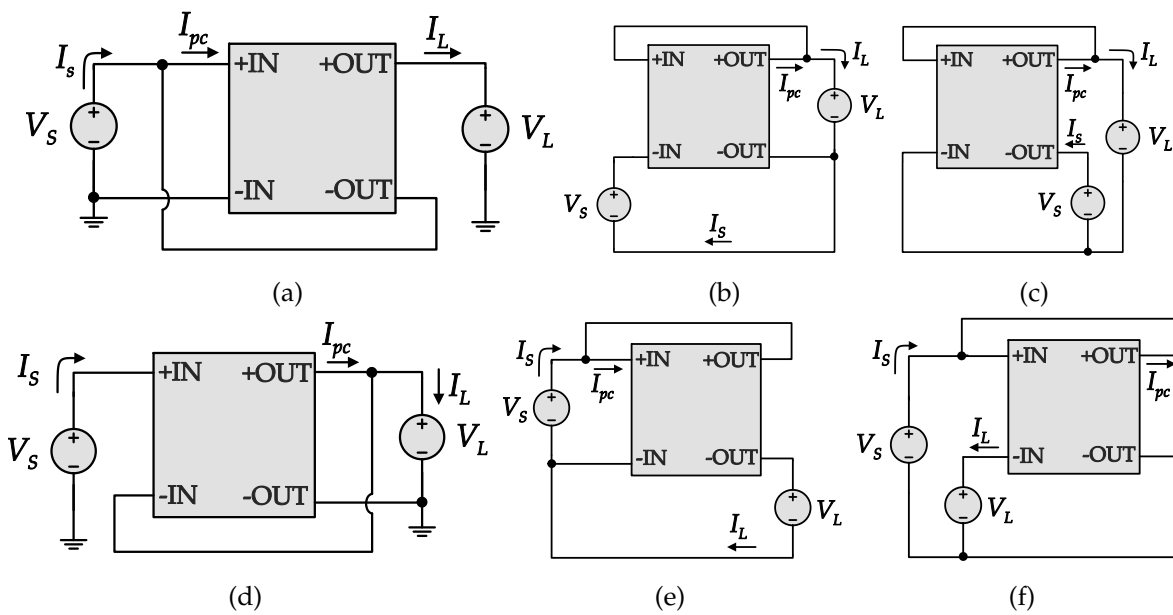


Figure 3.14: PPC topologies requiring isolated DC-DC converters (a) IPOS step-up (b) ISOP-I step-up (c) ISOP-II step-up (d) ISOP step-down (e) IPOS-I step-down (f) IPOS-II step-down.

The metric defining the amount of power processed by these converters is known as the active power ratio (K_{pr}), which is defined as:

$$K_{pr} = \frac{P_{pc}}{P_s} \quad (3.1)$$

where P_{pc} is the power processed by the converter and P_s is the source power. The converter operates in PPC mode when the partial power ratio, K_{pr} , is less than 1. For example, we may calculate the K_{pr} of the architecture in Figure 10a. The first step is to apply Kirchhoff's voltage and current rules to the architecture as described in equations (3.2) and (3.3), followed by computing the system efficiency as in (3.4):

$$V_L = V_s + V_{out} \quad (3.2)$$

$$I_s = I_{pc} + I_L \quad (3.3)$$

$$\eta_{sys} = \frac{V_L I_L}{V_s I_s} \quad (3.4)$$

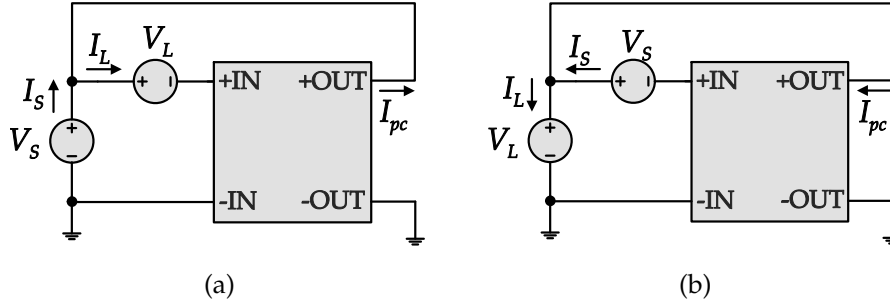


Figure 3.15: PPC topologies that do not require isolated DC-DC converters (a) step-up (b) step-down.

From (3.1), we get

$$K_{pr} = \frac{P_{pc}}{P_s} = \frac{V_{out} I_L}{V_s I_s} \quad (3.5)$$

By inserting equations (3.2), (3.3) and (3.4) into (3.5), we can get K_{pr} as a function of the converter static voltage gain ($G_V = V_L / V_S$) as given in (3.6).

$$K_{pr} = \eta_{sys} \left(1 - \frac{1}{G_V} \right) \quad (3.6)$$

By using a similar technique, the K_{pr} of other architectures in Figure 3.14 can be derived and are shown in Table 3.3.

Table 3.3: K_{pr} for different PPC configurations of Figure 10.

PPC configuration	K_{pr}
IPOS step up	$\eta_{sys} \left(1 - \frac{1}{G_V} \right)$
ISOP-I step up	$\eta_{sys} - G_V$
ISOP-II step up	$G_V - \eta_{sys}$
ISOP step down	$\eta_{sys} - G_V$
IPOS-I step down	$\eta_{sys} \left(1 - \frac{1}{G_V} \right)$
IPOS-II step down	$\eta_{sys} \left(\frac{1}{G_V} - 1 \right)$

[349] implemented the PPP converter depicted in Figure 3.16b, which is based on a DAB, for fast charging of EVs. This converter is configured as shown in Figure 3.14d. Figure 3.17 depicts some of the obtained results. Figure 3.17a illustrates that the DAB-FPP processes 100% of the source power at all times during the charging process, whereas the DAB-PPP initially processes around 40% of the input power, which declines as the battery state of charge grows. As a result, Figure 3.17b shows that the DAB-PPP has superior system efficiency for SoCs more than 5%.

The application of PPP converter technology to EV charging stations is very promising, and future charging stations are projected to adopt this approach. However, adequate isolation mechanisms must be studied before this technology can be commercialized.

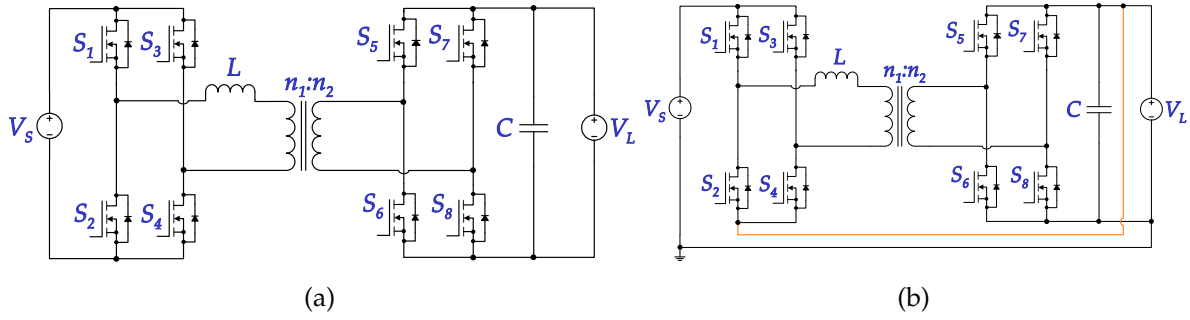
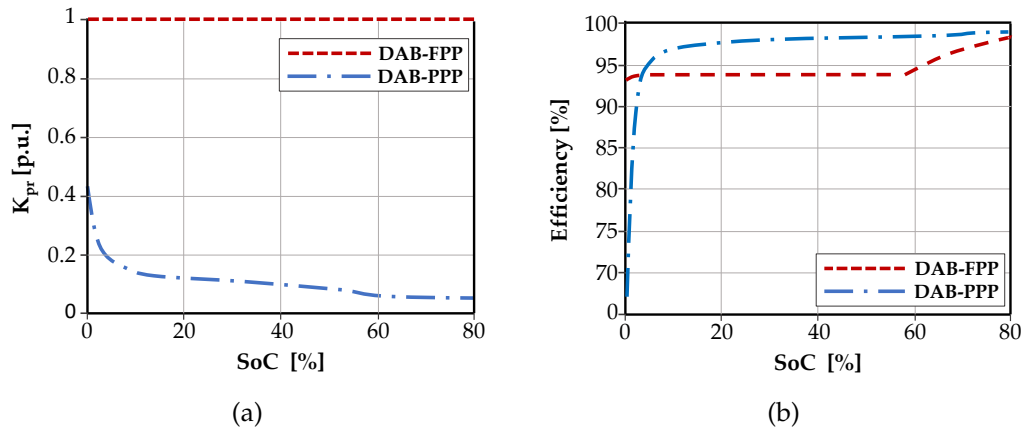


Figure 3.16: DC-DC converter based on DAB for fast charging station (a) FPP-DAB (b) PPP-DAB.

Figure 3.17: Comparison of DAB-FPP with DAB-PPP (a) processed power ratio (K_{pr}) vs SoC (b) efficiency vs SoC.

3.6 Multiport Converters for EV Charging Stations

Traditionally, Single Input Single Output (SISO) port power converters are used to handle the power flow for each energy source separately, which results in higher costs, more space requirements, and a greater number of components. Furthermore, the system becomes more complex as several converters are controlled independently. To overcome these issues, multiport converters have been proposed as an effective alternative. Integrating different energy sources and loads into a single converter reduces system complexity, resulting in cost savings and reduced space needs. One of the primary benefits of employing a multiport converter is its flexibility to handle a variety of energy sources, including grid-connected systems, EVs, ESSs, and RESs while permitting bidirectional power flow between each port. This adaptability allows for effective power flow management and the seamless integration of multiple energy sources into a single system. Furthermore, multiport converters help to increase the power density of the entire system. By merging the power conversion tasks of several converters into a single unit, the system's overall efficiency improves [350]. Moreover, by adopting a centralized control system, cumbersome communication between individual conversion steps in the SISO converters can be avoided. This streamlines the overall control structure and improves system reliability. The general structure of a two-stage multiport grid-connected structure is shown in Figure 3.18a.

It consists of a multiport DC-DC converter which takes inputs from RESs, ESS and EV and outputs a DC voltage fed to the DC-AC inverter for interfacing with the grid while a single-stage

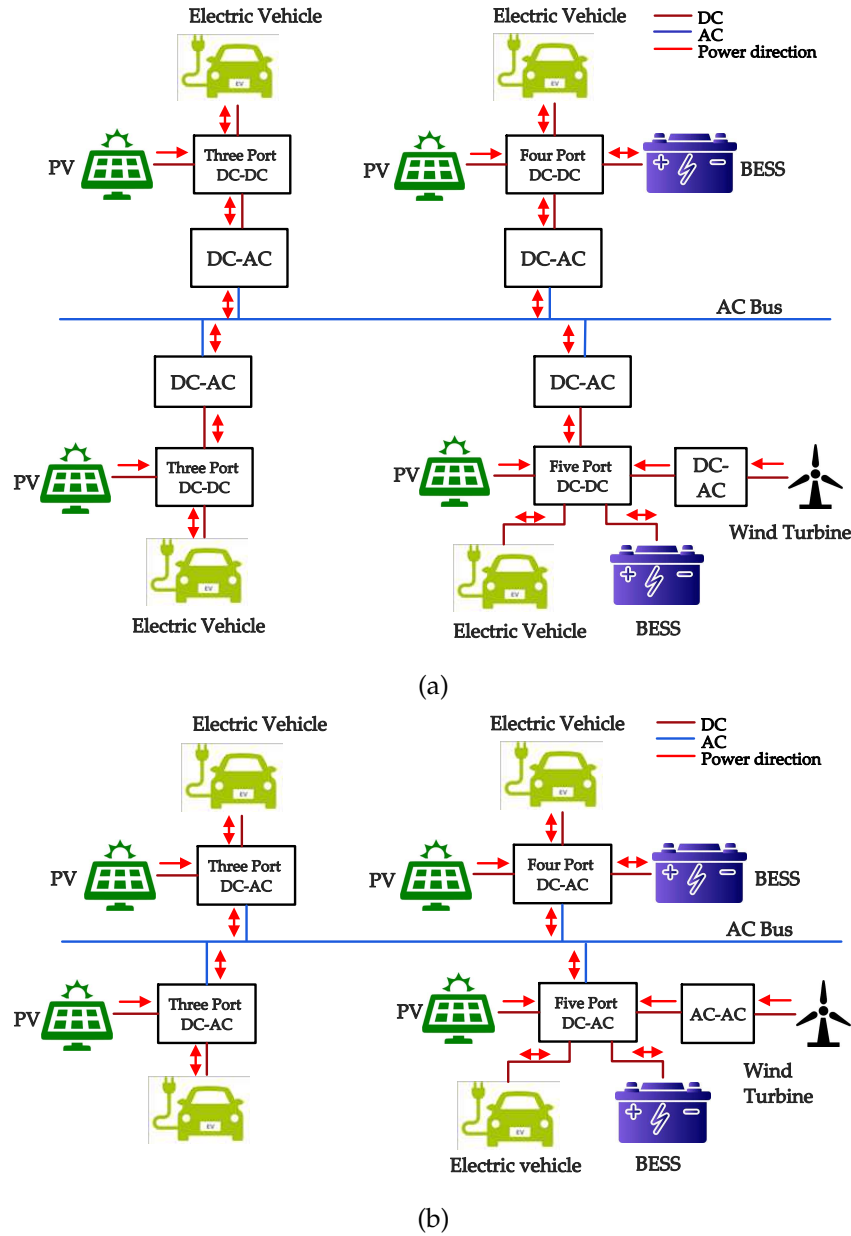


Figure 3.18: Multiport converter systems (a) two-stage multiport grid-connected system (b) single-stage multiport grid-connected system.

multiport DC-AC grid connected converter system is shown in Figure 3.18b which eliminates all the extra DC-AC inverters found in the two-stage structure. A comprehensive review focused on the state-of-the-art single-stage multiport inverters for multisource applications is provided by [351].

There are several topologies for multiport converters described in literature. Figure 3.19 shows a broad classification of multiport converters based on various selection criteria like structure, isolation properties, power flow direction, gain factor, and number of input/output ports (DISO, DIDO, MISO, MIMO, SIDO, SIMO) [352]. In general, the majority of known and reported multiport converters can be classified into three categories based on isolation characteristics: non-isolated multiport converters, fully isolated multiport converters, and partially isolated

converters.

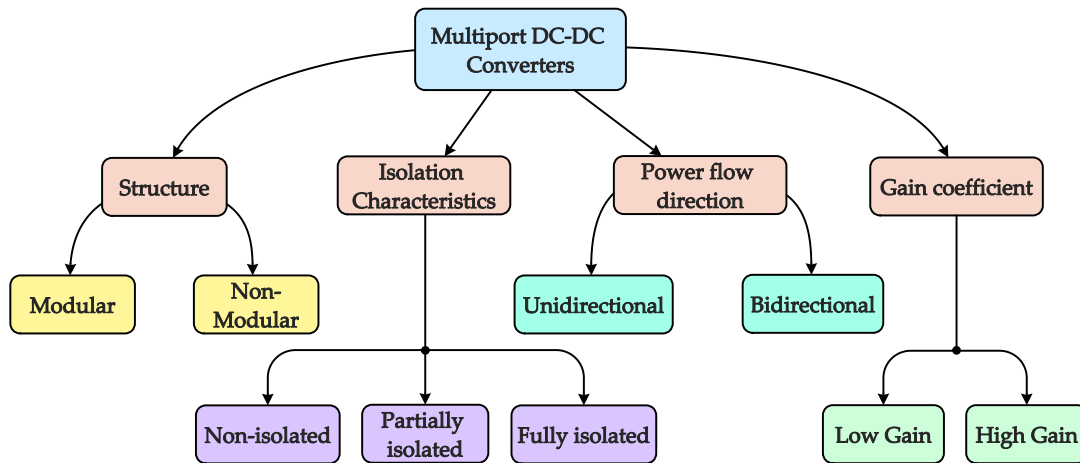


Figure 3.19: Classification of multiport converters.

Non-isolated multiport converters are those that lack electrical isolation between the input and output ports. In a non-isolated multiport converter design, as illustrated in Figure 3.20a, the input power ports are linked to a common electrical ground. They are typically derived from conventional two port converter topologies like boost, buck, buck-boost, sepic, cuk converters etc. They provide various advantages, including high power density, fewer switches, a relatively simple control method, and a compact design. Furthermore, these non-isolated multiport converters help to reduce costs while maintaining low levels of electromagnetic interference (EMI). However, soft switching cannot be easily performed, and voltage gain is rather small, even though it can be enhanced by employing coupled inductors, increasing the complexity of the converter [353]. A comprehensive review of some of the non-isolated topologies in literature has been presented by the authors of [354].

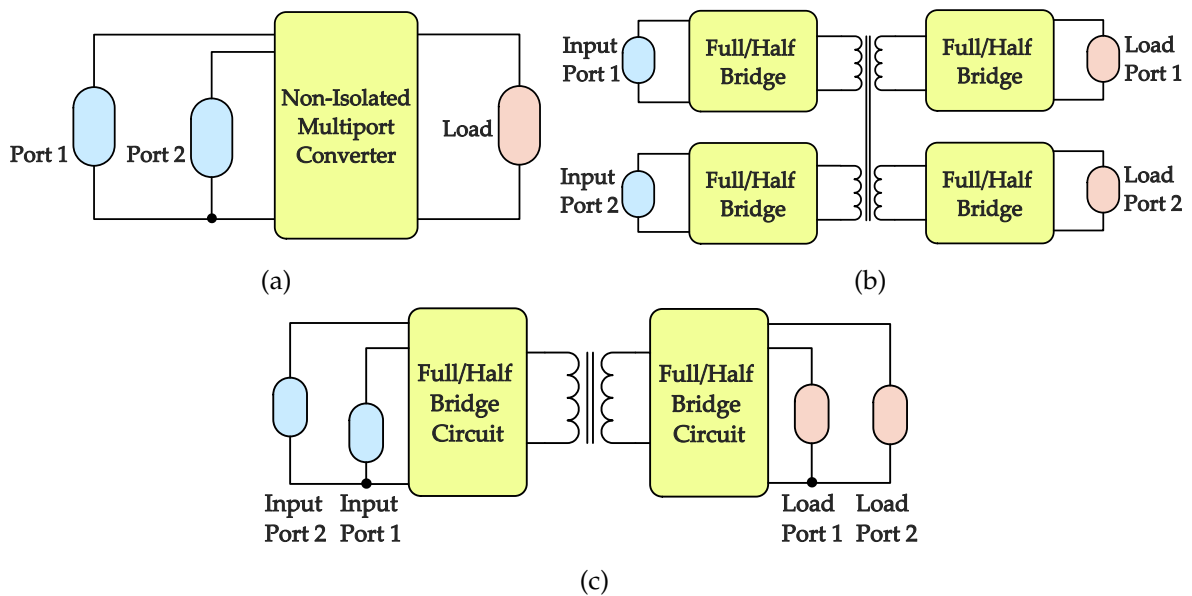


Figure 3.20: (a) Non-Isolated Multiport Converter (b) Isolated Multiport Converter (DIDO) (c) Partially Isolated Multiport Converter (DIDO).

Isolated multiport converters, shown in Figure 3.20b, typically integrate galvanic isolation between the input and output ports using multi-winding HFT. Thus, the major characteristic of isolated multiport converters is the use of separate windings for each power input and load output port. Isolated multiport converters provide multiple benefits, including a lower risk of electric shock, a wide range of voltage gain, noise filtering capabilities, the ability to maintain appropriate soft-switching conditions, and the capacity to combine varied voltage ratings. However, designing an HFT for high-voltage applications is difficult, expensive, and makes the converter bulky.

The partially isolated multiport converters depicted in Figure 3.20c are a unique category within the multiport converter world. This converter's topology is a combination of fully isolated and non-isolated multiport topologies. Partially isolated topologies use a single winding HFT for providing necessary isolation between the source side and the load side. To connect the HFT's single winding, it is required to connect all the input power ports to the input ports' common ground point. Partially isolated multiport converters provide several significant benefits, including high power density, configurable voltage ranges, and galvanic isolation of the load from the primary side. One of the key disadvantages of the partially isolated architecture is that it has a lower voltage scaling capability than a completely isolated multiport system [355]. State of the art review of the various partially isolated, fully isolated and non-isolated multiport converter topologies can be found in references [356–359].

3.7 Conclusion

This chapter has thoroughly explored power converters essential for EV charging stations, delving into the core components and configurations that facilitate an efficient and reliable battery charging process. We started by classifying battery charging based on power levels, differentiating between slow, semi-fast, fast, and ultra-fast charging modes, and discussing how these categories influence the design and deployment of charging infrastructure. Furthermore, the chapter examined various charging strategies and methods, highlighting their significance in optimizing energy transfer, reducing energy losses, and prolonging battery life.

Next, we discussed the architectures for fast EV charging, reviewing the benefits and challenges associated with DC bus, AC bus, and hybrid configurations, each offering distinct advantages tailored to specific applications and system demands. We also explored converter topologies crucial for EV charging systems, including both front-end AC-DC and back-end isolated and non-isolated DC-DC converters topologies. This section highlighted the importance of converter design in achieving high efficiency, power density, and durability.

Control techniques were also briefly mentioned, given their essential role in managing converter operations, ensuring stability, and optimizing performance under varying load conditions. The chapter's discussion on PPP DC-DC converters illustrated their potential to enhance efficiency and reduce component stress, especially within both isolated and non-isolated structures. Finally, we considered multiport converters, which provide versatile solutions for integrating RESs and ESSs into EV charging stations, thereby increasing the flexibility and sustainability of the charging infrastructure.

In conclusion, this chapter has offered a detailed exploration of the critical components that

make up power converters for EV charging stations. With the growing demand for EVs, the continued advancement of converter topologies, the development of efficient control strategies, and the creation of innovative charging architectures will be crucial in promoting the widespread adoption of EVs and advancing the shift towards a more sustainable transportation future.

Non-Modular DAB Dynamic Modeling and Robust Control Strategies

The DAB converter sets itself apart in the competitive field of bidirectional DC-DC converters for EV battery charging by having high power density, allowing for considerable power levels in a small size [360], and soft switching ability which reduces energy loss during operation and contributes to its remarkable efficiency. The DAB also includes galvanic isolation, a built-in safety feature that electrically separates the input and output sides, increasing both safety and versatility. Finally, the DAB converter has excellent voltage adaptability, supporting a wide range of input and output voltage levels. Figure 4.1 shows the DAB converter circuit, consisting of two full-bridge converters, an isolating HFT, and an energy storage inductor, which could be an external inductor or the transformer's lumped leakage inductor [361].



Modelling the DAB converter cannot be performed using the typical linear state-space averaging because the transformer current is sinusoidal and has an average value of zero. Consequently, approaches like reduced order average models [362], which neglect the dynamics of transformer and inductor current, multi-frequency averaging such as generalized average modelling (GAM) [363, 364], discrete full order models [365], and phasor models [366] are commonly used to design the converter control system. [367] proposes a detailed reduced

order average model in which the DC-side currents of the bridges are averaged to approximate transformer current. However, the model involves rederivation of the equations for different modulation strategies, which increases the complexity of the derivation process while a unique average model for any modulation approach is provided in [368]. However, the accuracy of the frequency response in [367] and [368] is restricted to one-tenth of the switching frequency. Full-order models provide higher frequency response accuracy in high-frequency zones and a lower frequency gain in magnitude response. Accordingly, [369] and [370] use GAM to build a continuous-time full-order model with a first-order harmonic approximation of the transformer current. However, when higher order harmonics are ignored, the large-signal model suffers from errors. The real and imaginary components of the Fourier coefficient provide two model states for each harmonic of the transformer current. Thus, higher order harmonics can be added to the model to improve its accuracy at the expense of increasing its complexity. Also, correction factors are introduced in [371] and [372] to reduce large-signal model error. High-frequency link voltages, current, and power are described in [373] and [374] using Fourier series. [375] presents a frequency-domain study of high-frequency links utilizing ac phasor theory. Furthermore, [376] proposed a full-order Frequency-Domain Model of the DAB converter that uses the Toeplitz operator to generate the state equations for each harmonic of a state variable. The GAM methodology is the most utilized in literature, although these works fail to account for the dynamics of the output capacitor's parasitic resistance.

Furthermore, prior research has examined a variety of control mechanisms for controlling power flow in DAB converters. PI control is a popular approach due to its simplicity. However, PI controllers struggle with parameter fluctuations and external disturbances, resulting in poor response times and possible instability in fast charging situations [377, 378]. Fuzzy logic control is more robust than PI control, but it needs sophisticated design and tuning methods, making it unsuitable for real-world applications [379, 380]. MPC has also been researched, resulting in a rapid dynamic response. However, MPC necessitates large computational resources, which can be difficult for resource-constrained embedded systems used in EV chargers [381, 382]. SMC is also widely used in DAB converters due to its inherent ability to handle system uncertainties and disturbances. However, while it is very robust and produces a fast dynamic response, a major limitation of this technique is its inherent chattering effect, which can result in increased losses, noise, and wear on power electronic components [383–385]. DAB passivity-based control (PBC) has also been investigated due to its capacity to handle nonlinearities (resilient to parameter fluctuations and external disturbances) while maintaining system stability. However, developing a PBC system frequently needs a solid knowledge of the system's energy features, as well as complicated mathematical formulas. This complexity makes implementing PBC in DAB converters difficult [386–389].

A fundamental downside of the aforementioned controllers is their reliance on precise mathematical models of the system or an in-depth comprehension. This criterion can be difficult to meet in practical applications [390]. To solve this constraint, there is growing interest in systems that focus on estimating and rejecting disturbances, with active disturbance rejection control (ADRC) being a notable example. ADRC is a well-known control strategy for DC-DC converters [391], but there are few studies in literature that apply this technique to the DAB converter for battery charging. ADRC is generally model-independent, requiring only plant order

information, and provides good regulation and disturbance rejection capabilities to ensure the converter's steady operation. However, due to the non-linear nature of both the battery load and the DAB converter, establishing a quick dynamic response for the output current/voltage remains a difficulty with ADRC alone, particularly under fluctuating input/output voltage situations such as those encountered during battery charging. A fast dynamic response is essential for fast charging applications because it allows the converter to quickly adjust the charging current to suit the battery's requirements and maximize charging efficiency [392–395].

As previously said, practically every DAB converter application requires robust and excellent dynamic transient performance under difficult and unpredictable situations, such as input voltage fluctuations and output load disturbances. Several combined feedback-feedforward control strategies have been developed, all of which attempt to considerably improve the converter's dynamic response during load transients or changes in reference currents/voltages. In [396], the load current is measured and supplied through a feedforward circuit to generate a phase shift that is added to the phase shift produced by the voltage feedback control loop. In this scenario, sudden load changes can cause a step change in the phase shift in the feedforward circuit, resulting in a speedy change in the converter output power and hence tight output voltage regulation. Another feedforward control system suggested in [397] is virtual direct power control (VDPC). This method enhances the converter's dynamic performance by introducing a virtual output voltage, which eliminates the dependence of the feedforward phase-shift on circuit parameters such as transformer turns ratio, switching frequency and inductance. Furthermore, [398] proposes an output-impedance shaping method based on load current feedforward to improve the DAB converter's dynamic response. Moreover, [399] presents a dual-terminal voltage feedforward based direct power control scheme (DVF-DPC) to assist the converter in attaining speedy and exact output power regulation under scenarios such as startup, load step-change, power reference step-change, and voltage variations. In addition, [400] suggests a direct actual power control (DAPC) strategy based on virtual impedance estimation (VIE) for a current-fed DAB converter that achieves quick transient response for step changes in reference output voltage without overshoots, load step change, or input voltage fluctuation. Another way for dynamically improving the DAB converter's response is inductor peak current mode control, which employs current modulation rather than phase shift modulation [401,402]. The benefits of this approach include transformer over-current prevention, elimination of DC-offset transformer current during step changes in phase shift, and the feedforward path's independence from circuit parameters such as inductance and switching frequency. However, these strategies are often exclusively used in SPS-modulated systems. Accordingly, [403] proposes a simple power estimation approach using TPS. This approach, based on the DAB converter's operational parameters, improves the dynamic response of the output voltage. Also, [404] proposes an H-Infinity robust controller with load current feedforward for a DAB converter using DPS modulation, with the main goal of improving the converter's dynamic response while accounting for parameter uncertainty caused by variations in input voltage across a wide range as well as load uncertainty. Finally, [405] presents an Improved Dynamic Response method with Dual Phase-Shift (IDR-DPS) for a DAB DC-DC converter. This IDR-DPS technique attempts to improve system performance and remove DC bias concerns caused by power fluctuations.

There are several strategies in literature that can be used to charge EV batteries as mentioned

in Section 2.6. The CC-CV approach is the most widely utilized way of battery charging because it assures safe charging and battery health. To accomplish CC-CV charging, two common control mechanisms are employed. Figure 4.2a depicts the first technique, which employs two distinct single battery current and voltage feedback loops that alternate depending on the charging state [406, 407]. An alternate strategy is to nest the battery current control loop within the voltage loop (Figure 4.2b) [408, 409]. As a result, the battery current is always under control during both the CC and CV stages, thereby protecting the battery from overcurrent and extending its lifetime. Furthermore, providing a seamless transition between the two primary charging stages (CC and CV) is essential for EV battery charging [410]. However, this transition may produce disturbances that disrupt the DAB converter's performance, potentially resulting in higher thermal stress on components as well as voltage and current spikes that jeopardize system stability and battery health [411].

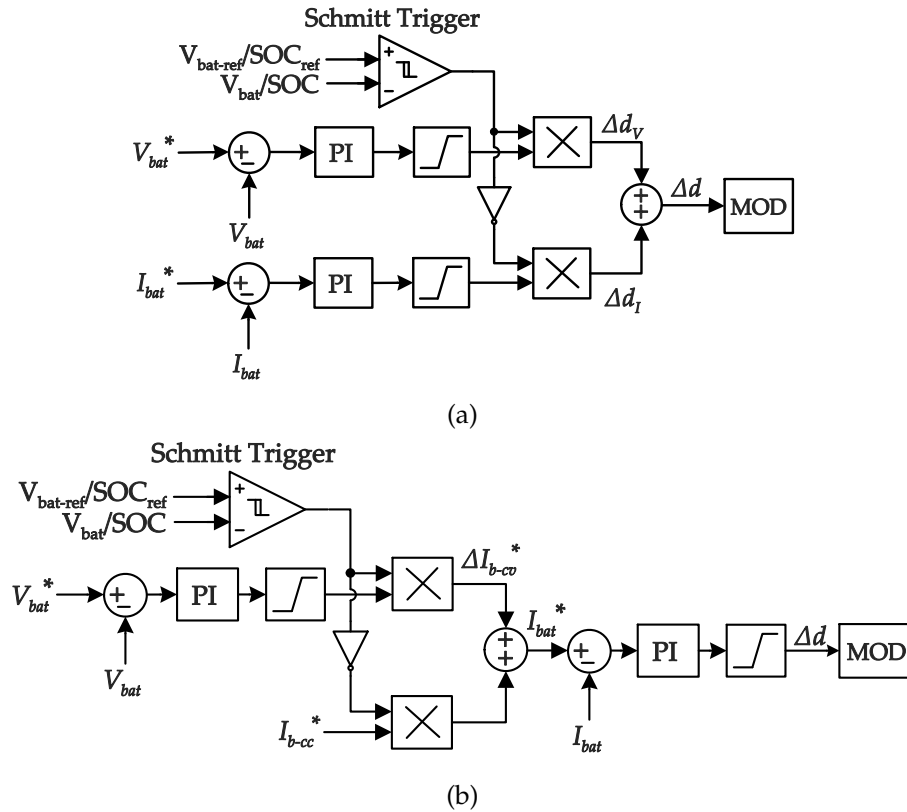


Figure 4.2: Battery voltage and current regulations: (a) two single feedback loops (b) one cascaded feedback loop.

There are few studies in literature that attempt to address this transition phenomenon, thereby increasing the dynamic response of DC-DC converters used for battery charging. A fast current controller (FCC) based on direct power control is suggested by [412] for monitoring the desired output current under various input/output parameter variations; however, this work only uses the CC charging technique with a single current loop, and thus does not address the issues that arise when two cascaded loops are used. Moreover, [413] suggests a duty ratio feedforward control strategy for achieving quick current dynamic response in a bidirectional H-bridge. Again, a single loop CC stage is used without regard for the CV stage. The authors of [414]

suggest a Kalman filter-based SoC estimating technique for decreasing switching transients during charging mode selection, and simulation results show improved performance. Another study [415] used a combination of fuzzy-PI control and Bayesian regularization (BR) algorithm-trained artificial neural network (ANN)-based control to address potential discontinuities in charging current and voltage caused by the transition from CC to CV. Additionally, [416] suggests a probabilistic fuzzy neural network (PFNN) controller for a phase shift full bridge (PSFB) DC-DC converter to significantly reduce the discontinuous charging voltage and current during the transition between the CC and CV charging modes, with experimental results demonstrating that the proposed controller achieves smooth voltage and current responses, faster response times, and improved efficiency during the CC-CV transition. Finally, [417] presents a Schmitt trigger strategy for decreasing switching transients during the CC-CV mode transition, with hardware-in-the-loop simulations confirming its usefulness. This extra Schmitt trigger circuit increases system component and power losses.

Building on these prior works, this chapter presents an enhanced GAM technique based on SPS modulation in which the parasitic resistance of the output capacitor is evaluated and the impact on system dynamics is investigated. The revised GAM model is then utilized to construct a PI controller as well as a novel simple feedforward control system that can dynamically aid in battery charging, solving the challenging task of making a seamless transition between the CC and CV modes of operation. Following that, the PI control system is replaced with both LADRC and NLADRC, describing their design process and proposing novel power-based and droop-based feedforward techniques that significantly improve the dynamic performance, mitigate disturbances, and strengthen the DAB converter for fast EV battery charging.

Droop control is a decentralized control strategy commonly employed in power systems that enables numerous converters to automatically share power without the need for sophisticated communication protocols [418, 419]. By introducing a droop-based approach into the LADRC framework, this work attempts to produce faster response times for output and input converter currents/voltages, allowing the converter to quickly adjust to changing battery voltage and grid conditions throughout the fast-charging process. The droop-based technique features an adaptive control system that modifies the reference values based on load conditions, i.e. it dynamically adjusts the converter's operating point, resulting in a more seamless and smooth transition between the CC and CV charging stages. These droop-based strategies provide a novel approach to addressing the challenges of traditional techniques and mitigating the disruptions commonly associated with these transitions, hence retaining converter performance and reliability. Furthermore, by combining droop-based feedforward control and LADRC, the proposed system not only improves dynamic performance but also lowers peak input currents. This reduction enables the use of lower-rated components in the converter design, thus cutting total costs and boosting the practicality of implementing more efficient and reliable fast-charging stations on a broad scale.

The remainder of this chapter is organized as follows: Section 4.2 analyzes the operation of a DAB DC-DC converter based on SPS modulation, while Section 4.3 models the system components, including the DAB GAM and Thevenin battery model. Section 4.4 explains the proposed PI, LADRC, and NLADRC control systems, as well as the novel performance enhancement feedforward approaches and mathematical derivations. Some MATLAB/Simulink

numerical simulations are also included to validate the control algorithms described in this section, as well as comparisons of various control strategies in terms of robustness and response time, and Section 4.5 concludes the work.

4.2 DAB Converter Principles of Operation under SPS Modulation

4.2.1 Steady State Operation

As represented in the typical DAB converter topology shown in Figure 4.1, the input and output DC voltages are converted into two intermediate high frequency square wave signals (V_1 and V_2) by the two symmetrical full bridges. By using single-phase shift modulation on each H-bridge, the power flow can be controlled by adjusting the phase shift angle between Full-bridge 1 and Full-bridge 2. Depending on the sign of the phase shift angle, power can flow from left to right or right to left. If the phase shift angle is positive, V_2 lags V_1 and power flows from left to right whereas if the phase shift angle is negative, V_1 lags V_2 and power flows from right to left. Under SPS modulation, each full bridge operates with the same switching frequency and a duty cycle of 50%.

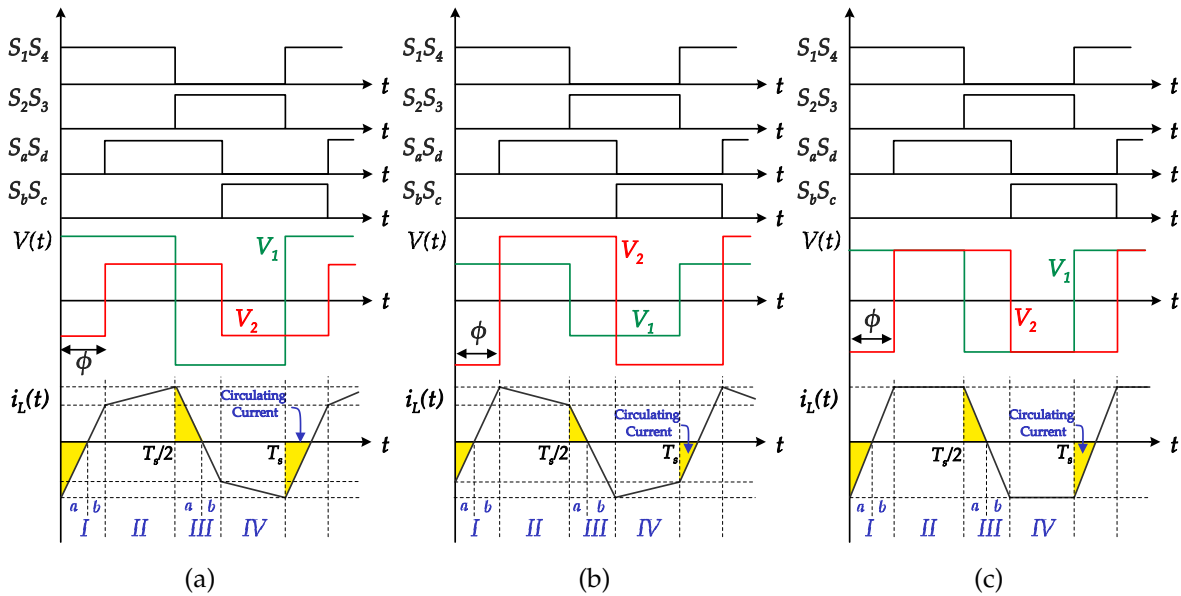


Figure 4.3: Typical theoretical waveforms of DAB converter under SPS modulation (a) buck mode ($V_g > V_o/n$) (b) boost mode ($V_g < V_o/n$) (c) gainless mode ($V_g = V_o/n$).

Figure 4.3 shows the typical waveforms of the converter with positive power flow operating in different SPS modes. The switching sequence is divided into four intervals (I, II, III, and IV) based on the phase shift between the voltages at the primary and secondary of the transformer. This division doesn't take into account the deadtime between the switches. Intervals I and III are further subdivided into two sub-intervals (I-a, I-b, III-a and III-b) as the inductor current waveform is both positive and negative during these intervals. The direction of current flow in the DAB converter during each of these intervals is shown in Figure 4.4.

One downside of the SPS modulation approach is the generation of significant circulating

currents during power flow due to the mismatched nature of the voltages on both sides of the transformer [420]. The shaded area in Figure 4.3's inductor current waveform represents this impact. This causes increased power losses, reducing power transmission efficiency. This impact can be decreased or eliminated by utilizing more complex modulation techniques, which will be discussed in the following chapter.

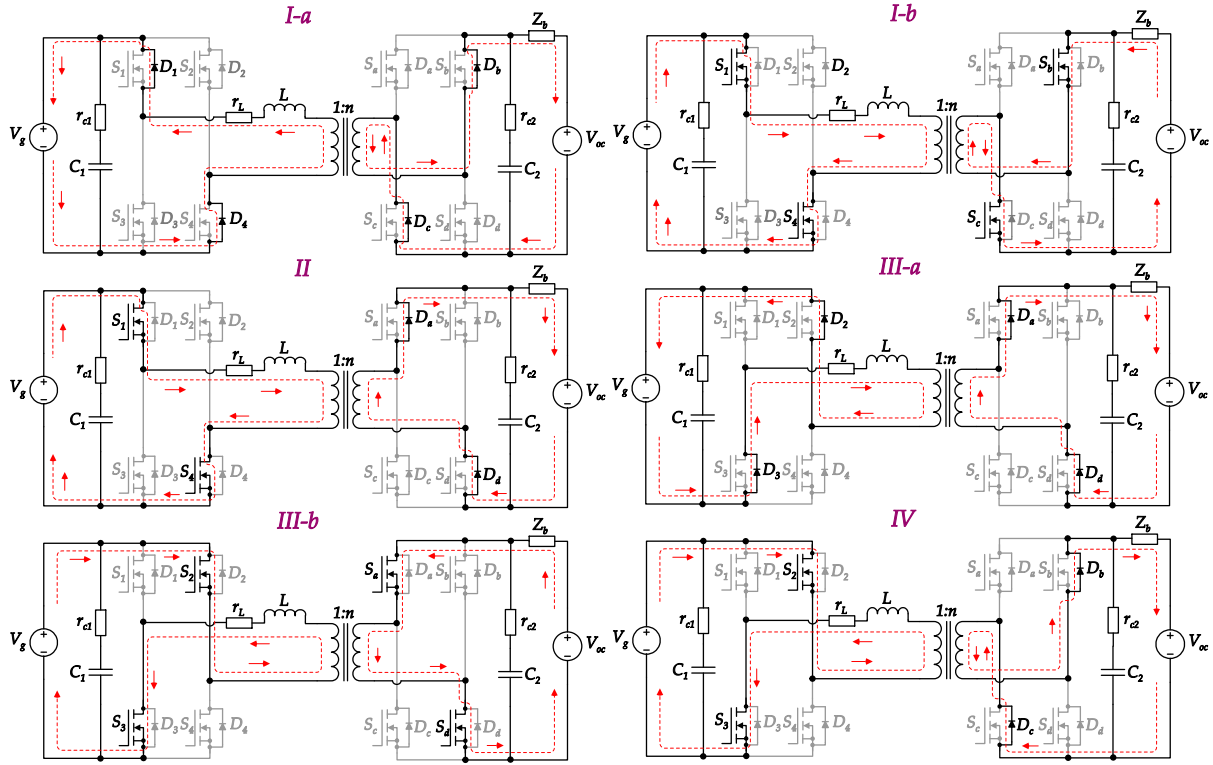


Figure 4.4: Operational modes of DAB converter under SPS modulation for forward power flow.

Figure 4.5 shows the inductor step voltage alongside a more detailed analysis of the inductor current at each switching interval. The phase shift, ϕ , between V_1 and V_2 is defined as

$$\phi = \frac{DT_s}{2} \quad (4.1)$$

Where D is the phase shift ratio and T_s is the switching period which is the reciprocal of the switching frequency f_s . The currents I_1 and I_2 define the currents at which the switching devices switch. In buck mode, I_1 is the switching current of the secondary bridge and I_2 is the switching current of the primary bridge and vice versa in boost mode.

The slope of the inductor current during each interval can be derived using Faraday's law. From this, the currents I_1 and I_2 can be derived as a function of t_1 and t_2 during interval I as given in (4.2). This analysis considers the buck mode of operation.

$$\begin{cases} I_1 = \frac{\left(V_g + \frac{V_o}{n}\right)}{L} t_2 \\ I_2 = \frac{\left(V_g + \frac{V_o}{n}\right)}{L} t_1 \end{cases} \quad (4.2)$$

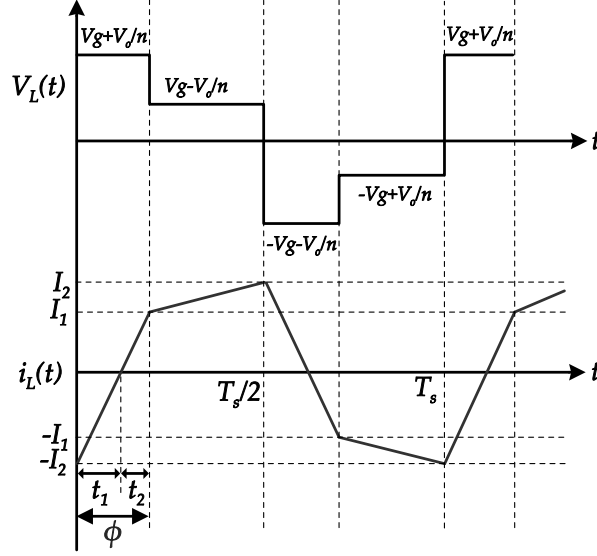


Figure 4.5: Detailed representation of inductor voltage and current.

From (4.2), we can derive (4.3) for interval I considering that $t_1 + t_2 = \phi$.

$$I_1 + I_2 = \frac{\left(V_g + \frac{V_o}{n}\right)}{L} \phi \quad (4.3)$$

Moreover, the difference between I_2 and I_1 during interval II can be derived from Figure 5 and is given in (4.4).

$$I_2 - I_1 = \frac{\left(V_g - \frac{V_o}{n}\right)}{L} \left(\frac{T_s}{2} - \phi\right) \quad (4.4)$$

From (4.3) and (4.4), the switching currents are given by (4.5).

$$\begin{cases} I_1 = \frac{T_s V_g}{4L} [(2D - 1) + M] \\ I_2 = \frac{T_s V_g}{4L} [1 + (2D - 1)M] \end{cases} \quad (4.5)$$

Where M is the converter gain given by V_o/nV_g . Using (4.5), we can derive the current shift times t_1 and t_2 from (4.2) as in (4.6)

$$\begin{cases} t_1 = \frac{T_s [1 + (2D - 1)M]}{4(1 + M)} \\ t_2 = \frac{T_s [(2D - 1) + M]}{4(1 + M)} \end{cases} \quad (4.6)$$

The input current is gotten by reflecting the inductor current to the input port noting that $i_{in} = i_L$ when switch pair S_1S_4 is ON while $i_{in} = -i_L$ when switch pair S_2S_3 is ON. The resulting waveform is shown in Figure 4.6a. The average input current can be obtained by integrating its waveform (signed sum of area under the graph) over half a switching period due to half wave symmetry as in (4.7). It can also be noticed from Figure 4.6a that the ripple frequency is twice the switching frequency [421].

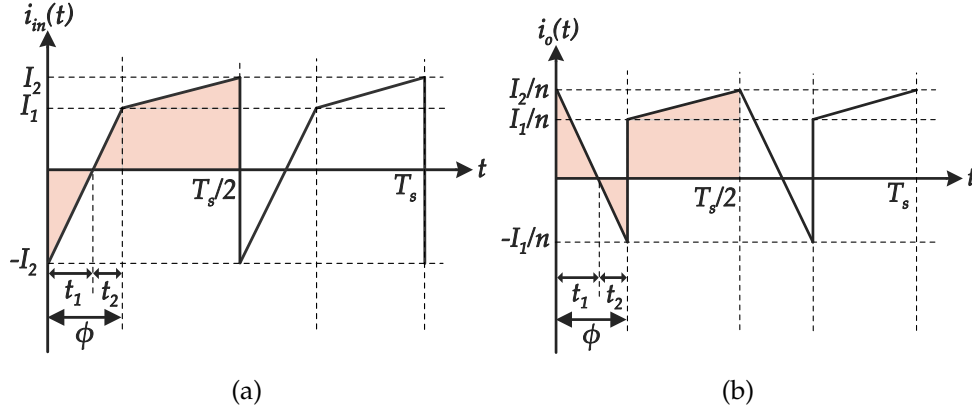


Figure 4.6: (a) Input current of DAB converter (b) Output current of DAB converter.

$$\langle i_{in} \rangle = \frac{2}{T_s} \left[\frac{t_2 I_1}{2} - \frac{t_1 I_2}{2} + (I_1 + I_2) \left(\frac{T_s}{2} - \phi \right) \right] \quad (4.7)$$

By using equations (4.1)–(4.4), equation (4.7) can be simplified to obtain equation (4.8).

$$\langle i_{in} \rangle = \frac{V_o D(1 - |D|)}{n L f_s} \quad (4.8)$$

The load current is gotten as the average value of the output current in Figure 4.6b ($i_o = I_L$ when $S_a S_d$ are ON and $i_o = -I_L$ when $S_b S_c$ are ON). Just as with the input current, the average current value is derived by integrating the output current waveform (the signed sum of the area under the graph) over half a switching period as given by (4.9). Like the input current, the output current ripple frequency is twice the switching frequency.

$$\langle i_o \rangle = \frac{2}{n T_s} \left[\frac{t_1 I_2}{2} - \frac{t_2 I_1}{2} + (I_1 + I_2) \left(\frac{T_s}{2} - \phi \right) \right] \quad (4.9)$$

By making use of equations (4.1)–(4.4), equation (4.9) can be simplified to obtain equation (4.10).

$$\langle i_o \rangle = \frac{V_g D(1 - |D|)}{2n L f_s} \quad (4.10)$$

It's noticed from (4.10) that the average output current doesn't depend on the output voltage, thus the converter acts as a current source whose value depends only on the phase shift duty ratio, input voltage, switching frequency and leakage inductance of the HFT.

From (4.10), we can derive the transferred active power as in (4.11).

$$P_t = V_o \langle i_o \rangle = \frac{V_g V_o D(1 - |D|)}{2n L f_s} \quad (4.11)$$

From (4.11), a per unit plot of power flow in the converter as a function of phase shift can be obtained, as shown in Figure 4.7. The power transferred in the positive direction increases with the phase shift angle (ϕ), peaking at $\pi/2$. Beyond this point, any further increase in the phase shift angle reduces the amount of power delivered. A similar pattern is observed in the opposite direction, with the maximum reverse power happening at $-\pi/2$.

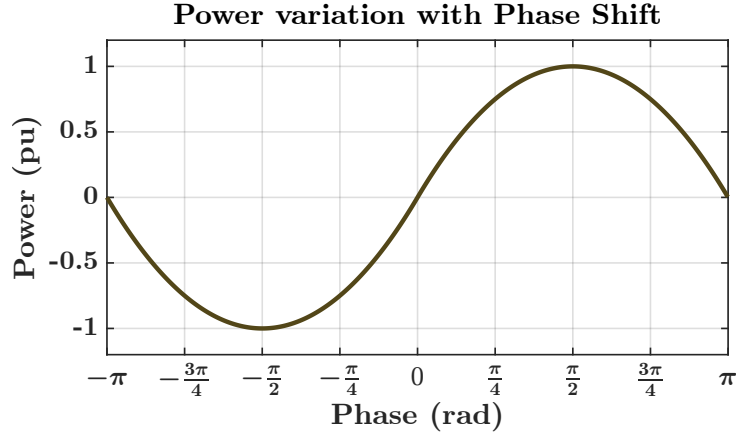


Figure 4.7: Variation of power flow with phase shift under SPS.

The transformer and the primary-side inductor see the entire primary current, thus it is important to size this RMS current as it affects copper losses. The RMS value of inductor current is given by (4.12).

$$i_{L-rms} = \sqrt{\frac{2}{T_s} \int_0^{T_s/2} i_L^2(t) dt} \quad (4.12)$$

Where $i_L(t)$ is the instantaneous value of the inductor current and given by (4.13).

$$i_L(t) = \begin{cases} \frac{I_1}{\left(\frac{DT_s}{2} - t_1\right)} t, & 0 < t < \frac{DT_s}{2} - t_1, \\ I_1 + \frac{\Delta I}{\left(\frac{T_s}{2} - \frac{DT_s}{2}\right)} t, & 0 < t < \frac{T_s}{2} - \frac{DT_s}{2}, \\ I_2 - \frac{I_2 t}{t_1}, & 0 < t < t_1. \end{cases} \quad (4.13)$$

Where $\Delta I = I_2 - I_1$. Inserting (4.13) into (4.12), we can get a simplified expression of the inductor/transformer current during buck mode given by (4.14) [422, 423].

$$i_{L-rms} = \sqrt{\frac{2}{T_s} \left[\frac{I_1^2 t_2}{3} + \frac{I_2^2 t_1}{3} + \left(I_1^2 + \frac{\Delta I^2}{3} + I_1 \Delta I \right) \left(\frac{T_s}{2} - \frac{DT_s}{2} \right) \right]} \quad (4.14)$$

A similar procedure can be used to obtain the average and RMS current values for the switching devices on both the primary and secondary full bridges of the DAB converter using the buck waveforms shown in Figure 4.3a and are respectively given listed in Tables 4.1 and 4.2 respectively.

The current that flows from the output bridge towards the load contains high frequency harmonics superimposed on its average value due to the rectification process. Thus, to reduce the ripple at the converter output, an output capacitor is used. The size of this capacitor is obtained from (4.15) and it's calculated such that it satisfies the largest ripple voltage (ΔV_o) allowed. The input capacitor value can also be obtained using (4.15) but V_g should become V_o .

$$C_{out} = \frac{V_{g,max} D_{max}^2}{8n f_s^2 L \Delta V_o} \left(\frac{D_{max}^2}{4} - D_{max} + 1 \right) \quad (4.15)$$

Table 4.1: RMS current of switching devices in primary and secondary full bridges (buck mode)

Device	Location	RMS current expression
Transistor	Primary Full bridge	$I_{rms} = \sqrt{\frac{1}{T_s} \left[\frac{I_1^2}{3} t_2 + \left(I_1^2 + \frac{\Delta I^2}{3} + I_1 \Delta I \right) \left(\frac{T_s}{2} - \frac{DT_s}{2} \right) \right]}$
Diode		$I_{RMS} = \sqrt{\frac{1}{T_s} \left(\frac{I_2^2 t_1}{3} \right)}$
Transistor	Secondary Full bridge	$I_{RMS} = \sqrt{\frac{1}{T_s} \left(\frac{I_1^2}{3} t_2 \right)}$
Diode		$i_{rms} = \sqrt{\frac{1}{T_s} \left[\frac{I_2^2}{3} t_1 + \left(I_1^2 + \frac{\Delta I^2}{3} + I_1 \Delta I \right) \left(\frac{T_s}{2} - \frac{DT_s}{2} \right) \right]}$

Table 4.2: Average current of switching devices in primary and secondary full bridges (buck mode)

Device	Location	RMS current expression
Transistor	Primary Full bridge	$I_{avg} = \frac{\frac{1}{2} I_1 t_2 + \frac{1}{2} (I_1 + I_2) \left(\frac{T_s}{2} - \frac{dT_s}{2} \right)}{\frac{T_s}{2} - t_1}$
Diode		$I_{avg} = \frac{\frac{1}{2} I_2 t_1}{t_1}$
Transistor	Secondary Full bridge	$I_{avg} = \frac{\frac{1}{2} I_1 t_2}{t_2}$
Diode		$I_{avg} = \frac{\frac{1}{2} I_2 t_1 + \frac{1}{2} (I_1 + I_2) \left(\frac{T_s}{2} - \frac{dT_s}{2} \right)}{\frac{T_s}{2} - t_2}$

4.2.2 Soft Switching Limits (Soft Switching vs Reactive Current)

To reduce the amount of switching losses, soft switching is typically employed. Two methods used are zero current switching (ZCS) and zero voltage switching (ZVS) whereby the switching devices are turned ON at either zero voltage or current. However, for the DAB converter employing SPS, ZCS can't be considered as the power will no longer be variable.

In DAB converters employing SPS, ZVS occurs during the deadtime period present when transitioning from one interval to the other. During this deadtime period, the inductor stored energy discharges the output parasitic capacitances of the switching MOSFETs and holds them close to zero before the switches are turned ON. The value of this turn-ON voltage is determined by the forward voltage drop of the internal body diodes.

The ZVS principle is explained in Figure 4.8 for the transition from Interval I-b to II. Figure 4.8a shows the current paths in the DAB converter just before the end of interval I-b when the primary switch pair S_1S_4 and secondary bridge switch pair S_bS_c are all in conduction. During this time, the voltage across C_b and C_c is zero while the voltage across C_a and C_d is the full output voltage (V_o). During the deadtime when all the switches in the secondary are OFF, the inductor-stored energy circulates current which divides into two equal parts to discharge the capacitances C_a and C_d to near zero voltage and charge the capacitances C_b and C_c to the full secondary voltage as shown in Figure 4.8b. When the discharge voltage across the capacitances C_a and C_d is equal to the forward bias voltage of the anti-parallel diodes D_a and D_d , the diodes turn ON and start conducting as shown in Figure 4.8c. The diodes conduct until their corresponding

switch is turned ON as shown in Figure 4.8d, at which point the circuit has transitioned to interval II with ZVS. The same process happens for the other transition periods [424].

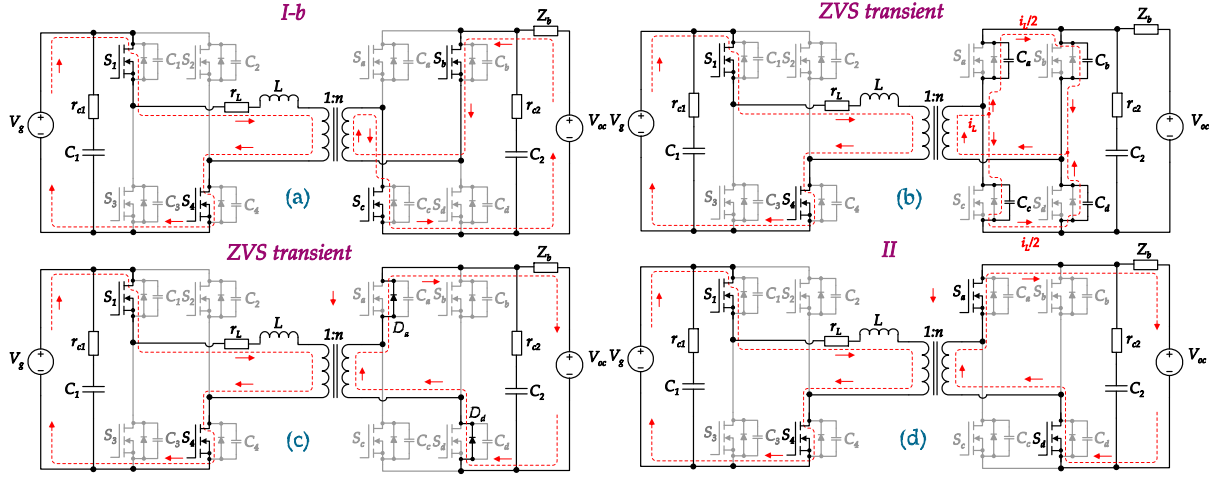


Figure 4.8: Current paths in the converter during commutation from interval I-b to II.

As explained above, the dead time (t_d) is of utmost importance for ZVS to occur. If the dead time is too short, the switch will turn ON before the body diode conducts meaning that there will be switching loss. Moreover, if it is shorter than the diode reverse recovery time, it's possible to create a short circuit or some other undesired converter behavior could be observed. Therefore, the minimum deadtime is also limited by the reverse recovery time of the body diodes. Furthermore, a too long dead time means that the diodes conduct for a very long time which will lead to more conduction losses as diodes have more conduction loss than MOSFETs. In any case, the conduction losses caused by diodes are in most cases smaller than the MOSFET switching losses, so longer dead time is more favorable than a too short deadtime. The minimum deadtime can be obtained using equation (4.16).

$$t_{d,min} = \frac{2V_{ds}C_{oss}}{I_{sw}} \quad (4.16)$$

where V_{ds} is the drain to source voltage of the switch which is V_g for the primary bridge and V_o for the secondary bridge, C_{oss} is the output parasitic capacitance that is typically given in the device's datasheet, I_{sw} is the current at the switching instant gotten from either I_1 (for output bridge) or I_2 (for input bridge).

Neglecting the energy required to charge/discharge the parasitic output capacitances, it's possible to define the boundaries of ZVS for both the input and output bridges. For this, the currents I_1 and I_2 defined in equation (4.5) are very important. To have ZVS on both bridges, I_1 and I_2 should be positive. Thus, if $M = 1$, it's observed from (4.5) that both I_1 and I_2 are greater than zero making it possible to achieve ZVS for any power transferred. If on the other hand $M < 1$, the converter works in buck mode and I_2 is always positive whereas I_1 could be negative creating hard switching operation in the output bridge. Finally, if $M > 1$, the converter works in boost mode and I_1 is always positive whilst I_2 could be negative causing hard switching in the input bridge. The ZVS working area using SPS for positive values of phase shift can be summarized as in Table 4.3.

Table 4.3: Conditions for ZVS under SPS for positive power flow

Condition	Input Bridge	Output Bridge
$I_1 > 0$ and $I_2 > 0$	ZVS	ZVS
$I_1 > 0$ and $I_2 < 0$	Non-ZVS	ZVS
$I_1 < 0$ and $I_2 > 0$	ZVS	Non-ZVS

Considering the limitations mentioned, the conditions to obtain ZVS are determined by phase shift ratio and is given by equation (4.17).

$$\begin{cases} I_1 > 0 \implies D > \frac{1-M}{2}, \text{ if } M < 1 \\ I_2 > 0 \implies D > \frac{M-1}{2M}, \text{ if } M > 1 \end{cases} \quad (4.17)$$

Figure 4.9 shows plots of the ZVS operating region with SPS modulation considering different parameters. Figure 4.9a shows that when $M = 1$, ZVS is fulfilled for any value of phase shift ratio, D . Thus, a good way to design the converter is to select a value of n to obtain $M = 1$ in nominal conditions. Moreover, the higher D is the higher the probability of working within the ZVS region. However, when $M \neq 1$, ZVS is lost at light loads. Figure 4.9b demonstrates that the ZVS region is also dependent on the value of the leakage inductance. Increasing the inductance increases the converter's soft switching ability up to very low power levels (light loads).

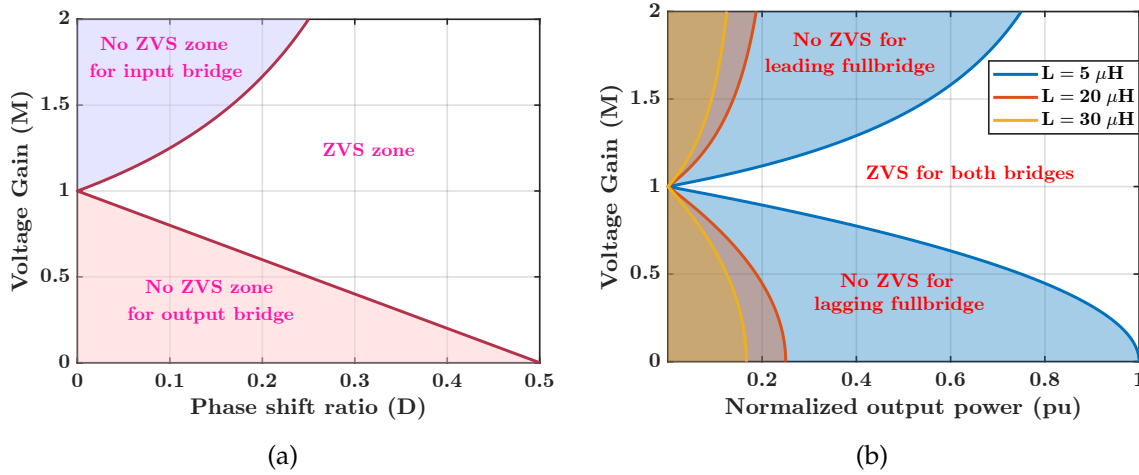


Figure 4.9: ZVS regions under SPS modulation (a) variation of converter gain with phase shift ratio (b) variation of converter gain with normalized output power for different inductor values.

Figure 4.9 shows that ZVS is increased for higher values of D and L . However, increasing these parameters leads to increased transformer reactive currents, thus higher conduction losses according to (4.18) which shows the sum of the percentage of reactive current at the input and output bridge derived by finding the negative area under the input and output current waveforms in Figure 4.6 during half a switching period and then dividing the respective expressions by the average input and output currents in (4.8) and (4.10). Therefore, D is typically chosen less than 0.35 to reduce the circulation currents.

$$\lambda_t = \lambda_o + \lambda_i = \frac{(2D - 1 + M)^2}{8D(1 - D)(1 + M)} + \frac{[(2D - 1)M + 1]^2}{8D(1 - D)(1 + M)M} \quad (4.18)$$

The boundary conditions described by (4.17) have to be fulfilled to achieve ZVS, however they don't ensure ZVS. In the absence of a snubber capacitor across the device, during turn-off, resonance would naturally occur between the intrinsic capacitance (C_{oss}) and the coupling inductance (L). Thus, to ensure ZVS, the values of I_1 and I_2 do not only have to be higher than zero but also have to be higher than a certain minimum inductor current needed to charge and discharge the output parasitic capacitances of the transistors [425]. The minimum inductor current can be obtained by noting that the energy stored in the leakage inductor must be greater than or equal to the energy stored in the equivalent output capacitances of the transistors during the deadtime interval as given in (4.19).

$$E_L \geq E_C \implies \frac{1}{2}Li_L^2 \geq 4 \left(\frac{1}{2}C_{oss}V_{ds}^2 \right) \quad (4.19)$$

From (4.19), the minimum required inductor current is given by (4.20).

$$i_{L,min} = 2V_{ds}\sqrt{\frac{C_{oss}}{L}} \quad (4.20)$$

Equation (4.20) can then be used to derive the sufficient condition to obtain ZVS for both the input and output bridges as given in (4.21).

$$\begin{cases} I_1 > i_{L,min} \implies D > \frac{1-M}{2} + \frac{4nM}{T_s}\sqrt{LC_{oss}}, & \text{if } M < 1 \\ I_2 > i_{L,min} \implies D > \frac{M-1}{2M} + \frac{4}{MT_s}\sqrt{LC_{oss}}, & \text{if } M > 1 \end{cases} \quad (4.21)$$

Finally, it is interesting to note that the ZVS method explained here helps eliminate only the turn ON losses, thus the turn OFF switching losses will still be incurred due to capacitance charging.

4.3 System Modeling

4.3.1 Thevenin Model of EV battery

To conduct power electronic simulations involving batteries, it is essential to model them electrically. From the various electrical equivalent circuit battery models described in Section 2.3.1, the second-order Thevenin equivalent model shown in Figure 4.10 has been selected for this work. This model has been chosen due to its simplicity and sufficiently accurate computational results. It does not account for the battery's self-discharge effect and the battery's open circuit voltage, resistances, and capacitances depend on both the SoC and temperature; however, this work ignores the temperature's effect on these parameters.

The parameter determination technique is carried out using a pulse discharge test. The process begins with a 1C current pulse applied for 120 seconds to discharge a fully charged battery at equilibrium. As the battery is discharged, its voltage begins to decrease. Following the application of the 120-second pulse, the cell is allowed to relax for 360 seconds. The process is continued for a series of current pulses before stopping when the battery voltage approaches the lowest threshold voltage (cut-off voltage), at which point it is regarded entirely discharged [426,427]. Figure 4.11 depicts the end-of-test battery current and voltage curves. The open circuit voltage

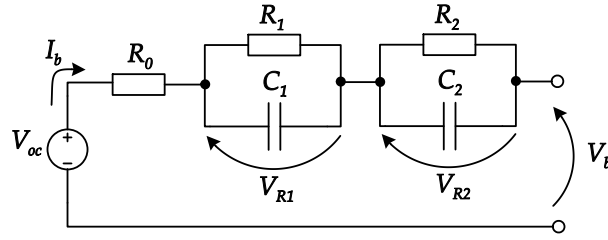


Figure 4.10: Thevenin second-order equivalent circuit battery model.

(V_{oc}) at various SoCs is determined by measuring the battery's steady voltage value right before the end of the relaxation phase, when no current flows in/out of the cell, as shown in Figure 4.11.

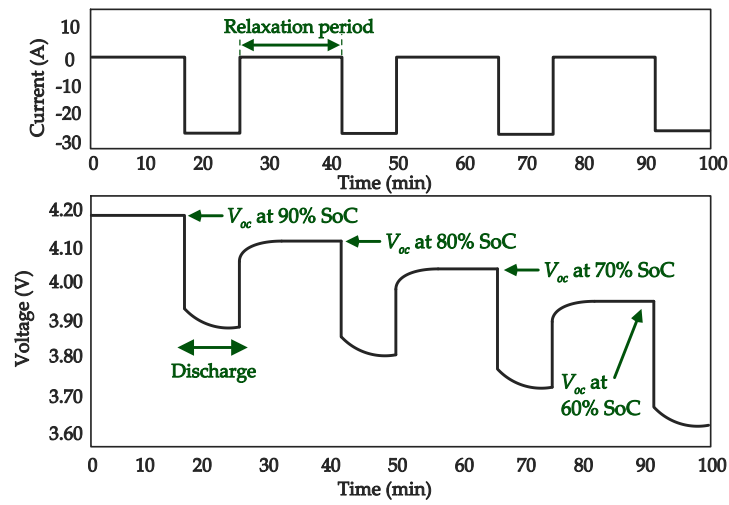


Figure 4.11: Battery current and voltage from pulse discharge test.

The additional parameters are derived by fitting an exponential curve to the observed voltage profile. The battery terminal voltage can be curve-fitted using the exponential form given in equation (4.22).

$$V_b(t) = a - be^{-\frac{t}{\tau_1}} - de^{-\frac{t}{\tau_2}} \quad (4.22)$$

From (4.22), the battery parameters can be obtained as given in (4.23) for different SoCs

$$R_o = \frac{V_{oc} - a}{I_b}, \quad R_1 = \frac{b}{I_b}, \quad R_2 = \frac{d}{I_b}, \quad C_1 = \frac{\tau_1}{R_1}, \quad C_2 = \frac{\tau_2}{R_2}. \quad (4.23)$$

The above-described method has been utilized by [428] to determine the parameters of a Li-ion battery cell and the results obtained are given in Table 4.4.

A frequency domain model of the battery can be developed as given in (4.24).

$$\begin{cases} V_b(s) = n_s V_{OC}(s) - \frac{R_o I_b(s)}{n_p} - V_{R1}(s) - V_{R2}(s), \\ V_{R1}(s) = \frac{1}{sC_1} \left(\frac{I_b(s)}{n_p} - \frac{V_{R1}(s)}{R_1} \right), \\ V_{R2}(s) = \frac{1}{sC_2} \left(\frac{I_b(s)}{n_p} - \frac{V_{R2}(s)}{R_2} \right). \end{cases} \quad (4.24)$$

Table 4.4: Parameters of the second-order Thevenin equivalent model

SoC	V_{oc}	R_o (m Ω)	τ_1 (s)	R_1 (m Ω)	C_1 ($\times 10^3$ F)	τ_2 (s)	R_2 (m Ω)	C_2 ($\times 10^3$ F)
0	3.46	65	1.4769	33.4	0.0442	51.5996	16.9	0.3044
0.05	3.50	72	5.5741	5.1	1.0871	62.0732	9.1	0.6801
0.1	3.56	70	5.2938	4.1	1.2881	66.0502	8.5	0.7804
0.15	3.62	67	7.8370	4.3	1.8020	81.9001	7.9	1.0314
0.2	3.69	55	5.3763	4.0	1.3375	69.9301	9.1	0.7719
0.3	3.76	63	18.7512	7.2	2.6151	86.1204	2.3	3.5084
0.4	3.78	59	15.5497	4.5	3.4769	69.7350	4.8	1.4490
0.5	3.81	60	2.98833	2.5	1.1805	45.3309	8.6	0.5300
0.6	3.88	58	7.1276	4.7	1.5090	56.7859	8.7	0.6500
0.7	3.96	57	6.7249	52	1.2954	60.4230	10.2	0.5897
0.8	4.05	55	4.6404	47	0.9950	47.1254	10.2	0.4634
0.9	4.1	61	5.3220	4.9	1.0819	89.7116	43.3	0.8196
1.0	4.19	63	10.8684	4.3	2.5064	93.8967	7.0	1.3357

Where n_s and n_p are respectively the number of cells connected in series and parallel. The SoC is computed based on the coulomb counting technique. Here, the discharging current of the battery is measured and integrated over time to estimate the SoC [429]. This is given mathematically below.

$$\text{SoC}(t) = \text{SoC}(t_0) - \frac{\int_{t_0}^{t_0+\tau} I_b d\tau}{Q_{\text{rated}}} \quad (4.25)$$

where Q_{rated} is the rated or nominal capacity of the battery (Ah).

The resistance and capacitance values in Table 4.4 are used to create a 1D look-up table at different SOC's in MATLAB/Simulink from which the Thevenin equivalent model is then constructed using (4.24) and (4.25) as shown in Figure 4.12.

4.3.2 Enhanced Generalized Average Model (GAM) of DAB Converter

4.3.2.1 Basics of the GAM Framework

The Generalized Average Modeling (GAM) method, also known as dynamic phasor, is a frequency-domain technique that utilizes the complex exponential Fourier series expansion of periodic time-dependent variables to expand the state equations of a given converter circuit. This yields a differential equation governing the evolution of the complex magnitudes of successive harmonics for each state variable. While the choice of the number of harmonics for a specific state variable is discretionary, the accuracy of the approach is enhanced with an increased number of harmonics considered [430, 431].

The complex Fourier series representation of a periodic time signal $x(t)$ is given by

$$x(t) = \sum_{k=-\infty}^{\infty} x_k(t) e^{jk\omega_s t} \quad (4.26)$$

where $k \in \mathbb{Z}$, ω_s is the angular switching frequency, and x_k is the k^{th} harmonic complex Fourier coefficient of the variable x , which can be defined by a sliding average over the switching period

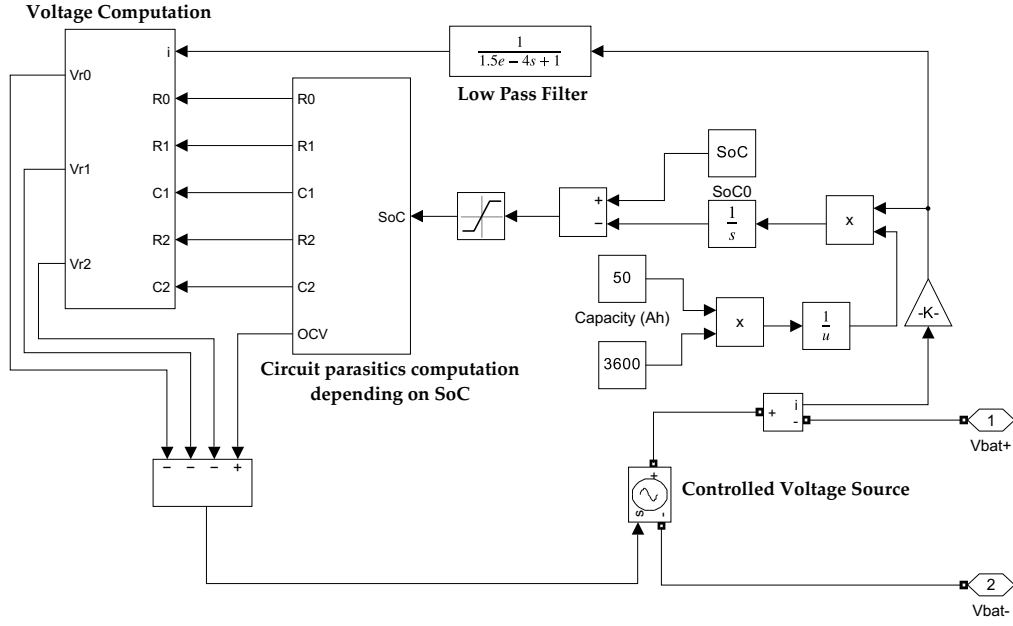


Figure 4.12: MATLAB/Simulink implementation of the second order Thevenin equivalent circuit battery model.

T_s as in (4.27).

$$x_k(t) = \frac{1}{T_s} \int_{t-T_s}^t x(\tau) e^{-jk\omega_s \tau} d\tau = \langle x \rangle_k(t) \quad (4.27)$$

Equations (4.26) and (4.27) lead to two fundamental properties for GAM simplification. The first concerns the time differentiation property of the complex Fourier series. According to this property, the derivative of the k^{th} -order sliding average of variable x is given by

$$\frac{d\langle x \rangle_k(t)}{dt} = -jk\omega_s \langle x \rangle_k(t) + \left\langle \frac{dx}{dt} \right\rangle_k(t) \quad (4.28)$$

The second property uses the 1D discrete convolution property of the complex Fourier series to define the k^{th} harmonic complex Fourier coefficient of the product of two variables x and y as given in (4.29).

$$\langle xy \rangle_k(t) = \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i}(t) \langle y \rangle_i(t) \quad (4.29)$$

Equations (4.28) and (4.29) are the underlying GAM expressions which can be used to model the DAB converter [432, 433]. Moreover, it is possible to see classical state-space averaging as a particular instance of the GAM framework, where only $k = 0$ terms are taken into account [434]. For this work, $k = 0$ for DC voltages while $k = \pm 1$ for the transformer AC currents and switching function components at the switching frequency ω_s .

4.3.2.2 Large Signal Model

To perform GAM, we transform the DAB circuit in Figure 4.1 into its equivalent shown in Figure 4.13. In this circuit, $S_1(t)$ and $S_2(t)$ are respectively the switching functions of the primary and

secondary H-bridges, and they are given by (4.30) and (4.31).

$$S_1(\theta) = \begin{cases} 1, & 0 \leq \theta < \pi \\ -1, & \pi \leq \theta < 2\pi \end{cases} \quad (4.30)$$

$$S_2(\theta) = \begin{cases} 1, & \phi \leq \theta < \pi + \phi \\ -1, & \pi + \phi \leq \theta < 2\pi + \phi \end{cases} \quad (4.31)$$

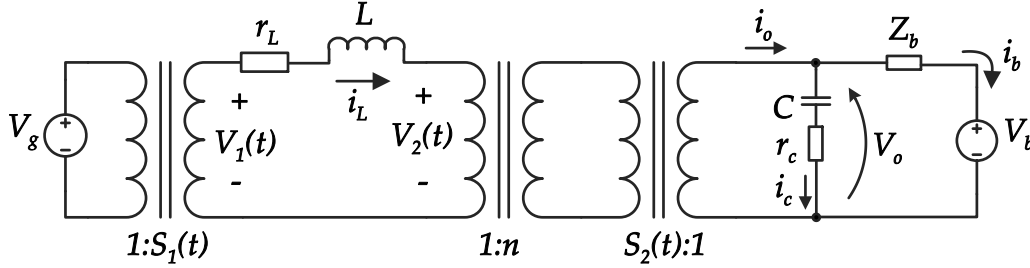


Figure 4.13: DAB equivalent circuit for GAM.

The exponential Fourier series representation of S_1 and S_2 are respectively given by (4.32). Figure 14 shows a comparison between the piece-wise switching functions given by (4.30) and (4.31) with the Fourier series obtained with (4.32) over two periods for $M = 40$ and $\phi = \pi/4$

$$S_1(\theta) = \sum_{m=\text{odd}}^{\infty} \left(\frac{2}{j\pi m} e^{jm\theta_s} \right), \quad (4.32a)$$

$$\begin{aligned} S_2(\theta) &= S_1(\theta - \phi) = \sum_{m=\text{odd}}^{\infty} \left(\frac{2}{j\pi m} e^{jm(\theta_s - \phi)} \right) \\ &= \sum_{m=\text{odd}}^{\infty} \left(\frac{2}{j\pi m} e^{-jm\phi} e^{jm\theta_s} \right). \end{aligned} \quad (4.32b)$$

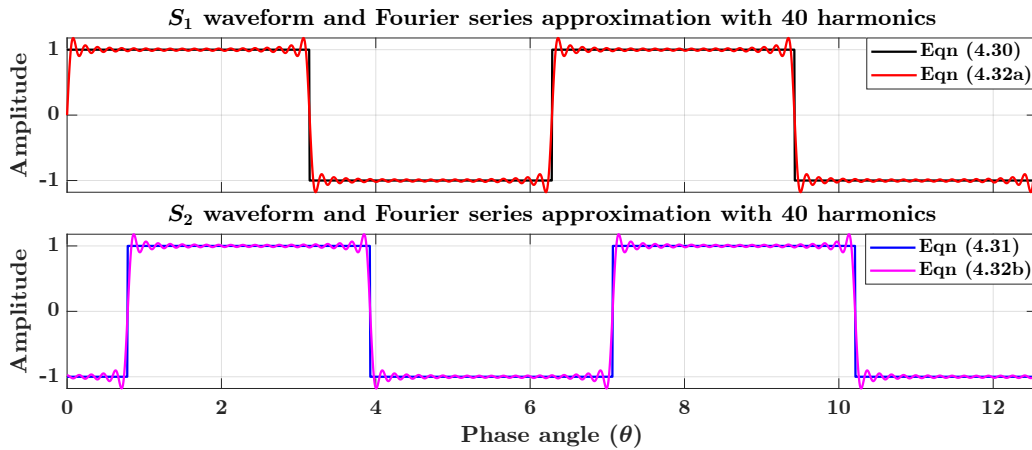


Figure 4.14: Visualization of the Fourier series representation of S_1 and S_2 .

From Figure 4.13, the following circuit equations can be derived:

$$\frac{di_L}{dt} = \frac{v_g S_1}{L} - \frac{i_L r_L}{L} - \frac{(S_2)^2 i_L r_c}{n^2 L} + \frac{S_2 i_b r_c}{nL} - \frac{v_c S_2}{nL} \quad (4.33)$$

$$\frac{dv_c}{dt} = \frac{i_L S_2}{nC} - \frac{i_b}{C} \quad (4.34)$$

Applying (4.28) to (4.33) and considering only the first harmonic content, we get the following expression:

$$\frac{d\langle i_L \rangle_1}{dt} = -j\omega \langle i_L \rangle_1 + \frac{\langle v_g S_1 \rangle_1}{L} - \frac{\langle i_L r_L \rangle_1}{L} - \frac{\langle (S_2)^2 i_L r_c \rangle_1}{n^2 L} + \frac{\langle S_2 i_b r_c \rangle_1}{nL} - \frac{\langle v_o S_2 \rangle_1}{nL} \quad (4.35)$$

Now the Fourier coefficients of S_1 , S_2 can be easily derived from (4.32) as:

$$\begin{cases} \langle S_1 \rangle_0 = 0; & \langle S_1 \rangle_1 = \frac{2}{j\pi} = -j\frac{2}{\pi}, \\ \langle S_2 \rangle_0 = 0; & \langle S_2 \rangle_1 = \frac{2}{j\pi} e^{-j\phi} = \frac{2}{\pi} [-\sin(\phi) - j\cos(\phi)]. \end{cases} \quad (4.36)$$

The Fourier coefficients of $(S_2)^2$ can be gotten by making use of (4.29) as given in (4.37):

$$\begin{cases} \langle S_2 S_2 \rangle_0 = \langle S_2 \rangle_1 \langle S_2 \rangle_{-1} + \langle S_2 \rangle_{-1} \langle S_2 \rangle_1 + \langle S_2 \rangle_3 \langle S_2 \rangle_{-3} \\ \quad + \langle S_2 \rangle_{-3} \langle S_2 \rangle_3 + \dots \\ \quad = \frac{8}{\pi^2} \sum_{p=0}^{\infty} \frac{1}{(2p+1)^2} = \frac{8}{\pi^2} \left(\frac{\pi^2}{8} \right) = 1, \\ \langle S_2 S_2 \rangle_1 = \langle S_2 \rangle_1 \langle S_2 \rangle_0 + \langle S_2 \rangle_0 \langle S_2 \rangle_1 + \langle S_2 \rangle_{-1} \langle S_2 \rangle_2 \\ \quad + \langle S_2 \rangle_2 \langle S_2 \rangle_{-1} + \dots \\ \quad = 0. \end{cases} \quad (4.37)$$

Then from (4.35) and using (4.29), the following coefficients can be gotten:

$$\begin{cases} \langle v_g S_1 \rangle_1 = \langle v_g \rangle_0 \langle S_1 \rangle_1 + \underbrace{\langle v_g \rangle_1 \langle S_1 \rangle_0}_{(=0)} = \langle v_g \rangle_0 \langle S_1 \rangle_1 = -j\frac{2v_g}{\pi}, \\ \langle i_L (S_2)^2 \rangle_1 = \underbrace{\langle i_L \rangle_0 \langle (S_2)^2 \rangle_1}_{(=0)} + \langle i_L \rangle_1 \langle (S_2)^2 \rangle_0 = \langle i_L \rangle_1, \\ \langle i_b S_2 \rangle_1 = \langle i_b \rangle_0 \langle S_2 \rangle_1 + \langle i_b \rangle_1 \langle S_2 \rangle_0 = \langle i_b \rangle_0 \langle S_2 \rangle_1 \\ \quad = \frac{2i_b}{\pi} [-\sin(\phi) - j\cos(\phi)], \\ \langle v_c S_2 \rangle_1 = \langle v_c \rangle_0 \langle S_2 \rangle_1 + \langle v_c \rangle_1 \langle S_2 \rangle_0 = \langle v_c \rangle_0 \langle S_2 \rangle_1 \\ \quad = \frac{2v_c}{\pi} [-\sin(\phi) - j\cos(\phi)]. \end{cases} \quad (4.38)$$

Let $\langle i_L \rangle_1 = x_1 + jx_2$. Using this and inserting (4.38) into (4.35), the following expressions are gotten:

$$\begin{cases} \frac{dx_1}{dt} = \omega x_2 - \frac{r_L}{L} x_1 - \frac{r_c}{n^2 L} x_1 - \frac{2i_b r_c}{\pi n L} \sin(\phi) + \frac{2v_c}{\pi n L} \sin(\phi), \\ \frac{dx_2}{dt} = -\omega x_1 - \frac{r_L}{L} x_2 - \frac{2v_g}{\pi L} - \frac{r_c}{n^2 L} x_2 - \frac{2i_b r_c}{\pi n L} \cos(\phi) + \frac{2v_c}{\pi n L} \cos(\phi). \end{cases} \quad (4.39)$$

Now, applying (4.28) to (4.34) and considering only the zero-order harmonic, the following expression is gotten.

$$\frac{d\langle v_c \rangle_0}{dt} = \frac{\langle i_L S_2 \rangle_0}{nC} - \frac{\langle i_b \rangle_0}{C} \quad (4.40)$$

From (4.40) and using (4.29), the following Fourier coefficients can be derived:

$$\begin{aligned}\langle i_L S_2 \rangle_0 &= 2 [\operatorname{Re}(\langle i_L \rangle_1) \operatorname{Re}(\langle S_2 \rangle_1) + \operatorname{Im}(\langle i_L \rangle_1) \operatorname{Im}(\langle S_2 \rangle_1)] \\ &= -\frac{4x_1}{\pi} \sin(\phi) - \frac{4x_2}{\pi} \cos(\phi).\end{aligned}\quad (4.41)$$

If it is assumed that the dynamics of the input voltage and load are much slower than those of the DAB converter, then $\langle v_c \rangle_0 = v_c$, $\langle v_o \rangle_0 = v_o$, $\langle i_o \rangle_0 = i_o$, and $\langle i_b \rangle_0 = i_b$. Using this assumption and inserting (4.41) into (4.40), the following GAM expression is obtained:

$$\frac{dv_c}{dt} = -\frac{4x_1}{\pi n C} \sin(\phi) - \frac{4x_2}{\pi n C} \cos(\phi) - \frac{i_b}{C} \quad (4.42)$$

The output equations of the system are given by:

$$\begin{cases} i_g = S_1 i_L, \\ i_o = \frac{S_2 i_L}{n}, \\ v_o = (i_o - i_b) r_c + v_c. \end{cases} \quad (4.43)$$

By applying (4.28) to (4.43), the output GAM expressions are obtained as follows:

$$\begin{cases} \langle i_g \rangle_0 = \langle S_1 i_L \rangle_0 = 2 [\operatorname{Re}(\langle i_L \rangle_1) \operatorname{Re}(\langle S_1 \rangle_1) + \operatorname{Im}(\langle i_L \rangle_1) \operatorname{Im}(\langle S_1 \rangle_1)] = -\frac{4x_2}{\pi}, \\ \langle i_o \rangle_0 = \frac{\langle S_2 i_L \rangle_0}{n} = -\frac{4x_1}{\pi n} \sin(\phi) - \frac{4x_2}{\pi n} \cos(\phi), \\ \langle v_o \rangle_0 = -\frac{4r_c x_1}{\pi n} \sin(\phi) - \frac{4r_c x_2}{\pi n} \cos(\phi) - r_c \langle i_b \rangle_0 + \langle v_c \rangle_0. \end{cases} \quad (4.44)$$

Equations (4.39), (4.42), and (4.44) give the large signal model of the DAB converter. The steady state values of x_1 , x_2 , and i_b can be obtained from (4.39) and (4.42) by zeroing out the derivatives and solving the ensuing simultaneous equations. The resulting expression in matrix form is given by:

$$\begin{bmatrix} -\frac{1}{L} \left(r_L + \frac{r_c}{n^2} \right) & \omega & -\frac{2r_c \sin(\Phi)}{\pi n L} \\ -\omega & -\frac{1}{L} \left(r_L + \frac{r_c}{n^2} \right) & -\frac{2r_c \cos(\Phi)}{\pi n L} \\ -\frac{4 \sin(\Phi)}{\pi n} & -\frac{4 \cos(\Phi)}{\pi n} & -1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ I_b \end{bmatrix} = \begin{bmatrix} -\frac{2V_c \sin(\Phi)}{\pi n L} \\ \frac{2}{\pi L} \left(V_g - \frac{V_c \cos(\Phi)}{n} \right) \\ 0 \end{bmatrix} \quad (4.45)$$

4.3.2.3 Small Signal Model

A power converter's controller design and stability analysis necessitate the construction of a small-signal control-to-output transfer function, which is the converter's dynamic response to a small deviation in the control signal. Thus, the small signal model is created by first applying a small perturbation to the variables of interest and then linearizing around the operating point. Equation (4.46) defines the perturbation signals under consideration, with upper-case variables representing steady state values, lower-case variables representing large signal states,

and lower-case variables with hats representing small signal states.

$$\begin{cases} x_1 = X_1 + \hat{x}_1, \\ x_2 = X_2 + \hat{x}_2, \\ i_b = I_b + \hat{i}_b, \\ i_g = I_g + \hat{i}_g, \\ v_g = V_g + \hat{v}_g, \\ v_c = V_c + \hat{v}_c, \\ \phi = \Phi + \hat{\phi}, \end{cases} \quad (4.46)$$

where the terms in sine and cosine are linearized according to the sinusoidal approximations given in (4.47), where q is a positive real constant, k is an arbitrary large signal variable having steady-state value K , and given a small perturbation $\hat{k}$:

$$\begin{cases} k \cos(q\phi) = (K + \hat{k}) \cos[q(\Phi + \hat{\phi})] \approx \cos(q\Phi)\hat{k} - qK \sin(q\Phi)\hat{\phi}, \\ k \sin(q\phi) = (K + \hat{k}) \sin[q(\Phi + \hat{\phi})] \approx \sin(q\Phi)\hat{k} + qK \cos(q\Phi)\hat{\phi}. \end{cases} \quad (4.47)$$

Inserting (4.46) into the large signal DAB model in (4.39), (4.42), and (4.44) yields the small signal model written in state-space form as:

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{v}_c \end{bmatrix} = A \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{v}_c \end{bmatrix} + B \begin{bmatrix} \hat{v}_g \\ \hat{i}_b \\ \hat{\phi} \end{bmatrix}, \\ \begin{bmatrix} \hat{i}_g \\ \hat{i}_o \\ \hat{v}_o \end{bmatrix} = G \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{v}_c \end{bmatrix} + H \begin{bmatrix} \hat{v}_g \\ \hat{i}_b \\ \hat{\phi} \end{bmatrix}, \end{cases} \quad (4.48)$$

where

$$\begin{aligned} A &= \begin{bmatrix} -\frac{1}{L} \left(r_L + \frac{r_c}{n^2} \right) & \omega & \frac{2 \sin(\Phi)}{\pi n L} \\ -\omega & -\frac{1}{L} \left(r_L + \frac{r_c}{n^2} \right) & \frac{2 \cos(\Phi)}{\pi n L} \\ -\frac{4}{\pi n C} \sin(\Phi) & -\frac{4}{\pi n C} \cos(\Phi) & 0 \end{bmatrix}, \\ B &= \begin{bmatrix} 0 & -\frac{2r_c \sin(\Phi)}{\pi n L} & \frac{2 \cos(\Phi)}{\pi n L} (V_c - r_c I_b) \\ \frac{2}{\pi L} & -\frac{2r_c \cos(\Phi)}{\pi n L} & \frac{2 \sin(\Phi)}{\pi n L} (r_c I_b - V_c) \\ 0 & -\frac{1}{C} & -\frac{4}{\pi n C} (X_1 \cos(\Phi) - X_2 \sin(\Phi)) \end{bmatrix}, \\ G &= \begin{bmatrix} 0 & -\frac{4}{\pi} & 0 \\ -\frac{4}{\pi n} \sin(\Phi) & -\frac{4}{\pi n} \cos(\Phi) & 0 \\ -\frac{4r_c}{\pi n} \sin(\Phi) & -\frac{4r_c}{\pi n} \cos(\Phi) & 1 \end{bmatrix}, \\ H &= \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{4}{\pi n} (-X_1 \cos(\Phi) + X_2 \sin(\Phi)) \\ 0 & -r_c & \frac{4r_c}{\pi n} (-X_1 \cos(\Phi) + X_2 \sin(\Phi)) \end{bmatrix}. \end{aligned}$$

From (4.48), we may derive the control equations required to create the DAB's control system. To validate the developed GAM, a small signal analysis is performed in PLECS for a DAB converter switching at 40 kHz and phase-shifted by 0.3π . Table 4.5 shows the design specifications for the DAB converter used to perform the model validation. Figure 4.15 shows a bode plot of the phase shift-to-output voltage transfer function ($V_o(s)/\phi(s)$) comparing the results obtained from both the GAM analysis and the PLECS simulation. Both models initially follow a similar trajectory as there is a gradual decrease in magnitude at lower frequencies and a corresponding phase lag as frequency increases. However, at higher frequencies, some divergences can be detected, particularly in the magnitude response where the PLECS simulation shows higher values and exhibits greater fluctuations. On the contrary, the GAM's response is smoother implying that it doesn't fully capture certain high frequency converter dynamics like switching effects or non-linearities which are more accurately reflected in the PLECS model. Overall, the GAM provides a reasonable approximation of the system's behavior especially in the lower and mid-frequency regions.

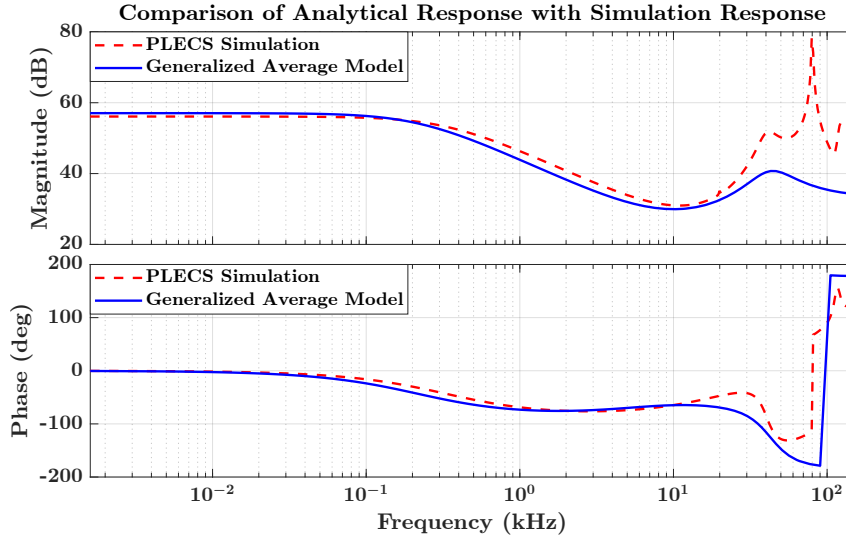


Figure 4.15: GAM validation through PLECS simulation.

Table 4.5: DAB converter specifications.

Parameter	Value
Input voltage (V_g)	756 V
Battery nominal voltage (V_o)	900 V
Switching frequency (f_s)	40 kHz
Leakage inductance (L)	2.6 μH
Parasitic resistance of inductor and transformer (r_L)	50 m Ω
Drain-source on resistance of MOSFET (R_{ds-on})	35 m Ω
Transformer turns ratio ($n_p : n_s$)	5 : 6
Output filter capacitor (C_f)	200 μF
Filter capacitor ESR (r_c)	50 m Ω

Figure 4.16 displays bode graphs of the control-to-output transfer function for various output capacitor parasitic resistances. It can be observed that at very low frequencies (less than 1 kHz), the equivalent series resistance (ESR) has little effect on the magnitude or phase of the converter's open loop response. However, at higher frequencies, spanning from around 1 kHz to the switching frequency (40 kHz) and beyond, the phase and magnitude variations are significant. This demonstrates that the capacitor ESR must be considered when designing the closed loop controller to improve system stability, particularly in the face of disturbances.

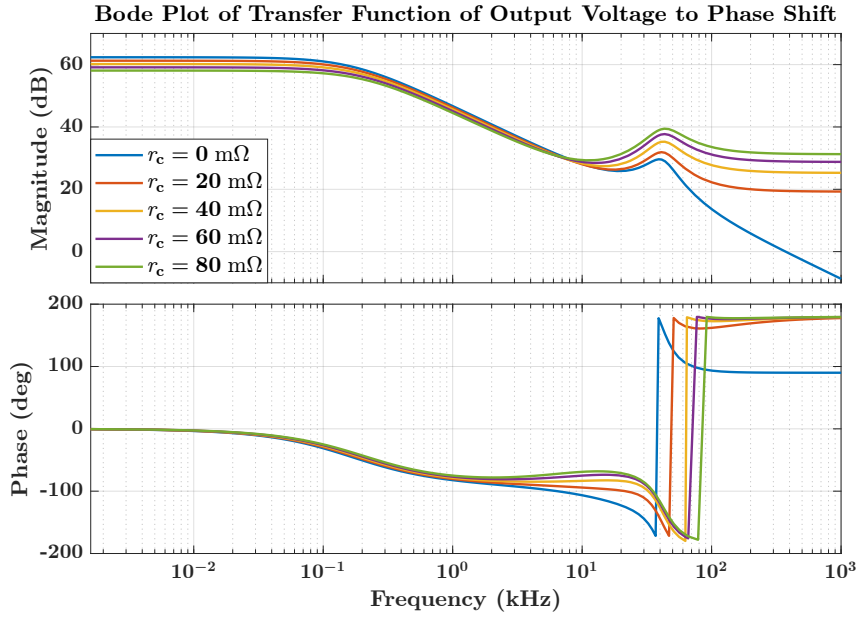


Figure 4.16: Open loop Bode plots of the control to output transfer function ($G_{V\phi}$) for different values of capacitor ESR.

Another very important transfer function is that of the output impedance of the converter which can be easily derived from Figure 4.13 and is shown to be load dependent as seen in (4.49).

$$\frac{\hat{v}_o}{\hat{i}_o}(s) = \frac{Z_b(1 + r_c Cs)}{1 + (r_c + Z_b) sC} \quad (4.49)$$

4.4 Control Strategies for DAB Converter

4.4.1 PI Controller Design for DAB Battery Charger

4.4.1.1 Proposed Feedforward Derivation

The control system implements the CC-CV battery charging technique where battery is first charged at CC and then CV. The control system's purpose is to ensure that the battery current and voltage achieve their respective reference levels quickly and precisely, as well as a smooth transition from CC to CV charging mode. To achieve these objectives, a cascaded two-loop combined feedback plus feed-forward control strategy is developed, which greatly enhances system stability and dynamic performance. The PI-based feedback path compensates for the feedforward path's errors.

The control law of a typical PI controller is given by (4.50).

$$u = k_p(r - y) + k_i \int (r - y) dt \quad (4.50)$$

Where k_p and k_i are the control parameters to be tuned, r is the reference value, and y is the measured signal. In the frequency domain, the PI controller consists of a pole at the origin and a zero, expressed as in (4.51), where $k_a = k_i/k_p$:

$$G_{pi}(s) = k_p \frac{s + k_a}{s} \quad (4.51)$$

The proposed fast dynamic cascade control system is shown in Figure 4.17. The measured output voltage (V_o) is compared with the reference value, and the difference is applied to a PI controller that generates the reference battery current for the innermost current loop. Moreover, it is made up of two adaptive feedforward expressions (FF1 and FF2) to reduce the system sensitivity to load and input voltage disturbances.

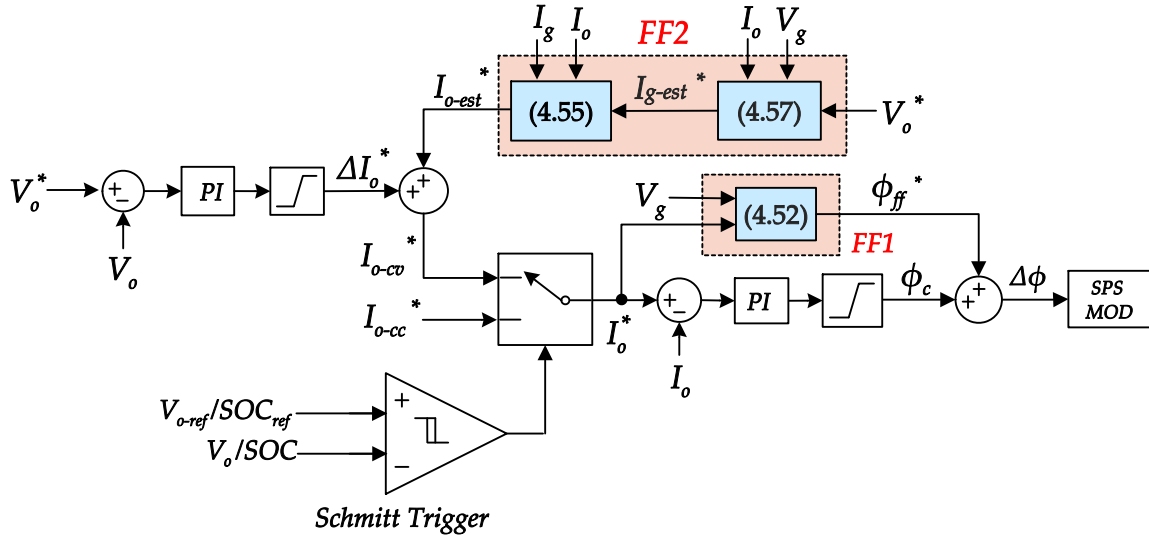


Figure 4.17: Schematic diagram of the proposed control system for DAB-based battery charging system.

FF1 is derived by rearranging the expression for the average output current in the DAB converter given in (4.10). From this expression, the desired phase shift angle (ϕ_{ff}^*) required for a particular battery current (i_o^*) to flow during charging can be expressed as follows:

$$\phi_{ff}^* = \begin{cases} \pi \left(\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2nf_s Li_o^*}{V_g}} \right), & i_o \geq 0 \\ \pi \left(-\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2nf_s Li_o^*}{V_g}} \right), & i_o < 0 \end{cases} \quad (4.52)$$

As observed, the expression in (4.52) is nonlinear. To linearize it using small-signal analysis and obtain the input-output transfer function, the derivative of ϕ with respect to i_o is required, as given in (4.53) where I_o is the steady-state value of i_o , calculated from (10).

$$K_{FF1}(s) = \frac{\hat{\phi}_{ff}(s)}{\hat{i}_o(s)} = \frac{d\phi_{ff}}{di_o} = \begin{cases} -\frac{\pi n f_s L}{V_g} \left(\frac{1}{4} - \frac{2n f_s L I_o}{V_g} \right)^{-1/2}, & i_o \geq 0 \\ \frac{\pi n f_s L}{V_g} \left(\frac{1}{4} + \frac{2n f_s L I_o}{V_g} \right)^{-1/2}, & i_o < 0 \end{cases} \quad (4.53)$$

Due to system non-idealities, a compensation phase shift ϕ_c is generated from the output of the inner current loop PI controller. Thus, the effective phase shift required for a dynamically performant inner current loop during both CC and CV charging modes is:

$$\Delta\phi = \phi_c + \phi_{ff}^* \quad (4.54)$$

During transients, the input-output power balance is disturbed, and since the voltage controller is slow, there is a delay in restoring this balance. These transients can be minimized, ensuring a seamless transition from CC to CV charging modes, if the ratio of the desired average battery current to its instantaneous current equals the ratio of the desired average input current to its instantaneous current:

$$\frac{i_{g_est}^*}{i_g} = \frac{i_{o_est}^*}{i_o} \implies i_{o_est}^* = \frac{i_{g_est}^*}{i_g} i_o \quad (4.55)$$

Here, $i_{o_est}^*$ is added to Δi_o^* , the output of the external voltage loop PI controller. The effective battery reference current for CV mode charging is thus given by:

$$i_{o_CV}^* = \Delta i_o^* + i_{o_est}^* \quad (4.56)$$

The desired input current ($i_{g_est}^*$) can be derived from the power balance between the input and output ports of the converter:

$$i_{g_est}^* = \frac{i_o}{v_g} v_o^* \quad (4.57)$$

Substituting (4.57) into (4.55), the feedforward output current of the converter is derived as:

$$i_{off2} = i_{o_est}^* = \frac{v_o^*}{i_g v_g} i_o^2 \quad (4.58)$$

Equation (4.58) is nonlinear and varies with the operating condition. Linearizing it around the operating point gives the transfer function:

$$K_{FF2}(s) = \frac{\hat{i}_{off2}(s)}{\hat{i}_o(s)} = \frac{2V_o^* I_o}{I_g V_g} \quad (4.59)$$

The tuning of the PI controller can be done using the transfer functions in (4.48) and (4.49). K_p should be designed to optimize system stability and anti-interference properties, while K_i is tuned for high gain to reduce tracking error. Additionally, an anti-windup scheme is necessary to prevent actuator saturation and maintain control performance. In this work, the back-calculation technique has been utilized.

4.4.1.2 Numerical Validation

To validate the theoretical analysis and control scheme proposed in Section 4.4.1.1, a battery charging system based on the DAB topology is modeled and implemented in the MATLAB/Simulink environment, following the specifications outlined in Table 4.6. The PI controllers are properly tuned using MATLAB's `SISOTOOL` and incorporated into the dual-loop control strategy shown in Figure 4.17. For the current control loop, the controller parameters are $K_{pi} = 0.003962$, $K_{ii} = 539.6244$, Phase Margin (PM) of 80° , and a Bandwidth (BW) of 10 kHz. For the voltage controller, the parameters are $K_{pv} = 0.66712$, $K_{iv} = 1.64 \times 10^5$, (PM) of 82° , and a BW of 2 kHz.

Table 4.6: DAB converter specifications.

Parameter	Value
Input voltage (V_g)	756 V
Battery nominal voltage (V_o)	900 V
Switching frequency (f_s)	100 kHz
Leakage inductance (L)	2.6 μH
Rated Power (P_o)	250 kW
Parasitic resistance of inductor and transformer (r_L)	50 m Ω
Drain-source on resistance of MOSFET (R_{ds-on})	35 m Ω
Transformer turns ratio ($n_p : n_s$)	5 : 6
Output filter capacitor (C_f)	200 μF
Filter capacitor ESR (r_c)	50 m Ω

The BW of the current loop controller is chosen to be $1/10^{th}$ the converter switching frequency to permit it react quickly to changes in load, input voltage or other disturbances while avoiding interactions with the high frequency switching harmonics (switching noise) introduced by the switching action of the semiconductor devices which could potentially lead to system instability. Furthermore, the voltage loop is much slower, and its BW has been set equal to $1/5^{th}$ that of the inner current loop to avoid conflicts in the control dynamics of both loops.

Figure 4.18 depicts the results obtained using the proposed control strategy. The battery is initially charged at a CC of 270 A, and the system has no control over the output voltage until about 7 ms after the charging mode is switched to CV. In this mode, the battery is charged at a constant voltage of 904 V. As can be seen, the battery current is also under control during this final stage, with a value of 236 A. Also noticeable is how smoothly and quickly the transition from CC to CV occurs in the presence of the proposed feedforward strategy.

Figure 4.19 offers a different perspective on the results shown in Figure 4.18, providing a clearer demonstration of the impact of the proposed control strategy. As illustrated, both the voltage (top) and current (middle) transition rapidly to the CV stage within 0.5 ms, with minimal dips when feedforward is applied. In contrast, without feedforward, the voltage and current experience larger dips, and the transition to steady state takes longer, approximately 2.5 ms. The absence of feedforward also leads to a more severe response in the reference battery current, which momentarily drops to zero due to the controller being unprepared for the sudden change in charging mode.

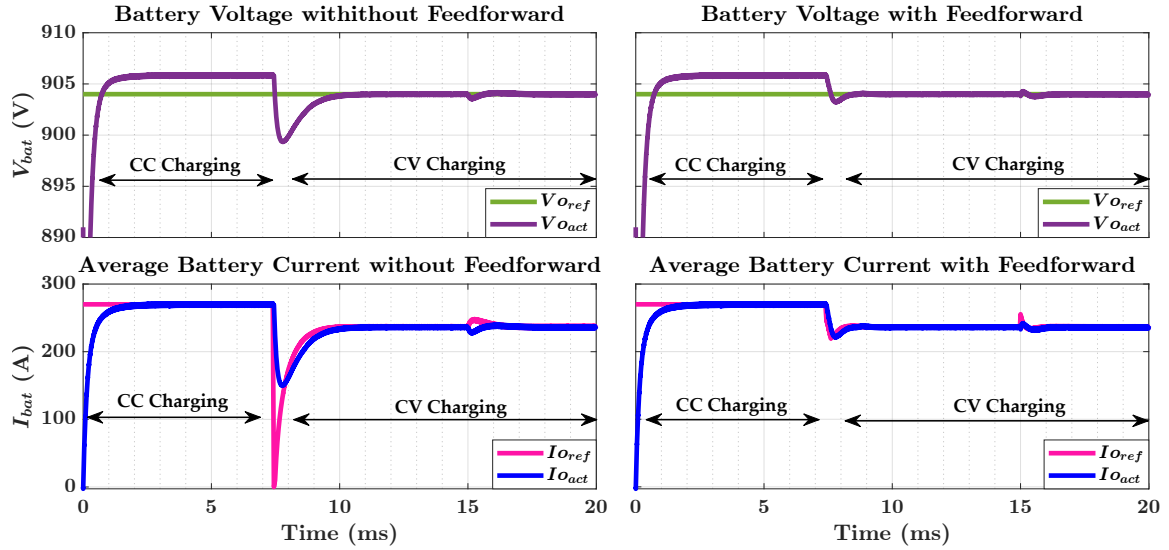


Figure 4.18: Battery voltage (**top**) and average battery current (**bottom**) without (**left**) and with (**right**) proposed feedforward.

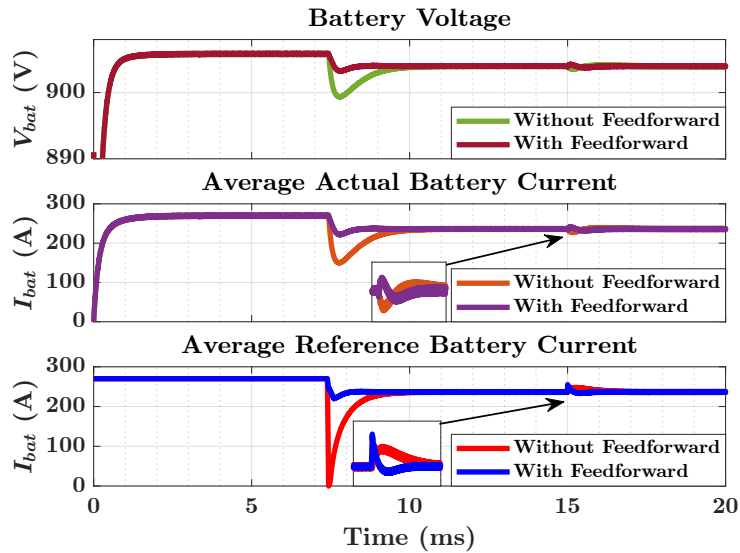


Figure 4.19: Comparison of current and voltage waveforms with and without the proposed feedforward control .

An input voltage disturbance is also investigated at $t = 15$ ms, and Figure 4.19 shows how rapidly the controller reference current reacts to this disturbance in comparison to the case where no feedforward is applied, whose controller takes longer to adjust and has large current overshoots, resulting in a lot of controller effort. The voltage loop also exhibits a similar behavior in response to input voltage disturbance.

Finally, the influence of the current loop PI controller integral gain constant on system performance is examined, with the findings presented in Figure 4.20. It is noticed that increasing the integral gain boosts the system's response speed, allowing the system to reach steady state quickly and reducing the time required for the switch from CC to CV to occur. However, this gain in response speed is accompanied with increased waveform overshoots, indicating a trade-off

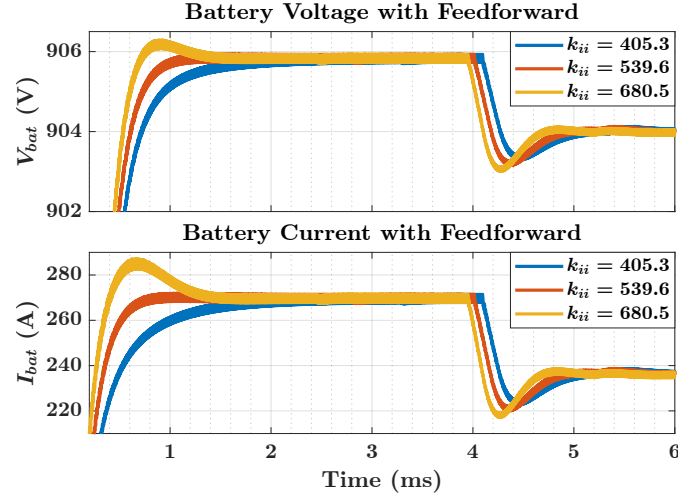


Figure 4.20: Effect of variation of current loop integral gain constant on system performance.

between faster dynamic performance and greater transient deviations. The impact of the PI controller's integral gain constant on the system's disturbance rejection ability is further shown in the bode plot of Figure 4.21 derive using the transfer function from total disturbance to the output current given in (4.60) where $G_p(s)$ is the phase shift to output plant transfer function derived from (4.48). It is again seen that increasing the integral constant leads to enhancing the disturbance rejection capability of the PI controller as the disturbance is generally at low frequency.

$$\frac{i_o(s)}{d(s)} = \frac{G_p(s)}{1 + G_{pi}(s)G_p(s)} \quad (4.60)$$

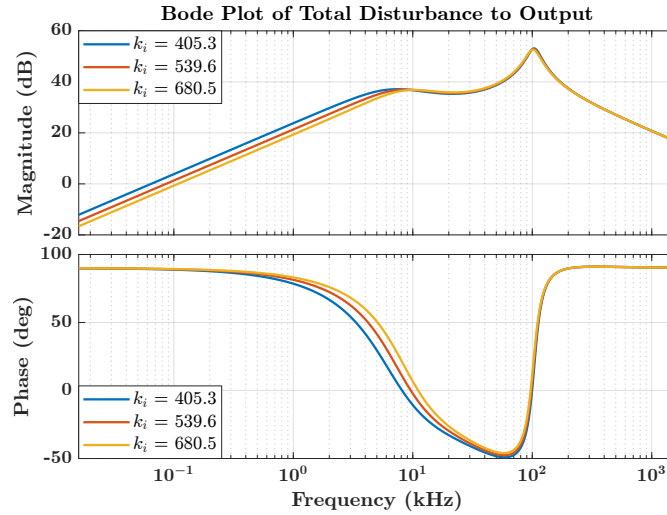


Figure 4.21: Effect of PI controller integral constant variation on disturbance rejection performance.

4.4.1.3 Impact of Feedforward on System Stability

To analyze system stability, it is important to consider the small signal closed-loop diagram shown in Figure 4.22 from which the inner loop and outer loop forward transfer functions and hence loop gains can be determined.

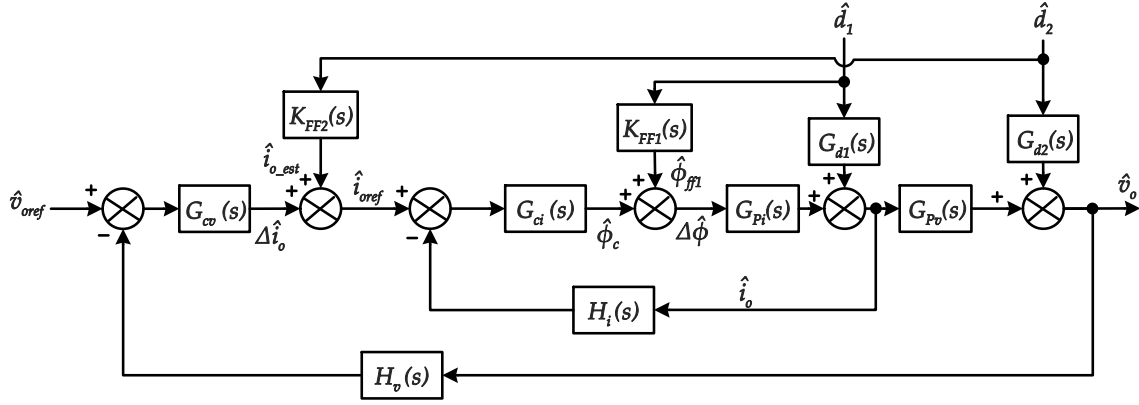


Figure 4.22: closed loop small signal model with feedforward of the converter system.

The loop gains of the inner current loop and outer voltage loop, assuming unity feedback gains, is given by (4.61).

$$\begin{cases} L_{in}(s) = (K_{FF1}(s) + G_{ci}(s))G_{pi}(s), \\ L_{out}(s) = \frac{(K_{FF2}(s) + G_{cv}(s))G_{pv}(s)(K_{FF1}(s) + G_{ci}(s))G_{pi}(s)}{1 + (K_{FF1}(s) + G_{ci}(s))G_{pi}(s)}. \end{cases} \quad (4.61)$$

Bode plots with and without feedforward of the loop gains given in (4.61) are plotted and the results are given in Figure 4.23.

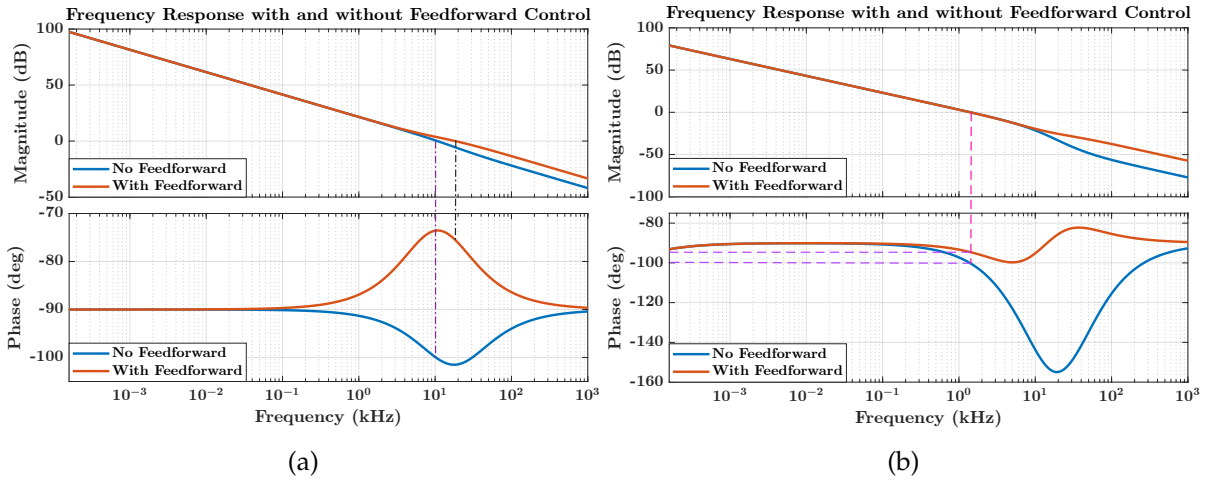


Figure 4.23: Bode plot of (a) current loop gain and (b) voltage loop gain with and without feedforward.

Figure 4.23a shows that without the feedforward, the system has a positive PM of 80° at a crossover frequency (BW) of 10 kHz as designed, hence showing that the system without the feedforward is stable. The introduction of the feedforward term increases the system gain as well as reduces the phase lag in the system at medium to high frequencies. This causes the system's PM to increase to 105° at a crossover frequency of 18 kHz, thus improving the system's stability. The increased gain, enhanced bandwidth, and reduced phase lag allow the system to respond more quickly to disturbances or setpoint changes, thus improving the dynamic performance of the system. A similar observation is noticed with the bode plot of the external voltage loop gain

shown in Figure 4.23b, which increases its PM from 80° when no feedforward is applied to 85° when feedforward is applied at the same crossover frequency of 1.4 kHz, while simultaneously reducing the phase delay, thus improving the entire system's speed of response, especially in the presence of disturbances.

4.4.2 LADRC for DAB: Design and Implementation

4.4.2.1 Basic Functional Principle of LADRC

LADRC is based on the principle of effectively estimating and compensating for both internal and external disturbances [435]. It consists of two main elements: the Linear State Error Feedback (LSEF) control law and the Linear Extended State Observer (LESO), as shown in Figure 4.24. The system has two core control loops: an inner disturbance rejection loop and an outer feedback control loop. The LESO predicts the total system disturbances, which are then mitigated by the inner loop. Together, the disturbance rejection and feedback control loops enhance the system's transient response and overall stability [436].

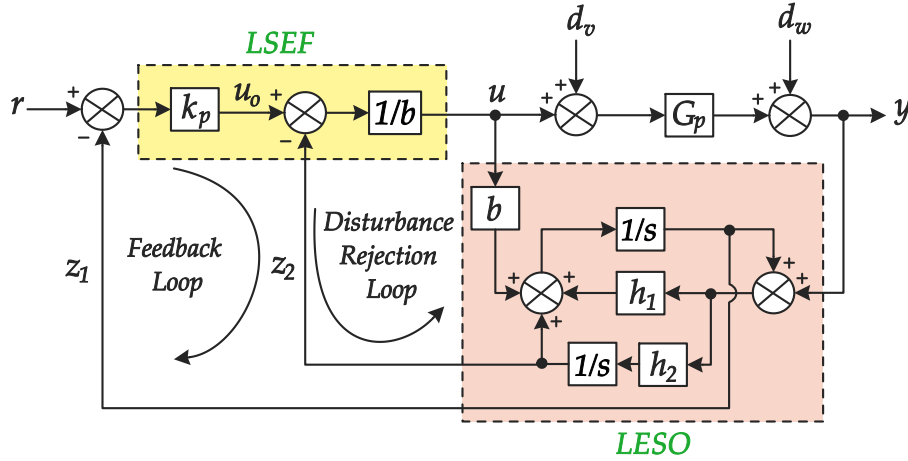


Figure 4.24: Schematic of the LADRC principle.

In Figure 4.24, r stands for the reference input signal while u_0 and u represent the controlled variables. External disturbances impacting the system are denoted by d_v and d_w . The system's plant or controlled object is shown as G_p , and the system's output signal is indicated by y . The variables z_1 and z_2 represent the estimated values of the system output and total disturbance, respectively. The controller parameter is represented by k_p and b denotes the system gain.

Any first-order SISO system can be approximated by the following expression:

$$\dot{y} = bu + f(y, u, d_v, d_w, t) \quad (4.62)$$

where f denotes the combined internal and external disturbances. The system's output signal y is assigned to the state x_1 (i.e., $y = x_1$), and an extended state x_2 is assigned to the lump disturbance f (i.e., $f = x_2$). Assuming that f is differentiable, the system dynamics can be written in state-space form as:

$$\begin{cases} \dot{x} = Ax + Bu + Ef \\ y = Cx \end{cases} \quad (4.63)$$

where

$$A = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} b \\ 0 \end{bmatrix}, \quad E = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, \quad C = \begin{bmatrix} 1 & 0 \end{bmatrix}.$$

The Luenberger-based LESO derived from the system in equation (4.63) can be expressed as follows:

$$\begin{cases} \dot{z} = Az + Bu + H(y - \hat{y}) \\ \hat{y} = Cz \end{cases} \quad (4.64)$$

where $z = \begin{bmatrix} z_1 & z_2 \end{bmatrix}^T$ is the estimate of the state variable x_1 and x_2 , and $H = \begin{bmatrix} h_1 & h_2 \end{bmatrix}^T$ is the observer gain vector.

Equation (4.64) can be rewritten in the form given in (4.65):

$$\begin{cases} \dot{z} = (A - HC)z + Bu + Hy \\ \hat{y} = Cz \end{cases} \quad (4.65)$$

From (4.65), the characteristic equation $\lambda(s)$ of the LESO can be obtained and is given by:

$$\lambda(s) = |sI - (A - HC)| = \begin{vmatrix} s + h_1 & -1 \\ h_2 & s \end{vmatrix} = s^2 + h_1s + h_2 \quad (4.66)$$

Following the bandwidth parameterization method [437], all poles of the system's characteristic equation are allocated to the observer bandwidth ω_o , leading to:

$$s^2 + h_1s + h_2 = (s + \omega_o)^2 = s^2 + 2\omega_os + \omega_o^2 \quad (4.67)$$

As a result, the observer gains can be calculated as: $h_1 = 2\omega_o$ and $h_2 = \omega_o^2$.

Furthermore, the estimated variables are used to execute the control law as indicated in Figure 4.24. This includes the disturbance rejection and error feedback control laws, given by [438]:

$$\begin{cases} u_o = k_p(r - z_1) \\ u = \frac{u_o - z_2}{b} = \frac{k_p(r - z_1) - z_2}{b} = K_p(R - \hat{z}) \end{cases} \quad (4.68)$$

where $R = \begin{bmatrix} r \\ 0 \end{bmatrix}$ and $K_p = \begin{bmatrix} k_p & 1 \end{bmatrix} / b$.

If the observer's state variable z_2 effectively tracks the total disturbance f of the system, then the system in (4.62) can be simplified to:

$$\dot{y} = bu + x_2 = (u_o - z_2) + x_2 \approx u_o \quad (4.69)$$

Using (4.68) and (4.69), and considering that $\hat{y} \approx y$, when the disturbance is compensated, the transfer function of the closed-loop control is:

$$G_{ry}(s) = \frac{y(s)}{r(s)} = \frac{k_p}{k_p + s} \quad (4.70)$$

By applying the bandwidth parameterization approach once more, the controller bandwidth ω_c is allocated to the poles of the transfer function $G_{ry}(s)$, leading to the following:

$$s + k_p = s + \omega_c \quad \Rightarrow \quad k_p = \omega_c \quad (4.71)$$

Therefore, the design of LADRC becomes more straightforward, focusing on defining the observer and controller bandwidths, which greatly simplifies the parameter tuning and design process. The controller bandwidth should be less than the observer bandwidth, typically $\omega_o = 3 \sim 10\omega_c$.

4.4.2.2 Frequency Domain Tracking and Stability Analysis of LESO

From (4.64), the observer transfer functions can be derived as in (4.72) after some simplifications.

$$\begin{cases} z_1(s) = \frac{h_2 + sh_1}{s^2 + sh_1 + h_2}y(s) + \frac{bs}{s^2 + sh_1 + h_2}u(s) \\ z_2(s) = \frac{h_2s}{s^2 + sh_1 + h_2}y(s) - \frac{h_2b}{s^2 + sh_1 + h_2}u(s) \end{cases} \quad (4.72)$$

Then from (4.72), the tracking errors due to the observation can be derived as in (4.73):

$$\begin{cases} e_1(s) = x_1(s) - z_1(s) = \frac{s^2}{s^2 + sh_1 + h_2}y(s) - \frac{bs}{s^2 + sh_1 + h_2}u(s) \\ e_2(s) = x_2(s) - z_2(s) = \frac{s(s^2 + h_1s)}{s^2 + sh_1 + h_2}y(s) - \frac{b(s^2 + sh_1)}{s^2 + sh_1 + h_2}u(s) \end{cases} \quad (4.73)$$

Assuming u and y are step signals, then $u(s) = \frac{K}{s}$ and $y(s) = \frac{K}{s}$, where K is the amplitude of the Bode signals. According to the final value theorem, the steady-state error is obtained as in (4.74) and it shows that the LESO has good convergence and estimation ability.

$$\begin{cases} e_{1ss} = \lim_{s \rightarrow 0} se_1(s) = 0 \\ e_{2ss} = \lim_{s \rightarrow 0} se_2(s) = 0 \end{cases} \quad (4.74)$$

To examine the system stability, it is helpful to go back to re-simplify (4.64) with the help of the control law given in (4.68). The expression given in (4.75) is obtained after this process:

$$\begin{cases} z_1(s) = \frac{h_1}{s + h_1 + k_p}y(s) + \frac{k_p}{s + h_1 + k_p}r(s) \\ z_2(s) = \frac{h_2(s + k_p)}{s(s + h_1 + k_p)}y(s) - \frac{k_ph_2}{s(s + h_1 + k_p)}r(s) \end{cases} \quad (4.75)$$

By inserting the expressions in (4.75) into the ADRC control law given by (4.68), a new control law is derived as given in (4.76):

$$u(s) = \frac{k_p(s^2 + sh_1 + h_2)}{b(s + h_1 + k_p)s}r(s) - \frac{k_p(h_1s + h_2) + h_2s}{b(s + h_1 + k_p)s}y(s) \quad (4.76)$$

Finally, by substituting (4.76) into (4.62), the s-domain control output is obtained as:

$$\begin{aligned} y(s) &= \frac{k_p}{s + k_p}r(s) + \frac{s(s + h_1 + k_p)}{(s + k_p)(s^2 + h_1s + h_2)}f(s) \\ &= G_{ry}(s)r(s) + G_{fy}(s)f(s) \end{aligned} \quad (4.77)$$

Noticeable from equation (4.77) is the fact that the system's output is made up of two parts: the reference tracking term and the total disturbance rejection term. Thus, the stability of the

closed loop control depends on the controller BW (defined by K_p) and the ESO BW (defined by h_1 and h_2). Moreover, if the disturbance term $f(s)$ is ignored, then the output simplifies to the expression given in (4.70) and in such a case, the tracking performance depends only on the controller BW. Figure 4.25 demonstrates that as the controller BW increases, the system stability margin increases and thus the speed of tracking increases. Moreover, high pass filtering is also enhanced due to the increase in gains at high frequencies. Regarding the disturbance rejection term, equation (4.77) shows that it depends on both the controller and observer BW. The bode plots in Figure 4.26 show that a better disturbance rejection performance is achieved as either the controller BW or the observer BW increases due to the rightward movement of the system's characteristic curve as BW increases. Furthermore, the observer's BW shouldn't be too large, since the LESO's noise sensitivity increases as its BW increases. Therefore, the design procedure involves a compromise between the noise immunity and disturbance rejection capabilities [439,440].

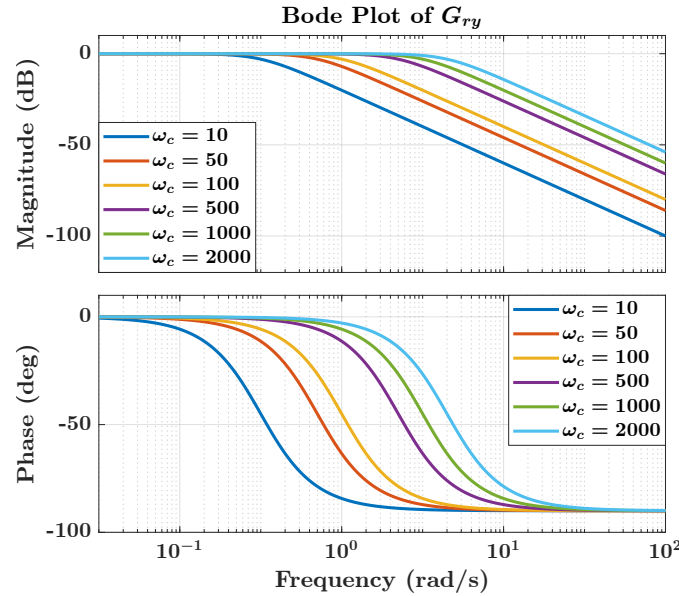


Figure 4.25: Bode diagram of $G_{ry}(s)$ when control BW (ω_c) varies.

4.4.2.3 Relationship Between LADRC and PI Control

It is important to consider how LADRC compares with a typical PI controller. The control law of a PI controller is defined by (4.50). The expression given in (4.50) can be readily rewritten in the form presented in (4.78).

$$u = \frac{k_{p2}(r - y) + k_{i2} \int (r - y) dt}{b_o} \quad (4.78)$$

where $k_{p2} = b_o k_{p1}$ and $k_{i2} = b_o k_{i1}$, with b_o being a positive constant. A comparison of (4.78) with the LADRC control law in (4.68) shows that the PI controller estimates the disturbance through its integral action as expressed in (4.79), where z_2 represents the disturbance estimated by the PI controller.

$$z_2 = -k_{i2} \int (r - y) dt \quad (4.79)$$

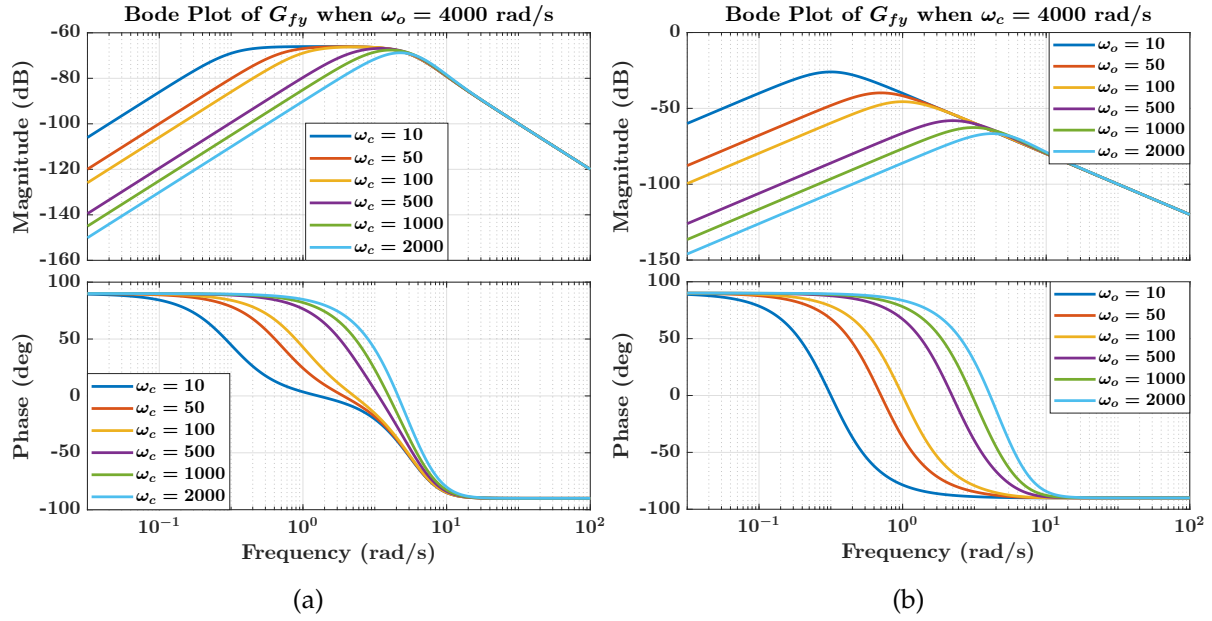


Figure 4.26: Bode diagram of $G_{fy}(s)$ when (a) control BW varies (b) observer BW varies.

If $k_p = k_{p2}$, then it is seen that the primary difference between the LADRC and PI control is the method used to estimate the total disturbance. LADRC employs an ESO (Extended State Observer) whereas a PI controller relies on the integral action of the error in the controlled variable.

4.4.2.4 LADR-based DAB Control System Design

The LADR-based control system proposed for EV battery charging is shown in Figure 4.27. It consists of an external LADRC voltage loop that produces the battery current setpoint for the LADRC battery current internal loop. This loop in turn produces the necessary phase shift to input to the SPS modulator, which controls power flow. Moreover, a novel feedforward loop (FF2) is added to the output of the external voltage loop, as explained in the following subsections. Finally, an internal feedforward expression (FF1) is included to enhance the dynamic response of the DAB converter. The FF1 expression is gotten from (4.52). The DAB converter control system design requirements are shown in Table 4.6.

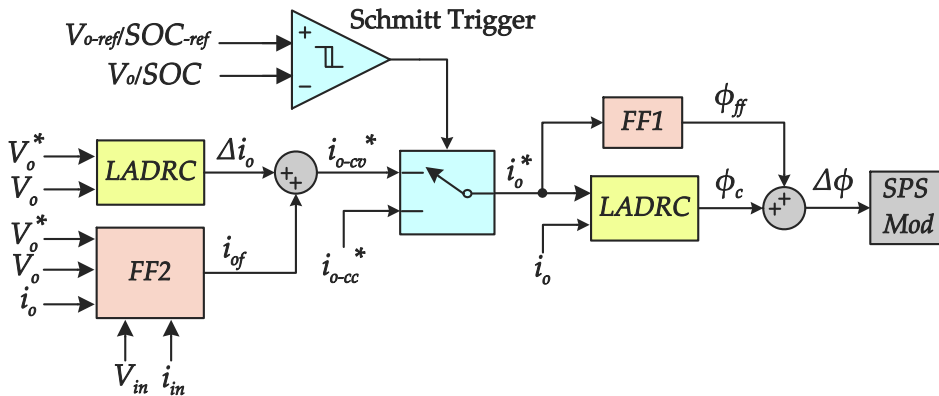


Figure 4.27: Proposed two-loop LADR-based battery charging control system.

A. LADRC-based Output Current Loop Control

This loop regulates the output current, thereby controlling the battery average current, and produces the necessary phase shift angle to control power flow. The output current control using LADRC begins with the dynamic equation of the inductor current derivative using the DAB equivalent circuit shown in Figure 4.13 and is given by (4.33). However, to simplify the analysis, the output capacitor ESR is considered small enough to be neglected. In this case, $v_o \approx v_c$, and (4.80) can be obtained.

$$\frac{di_L}{dt} = \frac{v_{in}S_1}{L} - \frac{i_L r_L}{L} - \frac{v_c S_2}{nL} \quad (4.80)$$

By substituting (4.80) into the time derivative of the output current in (4.43), the following equation is obtained:

$$\frac{di_o}{dt} = \frac{v_{in}S_1S_2}{nL} - \frac{S_2i_L r_L}{nL} - \frac{S_2^2 v_c}{n^2 L} \quad (4.81)$$

Letting $u_1 = S_1S_2$ and $u_2 = S_2^2$ simplifies (4.81) to:

$$\frac{di_o}{dt} = \frac{v_{in}u_1}{nL} - \frac{S_2i_L r_L}{nL} - \frac{u_2 v_c}{n^2 L} \quad (4.82)$$

To express (4.82) in a form that makes ϕ a control variable and thereby facilitates the application of the LADRC concept, an effective approach is to use the GAM method. Applying the GAM equation (4.28) to (4.82) results in:

$$\frac{d\langle i_o \rangle_o}{dt} = \frac{\langle v_{in}u_1 \rangle_o}{nL} - \frac{r_L \langle S_2 i_L \rangle_o}{nL} - \frac{\langle u_2 v_c \rangle_o}{n^2 L} \quad (4.83)$$

The expression for $\langle i_L S_2 \rangle_o$ is given by (4.41). However, for a very small ϕ , $\sin(\phi) \approx \phi$ and $\cos(\phi) \approx 1$, then (41) becomes:

$$\langle i_L S_2 \rangle_o = -\frac{4x_1}{\pi} \phi - \frac{4x_2}{\pi} \quad (4.84)$$

Using (4.29), the harmonic terms for u_1 and u_2 can be gotten. The u_2 terms are given in (4.37), while the u_1 terms are derived below:

$$\left\{ \begin{array}{l} \langle u_1 \rangle_o = \langle S_1 S_2 \rangle_o = \langle S_1 \rangle_1 \langle S_2 \rangle_{-1} + \langle S_1 \rangle_{-1} \langle S_2 \rangle_1 + \\ \quad \langle S_1 \rangle_3 \langle S_2 \rangle_{-3} + \langle S_1 \rangle_{-3} \langle S_2 \rangle_3 + \cdots \\ = \frac{8}{\pi^2} \sum_{p=0}^{\infty} \frac{1}{(2p+1)^2} = \frac{8}{\pi^2} \left(\frac{\pi\phi - \phi^2}{4} \right) = \frac{2}{\pi^2} (\pi\phi - \phi^2) \\ \langle u_1 \rangle_1 = \langle S_1 S_2 \rangle_1 = \langle S_1 \rangle_1 \langle S_2 \rangle_0 + \langle S_1 \rangle_0 \langle S_2 \rangle_1 + \\ \quad \langle S_1 \rangle_{-1} \langle S_2 \rangle_2 + \langle S_1 \rangle_2 \langle S_2 \rangle_{-1} + \cdots \\ = 0 \end{array} \right. \quad (4.85)$$

From the results in (4.37) and (4.85), the following can then be obtained:

$$\left\{ \begin{array}{l} \langle v_{in} u_1 \rangle_o = \langle v_{in} \rangle_o \langle u_1 \rangle_o + \underbrace{\langle v_{in} \rangle_1 \langle u_1 \rangle_{-1}}_{(=0)} + \underbrace{\langle v_{in} \rangle_{-1} \langle u_1 \rangle_1}_{(=0)} \\ \quad = \frac{2v_{in}}{\pi^2} (\pi\phi - \phi^2) \\ \langle v_c u_2 \rangle_o = \langle v_c \rangle_o \langle u_2 \rangle_o + \underbrace{\langle v_c \rangle_1 \langle u_2 \rangle_{-1}}_{(=0)} + \underbrace{\langle v_c \rangle_{-1} \langle u_2 \rangle_1}_{(=0)} \\ \quad = v_c \end{array} \right. \quad (4.86)$$

Inserting (4.84) and (4.86) into (4.83) yields:

$$\frac{d\langle i_o \rangle_o}{dt} = \frac{2v_{in}}{\pi^2 nL} (\pi\phi - \phi^2) - \frac{r_L}{nL} \left(-\frac{4x_1}{\pi} \phi - \frac{4x_2}{\pi} \right) - \frac{v_c}{n^2 L} \quad (4.87)$$

(4.87) can then be rewritten in a form suitable for LADRC:

$$\frac{di_o}{dt} = \frac{2}{\pi nL} (v_{in} + x_1 r_L) \phi + f(v_c, x_2, \phi) \quad (4.88)$$

(4.88) is in the form $\dot{y} = bu + f$, which then makes it easy to apply LADRC. Hence, their tuning follows the principles explained in Section 4.4.2.1.

B. LADRC-based Battery Voltage Loop Control

This loop controls the battery voltage during the CV charging mode. To implement LADRC, the dynamic equation for the derivative of the output capacitor voltage is necessary and is given by:

$$\frac{dv_c}{dt} = \frac{i_o}{C} - \frac{i_b}{C} = \frac{i_o}{C} + f(i_b) \quad (4.89)$$

Since (4.89) is already in the form $\dot{y} = bu + f$, v_c can then be directly controlled to generate the reference output current i_o according to the LADRC principle outlined in Section 4.4.2.1.

4.4.2.5 Proposed Feedforward for Dynamic Performance Enhancement

The transition from CC to CV charging presents a significant challenge for the system, often resulting in voltage and current spikes that impair performance. To mitigate this issue, feedforward compensation (FF2 block) is commonly implemented at the output of the external voltage loop controller, generating a feedforward current (I_{of}). This approach facilitates a smoother transition from CC to CV charging, thereby enhancing the dynamic response and efficiency of the system. The most widely used methods for calculating the feedforward expression [441] relies on balancing the total equivalent load conductance at each time step:

$$G_{Load}^* = G_{Load} \implies \left\{ \begin{array}{l} G_{Load}^* = \frac{i_{of}^*}{V_o^*}, \\ G_{Load} = \frac{i_o}{V_o}, \end{array} \right. \implies i_{of}^* = \left(\frac{V_o^*}{V_o} \right) i_o. \quad (4.90)$$

Although the LADRC with its ESO is effective at managing disturbances, the non-linear characteristic of DAB converters and battery systems pose challenges for the LADRC controller.

This non-linearity can result in system instability and difficulty achieving a stable operating state during charging. Consequently, the feedforward expression in (4.90) cannot be directly utilized in this scenario. To overcome this challenge, three new methods for computing the feedforward terms are proposed, which are described next.

A. Approach 1

This method is based on the load balance equation given in (80). Expression (90) is refined by introducing a convergence factor, α , which determines the system's ability to eliminate disturbances. The modified expression is given in (4.91):

$$i_{of1}^* = \left(\frac{V_o^*}{V_o} \right)^\alpha i_o \quad (4.91)$$

Even though (4.91) facilitates the converter's smooth transition from CC to CV and eliminates disturbances almost instantly, it necessitates very large convergence factor values to achieve, which may pose problems for the controller.

B. Approach 2

This strategy is a variation of (4.91) formulated to address the issue of requiring very large convergence factors. The revised expression incorporates a new fractional term that calculates the ratio between a specified input current reference and its instantaneous value. This new expression is given in (4.92).

$$i_{of2}^* = \left[\left(\frac{V_o^*}{V_o} \right) \left(\frac{i_{in}^*}{i_{in}} \right) \right]^\beta i_o \quad (4.92)$$

β is the convergence factor, similar to α , but its values can be significantly smaller in comparison to α . This is demonstrated in the curve shown in Figure 4.28, which illustrates how the normalized output current varies with changes in α and β for different normalized output voltage values. Considering a normalized output voltage of 1.1, the corresponding values of α and β for a per unit output current of 1.05 are found to be 0.5 and 0.25, respectively.

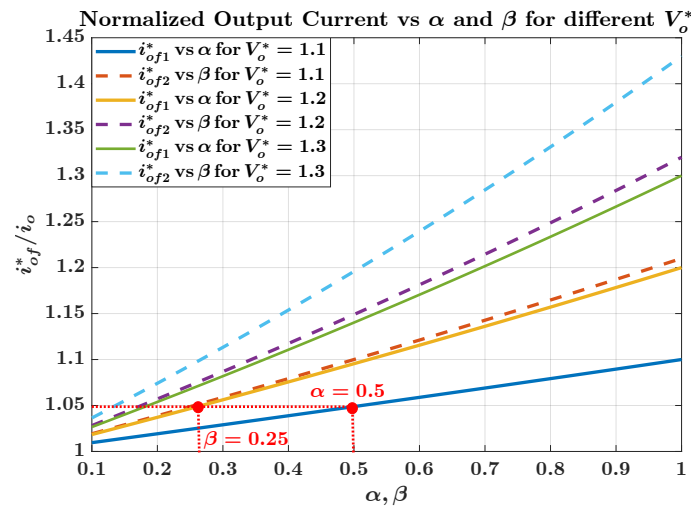


Figure 4.28: Normalized output current curve showing variations in α and β for different normalized output voltage values.

The reference input current introduced in (4.92) is calculated using a linear droop control approach. Consider $M(V_o^*, i_{in}^*)$ as a fixed point on a non-vertical line, L_1 , with a slope of k_d (droop constant). Let $N(V_o, i_{in})$ be an arbitrary point on L_1 as shown in Figure 4.29a. Then according to linear algebra, the slope of L_1 can be expressed as in (4.93):

$$k_d = \frac{i_{in}^* - i_{in}}{V_o^* - V_o} \implies i_{in}^* = k_d(V_o^* - V_o) + i_{in} \quad (4.93)$$

The slope k_d represents a conductance that can be regarded as either the converter's input conductance k_{d1} or the output load conductance k_{d2} . Therefore, i_{in}^* can assume two values depending on k_d and is given by:

$$i_{in}^* = \begin{cases} k_{d1}(V_o^* - V_o) + i_{in}, & \text{for } k_{d1} = \frac{i_{in}}{V_{in}} \\ k_{d2}(V_o^* - V_o) + i_{in}, & \text{for } k_{d2} = \frac{i_o}{V_o} \end{cases} \quad (4.94)$$

(4.94) can then be utilized alongside (4.92) to enhance the converter's dynamic response during its transition from CC to CV as well as in the presence of other system disturbances.

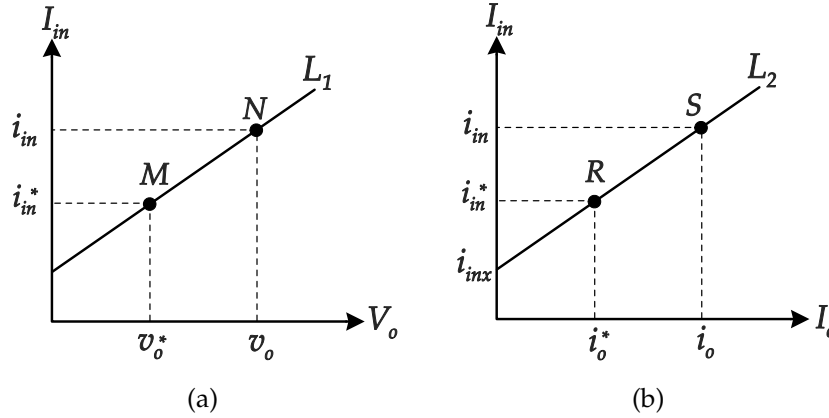


Figure 4.29: Relationship between (a) input current and output voltage; (b) input current and output current.

C. Approach 3

This approach employs a similar linear droop-based technique as before. Here, a feedforward term is obtained from the linear relationship between the input and output currents, as depicted in Figure 4.29b. If the fixed point $R(i_o^*, i_{in}^*)$ and an arbitrary point $S(i_o, i_{in})$ on the line L_2 are considered, then the droop slope m of L_2 can be expressed as:

$$m = \frac{i_{in}^* - i_{in}}{i_o^* - i_o} = \frac{V_o}{V_o^*} \quad (4.95)$$

After rearranging (4.95), the resulting feedforward expression is:

$$i_{of3}^* = \left(\frac{V_o^*}{V_o} \right) (i_{in}^* - i_{in}) + i_o \quad (4.96)$$

To derive i_{in}^* , the following expression is utilized:

$$i_{in}^* = \left(\frac{i_o}{V_{in}} \right) V_o^* \quad (4.97)$$

Furthermore, based on power balance theory, it can be concluded that:

$$i_o = \frac{V_{in} i_{in}}{V_o} \quad (4.98)$$

Now, in the presence of any disturbance, it is expected that the ratio of the desired average battery voltage to its instantaneous voltage will be equal to the ratio of the desired average input voltage to its instantaneous voltage, as expressed in (4.99):

$$\frac{V_o^*}{V_o} = \frac{V_{in}^*}{V_{in}} \implies V_{in} = \frac{V_{in}^* V_o}{V_o^*} \quad (4.99)$$

Substituting (4.99) into (4.98) results in:

$$i_o = \frac{V_{in}^* i_{in}}{V_o^*} \quad (4.100)$$

(4.97) and (4.100) can then be incorporated into (4.96) to obtain the complete robust feedforward expression in (4.101), which effectively mitigates system disturbances and improves system dynamics:

$$i_{of3}^* = \left(\frac{V_o^*}{V_o} \right) \left[\left(\frac{i_o}{V_{in}} \right) V_o^* - i_{in} \right] + \frac{V_{in}^* i_{in}}{V_o^*} \quad (4.101)$$

4.4.2.6 Numerical Validation

To verify the various SPS-based DAB LADR control techniques proposed in the previous section, MATLAB Simulink is employed. The parameters for the two loop controllers, along with the feedforward constants are presented in Table 4.7.

Table 4.7: Controller parameters.

Description	Parameter	Value
LADRC for output current	ω_{c1}, ω_{o1}	2000 rad/s, 6000 rad/s
LADRC for output voltage	ω_{c2}, ω_{o2}	500 rad/s, 3000 rad/s
Feedforward parameters	α, β	15, 6

The battery charging process begins with a CC of 270 A, followed by a CV of 904 V. Figure 4.30 shows the effect of the proposed feedforward approaches on the battery's voltage and current response during the transition between CC and CV charging modes. In both cases, with and without the techniques, the charging profile is the same. Initially, the battery undergoes a CC charging phase (0 – 7.5 ms), during which the current rises to the desired value of 270 A while the voltage remains uncontrolled. At $t = 7.5$ ms, the charging mode changes to CV at which point the control system starts to regulate the battery voltage to the target value of 904 V.

Without the suggested feedforward approaches, a significant issue arises during the CC to CV transition. The plot shows a noticeable dip in both the battery current and voltage, lasting approximately 4 ms, which can negatively affect battery health and system stability by introducing abrupt changes during this critical phase. In contrast, the plot with the droop-based feedforward technique implemented (using approach 3) demonstrates a much smoother and

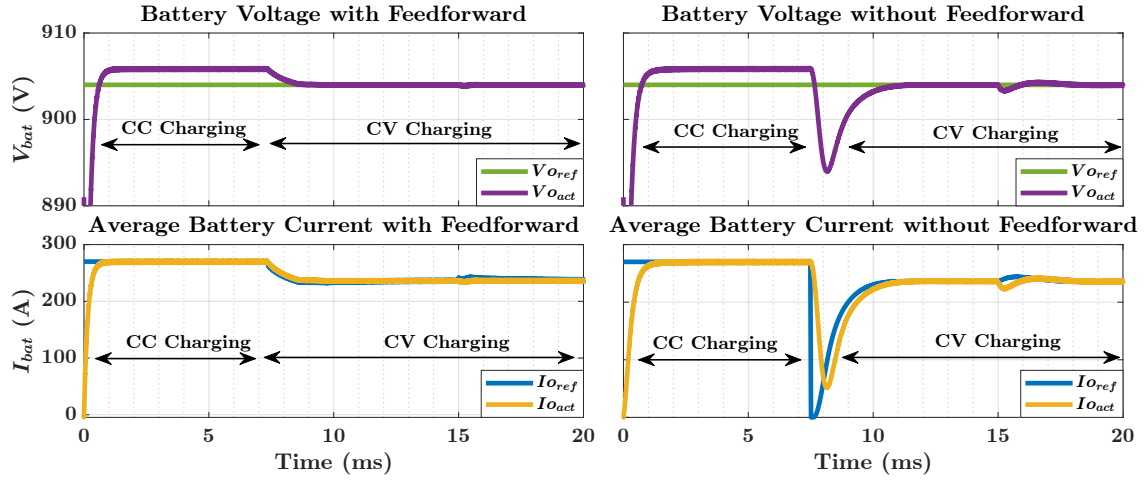


Figure 4.30: Battery voltage (**top**) and average battery current (**bottom**) with (**left**) and without (**right**) feedforward.

seamless transition, taking only about 1.5 ms, considerably faster than the case without the technique. This smoother transition not only reduces stress on system components but also potentially improves battery charging efficiency by preventing unnecessary fluctuations.

In Figure 4.30, there is also an input voltage variation which occurs at $t = 15$ ms, thus constituting a system disturbance. Without the feedforward approach, a slight undershoot in both the battery voltage and current is noticeable, and the controller takes around 3 ms to restore control. However, when using the proposed feedforward approach, this input disturbance is almost instantly observed and eliminated. This highlights the LARDC's robustness when combined with the proposed droop-based feedforward approaches.

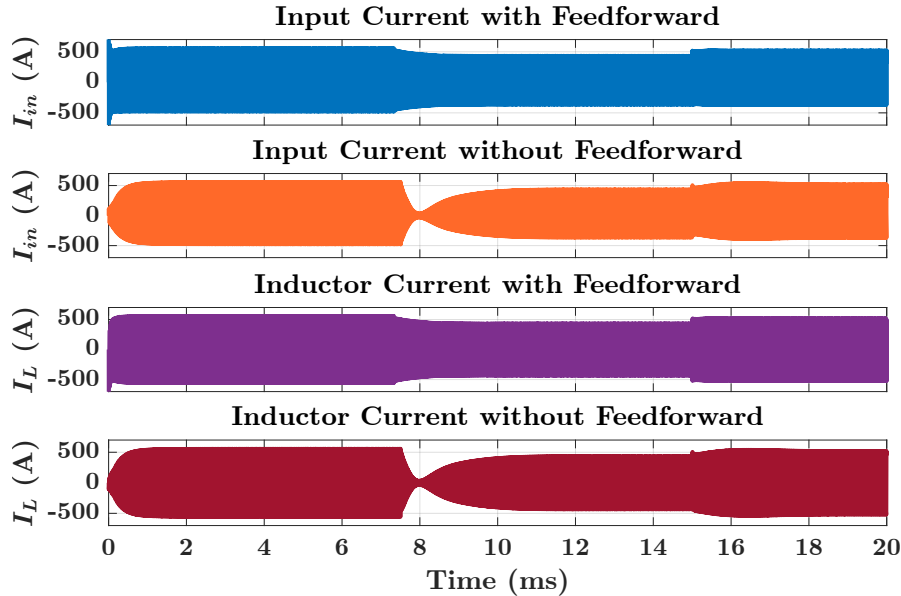


Figure 4.31: Input and inductor current transient waveforms with and without the proposed feedforward technique.

The input current and inductor current waveforms in Figure 4.31 indicate the overall influence of the CC-CV switch on the converter. In the absence of the proposed technique, a significant dip

in both the inductor and input currents is observed, as well as a gradual progression to steady state when an input voltage disturbance occurs at $t = 15$ ms. However, when the proposed feedforward technique is used in the control loop, the waveforms show a remarkably smooth transition. It is also noticeable that the controller responds almost instantaneously when the input voltage changes at $t = 15$ ms, as evidenced by the instantaneous rise in current amplitudes at this moment.

The three proposed feedforward approaches are then compared, as shown in Figure 4.32. All three approaches effectively enable a smooth and rapid transition from CC to CV modes, preventing the current and voltage dips and prolonged transients often encountered in such systems. However, it is important to note that approaches 1 and 2 offer superior dynamic stability than method 3 when utilized in conjunction with LADRC. Achieving optimal stability for all three approaches requires proper tuning of the LADRC BW parameters. Additionally, improper tuning in approach 3 may lead to oscillatory behavior, which can be mitigated by employing NLADRC.

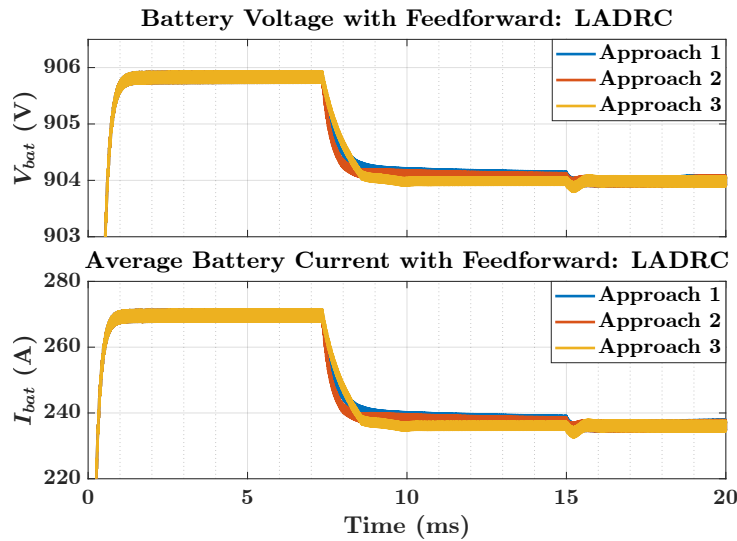


Figure 4.32: Comparing the transient performance of the proposed three approaches.

The robustness of the suggested feedforward approaches outlined in (4.91), (4.92) and (4.101) is compared with the traditional input-output port power balance approach given by (4.90). Figure 4.33 shows the results of charging the battery using approach 3, denoted by (4.101), alongside the conventional approach. In both scenarios, the battery is initially charged at CC of 270 A before being switched to CV of 904 V. Moreover, an input voltage disturbance is introduced at $t = 15$ ms during the CV stage.

The proposed approach ensures a smooth transition from CC to CV, with the voltage being immediately controlled and maintained, even in the presence of the input voltage disturbance. On the contrary, during the transition from CC to CV, the traditional approach fails to effectively control the voltage to its target value, despite the absence of the voltage and current dips shown in Figure 4.30 due to the lack of feedforward compensation. However, after the input voltage changes at $t = 15$ ms, the conventional approach eventually regains control of the voltage. This indicates that the conventional approach results in DAB converter stability at specific operating points, whereas the proposed approach ensures converter stability at all operating points within

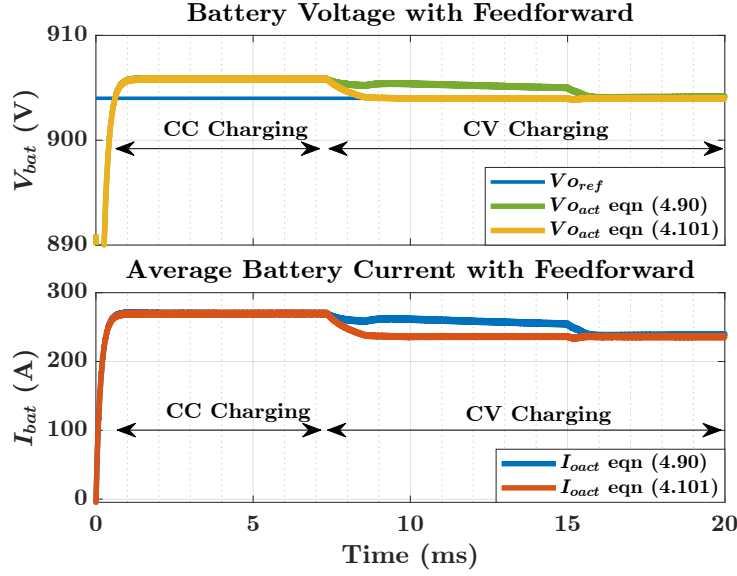


Figure 4.33: Comparing the conventional feedforward approach with the proposed approaches.

the battery limits, allowing it to deal with the converter's highly non-linear nature. A similar behavior is observed with the battery current.

4.4.3 NLADRC for DAB: Design and Implementation

Figure 4.34 shows the structure of a NLADRC. It is made up of three main components: a Tracking Differentiator (TD), Non-Linear State Error Feedback (NLSEF) and a Non-Linear Extended State Observer (NLESO). Each of these components is explained next.

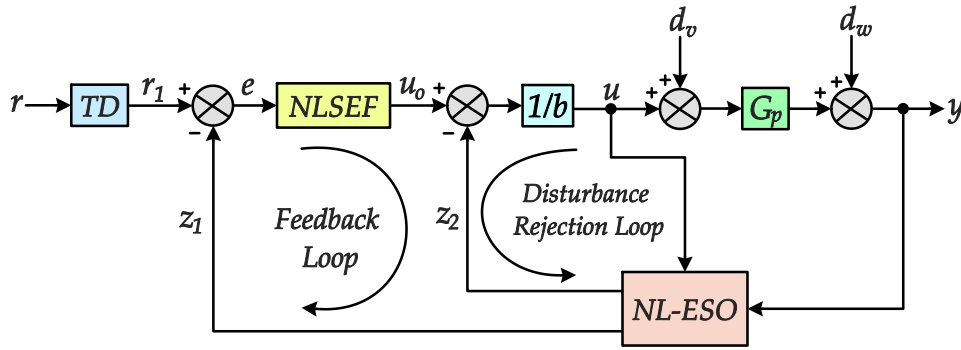


Figure 4.34: Structure of NLADRC.

4.4.3.1 Tracking Differentiator

The TD processes the reference signal, filters it and generates its derivative. This helps reduce signal noise, prevent sudden changes and avoid system overshoot by providing a gradual transition, thus leading to improved system stability. By ensuring that the reference signal is smooth and differentiable, the system's dynamic response and tracking accuracy is greatly enhanced [442].

The design of a TD relies on selecting an appropriate acceleration function with the following features. First, the acceleration function should behave as a linear function when close to the equilibrium point (origin) and nonlinear characteristics when far away from the equilibrium point. This helps to reduce the chattering effect caused by the controller switching thus enabling the rapid tracking of control signal. Secondly, the acceleration function should be as smooth and continuous as possible and the parameter tuning process should be as simple and feasible as possible [443, 444]. Based on these principles, several types of TD's have been constructed amongst which TD's based on the use of sigmoid functions are the most common due to their natural global fast convergence, simple structure as well as chattering-free [445]. Consequently, the TD proposed in this work is based on the use of sigmoid functions.

Some of the most commonly used sigmoid functions are given in Table 4.8 and each of them is plotted in Figure 4.35. As seen, these functions are odd, bounded between -1 and 1, smooth and become linear towards the equilibrium point. The narrow domain of these sigmoid functions improves the robustness of the TD against noisy signals.

Table 4.8: A list of some selected sigmoid functions

Sigmoid function	$f(x)$
Hyperbolic tangent	$\frac{e^x - e^{-x}}{e^x + e^{-x}}$
Arc tangent	$\frac{2}{\pi} \operatorname{Re} \left[\frac{i}{2} \ln \left(\frac{i+x}{i-x} \right) \right]$
Gudermannian function	$\frac{4}{\pi} \tan^{-1} \left(\tanh \left(\frac{x}{2} \right) \right)$
Logistic function	$\frac{1}{1+e^{-x}}$
Modified logistic function	$\frac{2}{1+e^{-x}} - 1$
Generalized logistic function	$\frac{1}{(1+e^{-x})^\alpha}$
Algebraic functions (sin(arctan(x)))	$\frac{x}{\sqrt{1+x^2}}$
Elliott squash function	$\frac{x}{1+ x }$

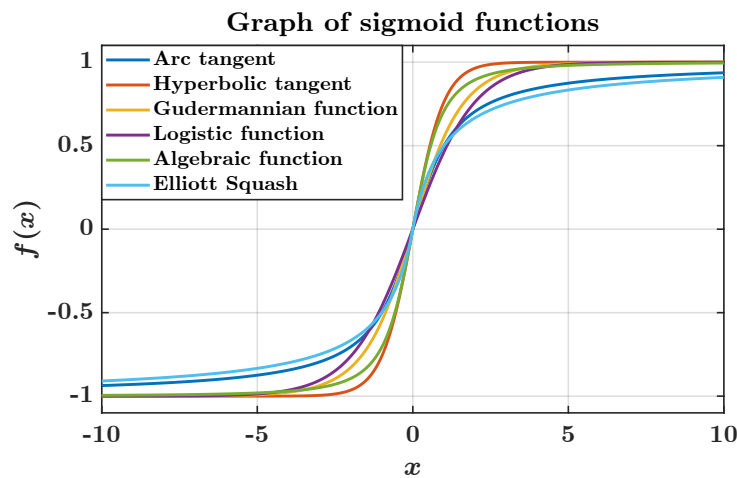


Figure 4.35: Some examples of selected sigmoid functions.

In this work, a first-order TD based on an augmented hyperbolic tangent function is proposed

and given in (4.102).

$$\dot{r}_1 = \alpha_1 \tanh[\beta_1(r - r_1)] + \alpha_2|r - r_1|^{\beta_2} \quad (4.102)$$

where r_1 is the tracked input signal and r is the reference input signal as seen in Figure 4.34. The power term $|r - r_1|^{\beta_2}$ introduces a sensitivity that varies based on the magnitude of the tracking error. This can be useful in cases where the differentiator needs to respond differently based on how far the output is from the reference. The tanh activation function provides a smooth nonlinear transition based on the tracking error. This nonlinearity helps handle abrupt changes in the reference signal while preventing excessive overshoot. α_1 and α_2 are parameters that determine how aggressively the differentiator responds to the tracking error. β_1 and β_2 are parameters that determine the shape and sensitivity of the response.

Figure 4.36 shows the impact of varying β_1 on the hyperbolic function. It is observed that changing β_1 changes the gradient of the function close to the origin. The larger β_1 is, the larger the slope of the approximate linear part of the curve near the origin, and the hyperbolic tangent function gets closer and closer to the sign function. On the other hand, the smaller the value of β_1 , the smaller and gentler would be the slope of the approximate linear part of the function.

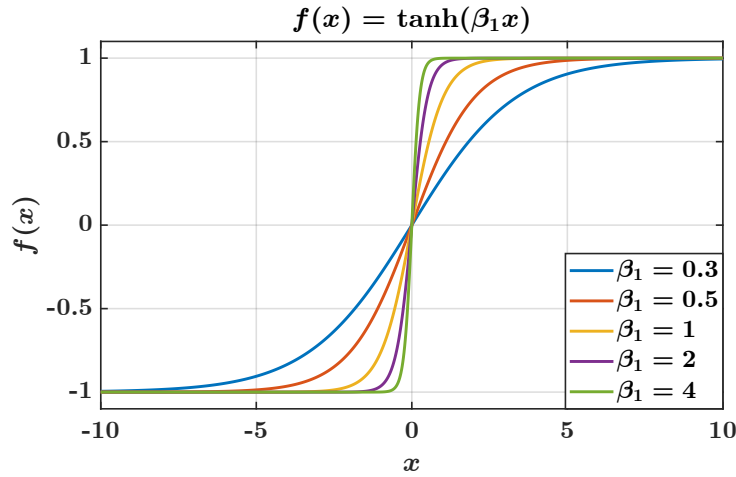


Figure 4.36: Curves of $\tanh(\beta_1 x)$ with variation in β_1 .

4.4.3.2 Non-linear Extended State Observer (NLESO)

As previously mentioned, the main function of the NLESO is to extract the signal derivatives and estimate the total system disturbances. The LESO defined by (4.64) requires adjustments of its gains to improve the observation performance. However, if the gain is too large, there will be amplification of system high-frequency noise which will lead to the peaking phenomenon during the transient period of the observer and may cause system destabilization. On the other hand, a small gain won't provide the required observation precision [446, 447]. Moreover, the traditional LESOs can't be used to reject time-varying disturbances. They can only attenuate constant or slow-varying and matched disturbances which isn't the case in real systems [448].

To deal with these issues, a NLESO is proposed in this work using the sigmoid function

whose form is given in (4.103).

$$\begin{cases} \dot{z}_1 = z_2 + bu + \delta_1 \tan^{-1} [\lambda_1(y - \hat{y})], \\ \dot{z}_2 = \delta_2 \tan^{-1} [\lambda_2(y - \hat{y})], \\ \hat{y} = z_1. \end{cases} \quad (4.103)$$

By defining the errors as $\varepsilon_1 = x_1 - z_1$ and $\varepsilon_2 = x_2 - z_2$, the error dynamics can be derived as in (4.104).

$$\begin{cases} \dot{\varepsilon}_1 = \dot{x}_1 - \dot{z}_1 = \varepsilon_2 - \delta_1 \tan^{-1} (\lambda_1 \varepsilon_1), \\ \dot{\varepsilon}_2 = \dot{x}_2 - \dot{z}_2 = \dot{f} - \delta_2 \tan^{-1} (\lambda_2 \varepsilon_1). \end{cases} \quad (4.104)$$

To determine system stability, a Lyapunov candidate function for the system is defined as:

$$V(\varepsilon_1, \varepsilon_2) = \frac{1}{2} \varepsilon_1^2 + \frac{1}{2} \varepsilon_2^2. \quad (4.105)$$

This function is always greater than zero except when $\varepsilon_1 = 0$ and $\varepsilon_2 = 0$, hence it is positive definite. The time derivative of the function is given as:

$$\dot{V} = \varepsilon_1 \dot{\varepsilon}_1 + \varepsilon_2 \dot{\varepsilon}_2. \quad (4.106)$$

Substituting (4.104) into (4.106) and simplifying gives:

$$\dot{V} = \varepsilon_1 \varepsilon_2 - \varepsilon_1 \delta_1 \tan^{-1} (\lambda_1 \varepsilon_1) + \varepsilon_2 \dot{f} - \varepsilon_2 \delta_2 \tan^{-1} (\lambda_2 \varepsilon_1). \quad (4.107)$$

For the system to be stable, $\dot{V}$ must be negative definite. Thus, the system gains must be chosen sufficiently large such that the following inequalities are satisfied:

$$\begin{cases} \delta_1 > \frac{\varepsilon_2}{\tan^{-1} (\lambda_1 \varepsilon_1)}, \\ \delta_2 > \frac{\dot{f}}{\tan^{-1} (\lambda_2 \varepsilon_1)}. \end{cases} \quad (4.108)$$

If ε_1 and ε_2 are constrained to a neighborhood around zero, then $\tan^{-1} (\lambda_1 \varepsilon_1) \approx \lambda_1 \varepsilon_1$ and $\tan^{-1} (\lambda_2 \varepsilon_1) \approx \lambda_2 \varepsilon_1$. The global stability condition can then be reformulated as in (4.109).

$$\begin{cases} \delta_1 > \frac{\varepsilon_2}{\lambda_1 \varepsilon_1}, \\ \delta_2 > \frac{\dot{f}}{\lambda_2 \varepsilon_1}. \end{cases} \quad (4.109)$$

The optimum observer gains are given by $\delta_1 = 2\omega_o$ and $\delta_2 = \omega_o^2/3$, where ω_o is the LESO bandwidth [449]. The scaling parameters λ_1 and λ_2 determine how quickly the estimation error converges to zero. By applying the proposed NLESO, the impact of the observer gains is reduced in the transient period (when the estimation error is large), thus enabling quick recovery of the system states.

4.4.3.3 Non-Linear State Error Feedback (NLSEF)

The NLSEF is a SISO module. The input signal is the error between the command signal from the TD and the output signal from the observer as observed in Figure 4.34. The nonlinear feedback controller proposed is designed according to (4.110).

$$\begin{cases} e = r_1 - z_1, \\ u_o = \delta_3 \tan^{-1}(\lambda_3 e). \end{cases} \quad (4.110)$$

From (4.110), the error dynamics, assuming that r_1 is constant, can be written as

$$\dot{e} = \dot{r}_1 - \dot{z}_1 = -(z_2 + bu + \delta_1 \tan^{-1}(\lambda_1 \epsilon_1)). \quad (4.111)$$

Using (4.110), the NLADRC control law can then be written as in (4.112)

$$u = \frac{u_o - z_2}{b} = \frac{\delta_3 \tan^{-1}(\lambda_3 e) - z_2}{b}. \quad (4.112)$$

Substituting (4.112) into (4.111) gives

$$\dot{e} = -(\delta_3 \tan^{-1}(\lambda_3 e) + \delta_1 \tan^{-1}(\lambda_1 \epsilon_1)). \quad (4.113)$$

For a small e , $\tan^{-1}(\lambda_3 e) \approx \lambda_3 e$ and $\tan^{-1}(\lambda_1 \epsilon_1) \approx \lambda_1 \epsilon_1$. Thus (4.113) becomes

$$\dot{e} = -(\delta_3 \lambda_3 e + \delta_1 \lambda_1 \epsilon_1). \quad (4.114)$$

To ensure that the controller stabilizes the system, it is necessary for $\dot{e}$ to be negative definite (i.e., $\dot{e} < 0$) as e turns to zero according to Lyapunov's stability theorem. If e and ϵ_1 are bounded, i.e., $|\epsilon_1| \leq M_1$ and $|e| \leq M_2$, then the stability condition will be given by (4.115).

$$\begin{cases} \delta_3 \lambda_3 > -\frac{\delta_1 \lambda_1 M_1}{M_2}, & \text{for } M_1 \neq M_2, \\ \delta_3 \lambda_3 > -\delta_1 \lambda_1, & \text{for } M_1 = M_2. \end{cases} \quad (4.115)$$

4.4.3.4 Numerical Simulations

To verify the performance of the suggested NLADRC strategy, the control diagram in Figure 4.27 is used, with the LADRC block replaced with the comparable NLADRC block in Figure 4.34. Furthermore, the DAB converter model described in Section 4.4.2.4 is employed again, particularly equations (4.88) and (4.89), which directly provide the b value. Furthermore, the specifications of the DAB converter employed for these verifications are the same ones stated in Table 4.6, and the parameters of the NLADRC controller are presented in Table 4.9 below.

Table 4.9: NLADRC parameters

Description	Component	Value
Voltage Loop NLADRC	TD	$\alpha_{1v} = 9 \times 10^4, \beta_{1v} = 20, \alpha_{2v} = 1, \beta_{2v} = 2$
	NLESO	$\delta_{1v} = 40\omega_{ov}, \lambda_{1v} = 0.04, \delta_{2v} = \omega_{ov}^2, \lambda_{2v} = 5, \omega_{ov} = 15 \times 10^4$
	NLSEF	$\delta_{3v} = 3.6 \times 10^3, \lambda_{3v} = 5$
Current Loop NLADRC	NLESO	$\delta_{1i} = 2\omega_{oi}, \lambda_{1i} = 5, \delta_{2i} = \omega_{oi}^2, \lambda_{2i} = 5, \omega_{oi} = 80 \times 10^4$
	NLSEF	$\delta_{3i} = 8.1 \times 10^5, \lambda_{3i} = 0.5$

As before, the battery is charged at CC of 270 A for 5 ms and then switched to CV of 904 V. Figure 4.37 shows that during the switch from CC to CV at $t = 5$ ms, the response with NLADRC is about 1 ms faster than that with LADRC and it doesn't exhibit any undershoot unlike that with LADRC which exhibits a slight undershoot. Moreover, at $t = 8.5$ ms an input voltage disturbance is emulated while at $t = 12.5$ ms, a 5% increase in the inductance is simulated. The figure shows that at both instances, the voltage and current responses with the NLADRC quickly recover to the initial control state compared to that with LADRC.

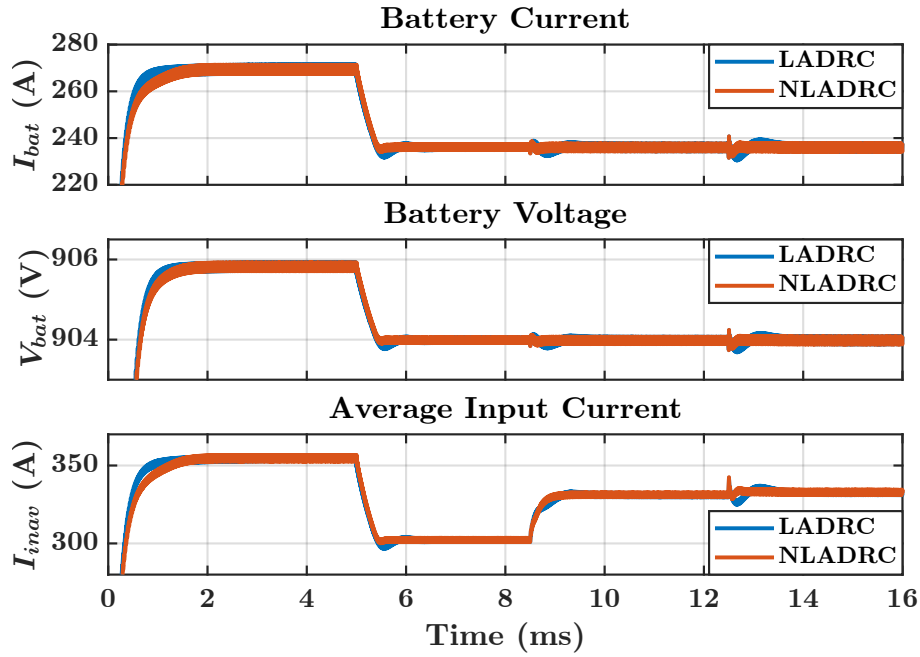


Figure 4.37: Comparison of converter battery current (**top**), battery voltage (**middle**) and average input current response (**bottom**) with LADRC and NLADRC.

4.5 Conclusion

Throughout this chapter, the detailed operation of the DAB converter under SPS modulation has been thoroughly explained and the implementation of a high power DAB-based battery charging system has also been described beginning with a detailed modelling of the battery using the second order Thevenin model together with its parameter extraction process, then examining the generalized average model of the converter and including the parasitic resistance of the output filter capacitor, which is typically ignored in literature due to complexity of analysis, but as illustrated, this resistance significantly affects the converter's dynamic behavior. A new control system combining feedforward and PI control was then proposed and both frequency response analysis and MATLAB-based simulations showed how this proposed system improves the battery's dynamic performance, especially in the presence of load and input voltage disturbances, compared to systems without the proposed control.

To overcome the challenges of PI-based controller, model independent LADRC was introduced, with its operating principles and design outlined. Building on this foundation, a detailed LADRC modeling approach was developed to enable effective control of key parameters

within the proposed cascaded two-loop control system. Furthermore, three different feedforward strategies were suggested to smooth the transition process from CC to CV during the battery charging process. Two of these techniques take advantage of the system's droop-like characteristics. Numerical simulations confirmed the effectiveness of these three approaches, demonstrating their potential to greatly improve battery charging performance. Moreover, the obtained results show that these strategies not only ensure smooth transitions but also maintain system robustness across all operating points, even under input voltage disturbances, unlike conventional methods that often focus on single loop control, add complexity or lose effectiveness under certain load conditions. In the introduction, some existing control strategies for DAB converters, including fuzzy logic, MPC, SMC, and PBC, were discussed. However, these techniques face challenges such as poor disturbance rejection, complicated design procedures, and unwanted outcomes like chattering. The suggested droop-based LADRC techniques address these constraints by providing a simpler, more robust solution that improves system stability and dynamic performance, particularly during the crucial CC to CV charging transition.

The ADRC was further extended with the introduction of NLADRC to deal with some of the well-known challenges of the LADRC like its applicability only to constant and known disturbances. An improved NLADRC exploring the benefits of sigmoid functions was proposed and numerical validations revealed that the proposed NLADRC has faster recovery time to load changes, input voltage disturbances and to parameter variations. The results acquired so far lay the foundation for more efficient and reliable battery charging systems, which are vital for broader adoption of EVs.

Chapter 5

Advanced Modulation Techniques and Vector Control for DAB Converters

5.1 Introduction

Various modulation techniques have been proposed for regulating power flow in DAB converters with the most fundamental method being Single Phase Shift (SPS) modulation as discussed in the preceding chapter. SPS generates two phase-shifted 2-level square voltages across both full bridges, but its simplicity comes at a cost; when the input and output voltages are mismatched, SPS results in high circulating reactive power (backflow) and reduced soft switching-capabilities. This leads to increased current stress, higher switching losses in the semiconductors, and greater losses in the magnetic components (inductors and transformers), ultimately lowering overall system efficiency [450]. To address these issues and improve efficiency, researchers have come up with advanced modulation strategies like Extended Phase Shift (EPS), Dual Phase Shift (DPS), and Triple Phase Shift (TPS) modulation. EPS introduces an internal phase shift in the primary full bridge, lowering current stress and circulating power, yielding improved efficiency with a three-level voltage on one side and two-level on the other. DPS, like EPS, applies equal internal phase shifts to both full bridges, producing symmetrical three-level square waves, which also enhances efficiency [451, 452]. TPS provides the greatest efficiency by enabling independent inner phase shifts within each full bridge, thus minimizing current stress and conduction losses, and maximizing the ZVS operating range [453–456]. TPS can work in 12 modes but due to operational symmetry, only modes 1 to 5 are typically explored. TPS modes 2 and 5 have demonstrated to be disadvantageous due to their lack of ZVS ability and elevated current stresses, consequently most works in literature focus on TPS mode 1, 3 and 4.

Aside from the phase shift modulation techniques described above, other modulation techniques have been proposed and employed for DAB including triangular modulation (TRM) [457–459], trapezoidal modulation (TZM) [460, 461], asymmetric duty cycle modulation (ADM), variable switching frequency modulation (VSFM) and hybrid modulation (HM).

In TRM (a boundary case between TPS mode 1 and 3), two 3-level voltages are generated across both terminals of the inductor with an arbitrary duty cycle. The resulting inductor current consists of three distinct time segments: during the first segment, the inductor current increases from zero to its peak value eventually decreasing back to zero in the second period

and maintaining this zero value in the third period. This modulation enables ZCS for the low voltage side (LVS) switches, which is desirable for minimizing switching losses, increasing switching speed and reducing EMI. However, TRM can only be applied when the transformer has a turns ratio such that $V_1 \ll \frac{V_2}{n}$ or $V_1 \gg \frac{V_2}{n}$ for reverse power flow [462]. Consequently, no power transfer occurs when $V_1 = \frac{V_2}{n}$. Unlike TPS modulation, the TRM is easier to implement and has insignificant reactive power losses [463]. While TRM is advantageous for low switching losses, it has the drawback that the condition $V_1 \ll \frac{V_2}{n}$ must be satisfied across the entire range of input and output voltages, limiting its maximum power transfer and thus restricting its use to low power applications [464]. This results in inefficient converter utilization. Moreover, the method is also prone to large peak current and RMS values. If pure ZCS is not required on the LVS, then TZM (a specialized case of TPS mode 3) can be employed since power transfer occurs even when $V_1 \approx \frac{V_2}{n}$. The most essential feature of TZM is the presence of a time interval in each half modulation period during which the current is zero, permitting ZCS in switches that are turned on under zero current condition. High converter efficiency can be achieved with TZM as the full bridge circuits operate with larger duty cycles, resulting in a lower peak and RMS currents compared to TRM [465]. ZCS is achieved for four transistors and ZVS for the remaining four, thereby leading to reduced switching losses compared to phase shift modulation and TRM. Moreover, It should be noted that TRM is a specific case of TZM [466].

To further extend the ZVS operating range and reduce RMS current, especially at light load, recent works have proposed asymmetrical duty modulations (ADM) which uses unequal duty cycles on the HV side bridge, resulting in an asymmetric waveform. Meanwhile, the duty cycles on the LV bridge are maintained at 50%, just like in SPS [467, 468]. ADM control can significantly reduce current stress and enhance the efficiency of DAB converter, especially when the input and output voltages are mismatched. Further improvements to ADM have been suggested by [469], [470] and [471] all aimed at increasing the number of ZVS switches, improving power transmission and eliminating current bias at light loads. These advancements show superior soft-switching performance at light loads compared to TPS. Variable switching frequency modulation (VSFM) has also been proposed to address the loss of ZVS during mode transitions in the traditional constant switching frequency modulation schemes described above [472]. VSFM scheme dynamically adjusts the switching frequency and phase shift(s) according to the load demand and voltage levels thus ensuring full ZVS across a wide voltage range [473]. Typically, at light load conditions, the switching frequency is lowered to reduce switching losses and enhance efficiency while at heavy load conditions, the switching frequency is raised to ensure fast power transfer [474, 475]. Despite its advantages, it could cause EMI problems if not properly controlled and has a difficult magnetic design. Finally, hybrid modulation (HM) methods which combine several different modulation techniques have been extensively discussed in literature [476–479]. HM optimizes efficiency across a broad range of power levels by applying different modulation methods in various power zones. However, HM leads to a complex implementation since the modulation strategy has to be changed according to the operating point.

The advanced modulation techniques discussed above have led to the development of efficiency optimization algorithms needing to adapt to a range of objectives. The four major objectives are as follows: minimizing peak and RMS inductor current; ensuring soft switching across all switches; minimizing backflow or reactive power; and minimizing overall power losses.

The challenge therefore lies in determining the optimal phase shift angles and duty cycles that achieve these objectives. However, the mathematical modeling of the DAB converter under these advanced modulation schemes is quite complex, requiring piecewise functions to account for various operating conditions and time intervals. Thus, to address these optimization problems, various complex iterative methods have been used including the Karush–Kuhn–Tucker or Lagrange multiplier method [480], Newton-Raphson’s method [481], mathematical programming methods, graphical optimization method [482], Particle Swarm Optimization [483], Ant Colony Optimization [484], genetic algorithm [485] and Deep Reinforcement Learning technique [486]. Despite their effectiveness, these methods have notable limitations, including high computational demands when implemented in DSPs, strong dependence on accurate initial guesses, and the need for a detailed understanding of the converter model.

Furthermore, present control methods for single-phase or three-phase DAB DC-DC converters typically utilize scalar control. This technique struggles to manage the reactive power flowing between the primary and secondary full bridges independently, as well as possess limited dynamic response. Vector control, an approach commonly applied in three-phase grid-connected systems, presents a promising alternative by allowing separate control of active and reactive power flows. Although vector control isn’t yet widely adopted in DAB applications, a few works have demonstrated its potential to enhance DAB converter performance offering advantages such as improved fault tolerance, faster dynamic response, higher power density, and greater efficiency [487–490]. However, accurately implementing vector control in high frequency converters pose several challenges like ensuring proper decoupling of the active and reactive currents from the measured harmonic current, as well as the need for a high-speed computational control hardware.

To address all the challenges mentioned above, this chapter presents a novel droop-based feedforward control scheme designed to enhance the efficiency of charge and discharge processes in EV storage systems. The key improvement lies in achieving a seamless transition between CC and CV charging modes in a DAB converter controlled by a DPS, thereby preventing potential disruptions during the charging process. Traditionally, such systems rely on a two-loop PI control, but a more advanced three-loop model-independent LADRC system is proposed and presented in this chapter. The standout feature of this advanced LADRC system is the addition of an extra loop that implements decoupled dq vector control of the inductor current, an uncommon feature in single-phase DAB converters. The contributions of this innovative control strategy are quite significant. First, the LADRC system which incorporates dq vector control allows for the optimal determination of both internal and external phase shift angles within the DPS modulator using the Fourier series analysis of three-level square wave bridge voltages. This optimization significantly reduces the peak inductor current, enabling the use of lower-rated switches and resulting in a more cost-efficient design. Notably, the Fourier series based fundamental component analysis (FCA) whose modelling is based on the first harmonic voltage component provides a very simple yet accurate analytical approach as the first harmonic component accounts for nearly all of the DAB converter’s active power content. Moreover, the independent control of the direct and quadrature inductor current components, facilitated by the LADRC system, results in a unity power factor, thus maximizing system efficiency and minimizing reactive or backflow power during DAB operation. In summary, this

chapter introduces a significant advancement in DAB converter control, combining smooth mode transitions, enhanced efficiency, and the capability to achieve a perfect power factor.

The remainder of this chapter is organized as follows: Section 5.2 describes the DAB converter's general functioning based on three-level voltage signals while Section 5.3 discusses the three-loop control, including the LADRC-based control design for each loop. This section also introduces the coordinate transformation method used to extract the dq components of the inductor current. Additionally, the proposed droop-based feedforward control for dynamic performance enhancement is discussed. Section 5.4 provides some numerical simulations to validate the performance of the control algorithms and finally, Section 5.5 concludes the chapter.

5.2 Unified Harmonic Analysis of DAB Converter under Three-level Modulated Phase Shift Control

5.2.1 Operational Principle of Three-level Phase Shift Modulation

At steady state, the DAB converter equivalent circuit is shown in Figure 5.1a. It is made up of two high frequency square wave voltage sources on either side of the inductor. Moreover, inductance L in Figure 5.1a is the summation of the HFT leakage inductance and an externally connected series inductor; V_p and V_s are the high frequency link (HFL) voltages of primary (FB1) and secondary (FB2) full bridges respectively with V_s being the FB2 voltage viewed from the primary side of the HFL transformer; i_L denotes the HFL inductor current. The universal waveforms resulting from three-level modulated phase-shift control are shown in Figure 5.1b, where $\hat{V}_{p1}$ and $\hat{V}_{s1}$ denote the fundamental sinusoidal components of the two voltages.

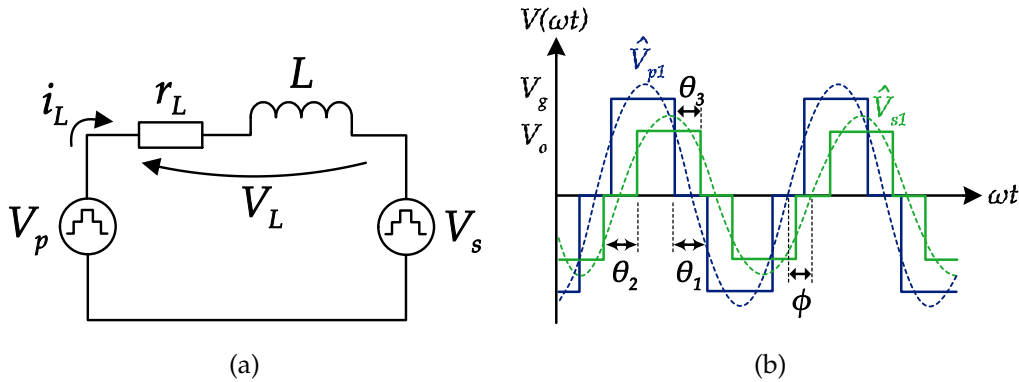


Figure 5.1: (a) DAB converter AC equivalent circuit (b) Illustrative waveforms depicting the three-level modulation technique applied to a DAB converter under unified phase-shift control.

The waveforms for unified phase-shift control consist of three phase shift angles: θ_1 , θ_2 , and θ_3 . Here, θ_1 and θ_2 represent the internal phase shifts between the parallel legs of FB1 and FB2, respectively, while θ_3 denotes the external phase shift between the square wave voltages of FB1 and FB2. The external phase shift between the fundamental components of the square wave voltages of each full bridge, ϕ , is related to the other phase angles by the equation: $\phi = \theta_3 + \left(\frac{\theta_1 - \theta_2}{2}\right)$ [491]. Consequently, unified phase shift control serves as a generic approach to expressing all of the phase shift control techniques outlined in Section 5.1. SPS occurs when

$\theta_1 = \theta_2 = 0$ and $\phi \neq 0$, EPS is realized when either $\theta_1 \neq 0, \theta_2 = 0, \phi \neq 0$ or $\theta_1 = 0, \theta_2 \neq 0, \phi \neq 0$, DPS is achieved when $\theta_1 = \theta_2 = \gamma \neq 0$ and $\phi \neq 0$, and TPS occurs when $\theta_1 \neq \theta_2 \neq 0$ and $\phi \neq 0$.

In this study, the focus is on the special case of the DPS, which allows for two operational modes: $0 < \gamma < \theta_3 < 1$ and $0 < \theta_3 < \gamma < 1$. Figure 5.2 shows the waveforms of the DAB converter for both operational modes under buck power flow. Also, Table 5.1 presents the active switches during each operating interval.

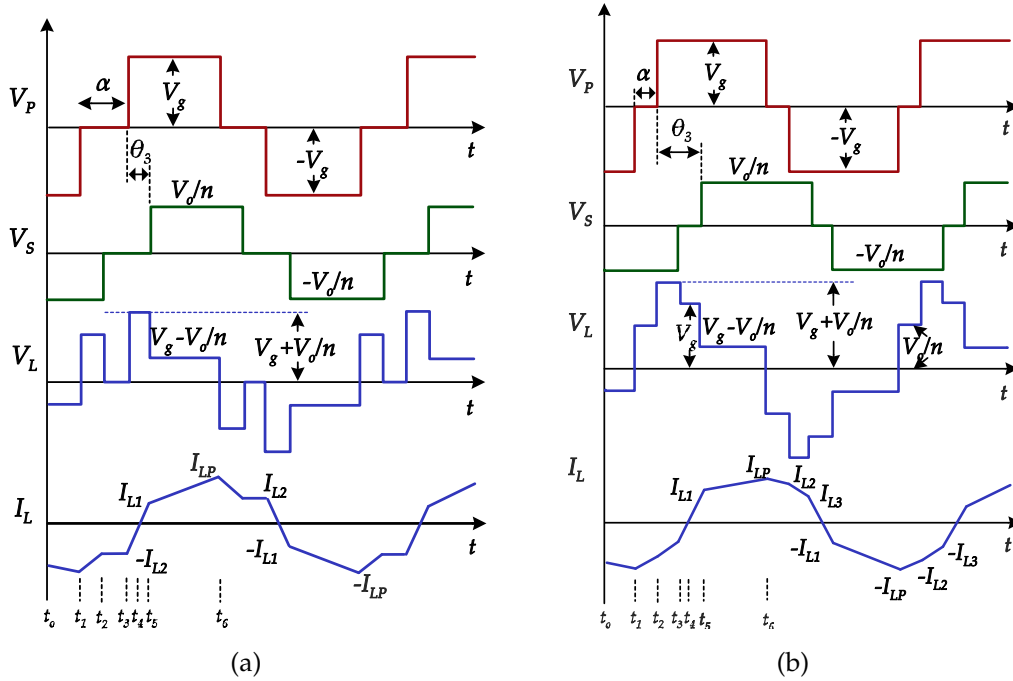


Figure 5.2: DAB waveforms under different DPS operating conditions: (a) $0 < \theta_3 < \gamma < 1$ (b) $0 < \gamma < \theta_3 < 1$.

Table 5.1: Active devices during each interval in DPS

Mode	Connecting Devices			
	$0 < \theta_3 < \gamma < 1$		$0 < \gamma < \theta_3 < 1$	
	FB1	FB2	FB1	FB2
$t_1 - t_2$	S ₃ D ₄	D _a D _d	S ₃ D ₄	D _a D _d
$t_2 - t_3$	D ₁ D ₄	D _a D _d	S ₃ D ₄	S _a D _d
$t_3 - t_4$	D ₁ D ₄	S _a D _d	D ₁ D ₄	S _a D _b
$t_4 - t_5$	S ₁ S ₄	S _a D _b	S ₁ S ₄	S _a D _b
$t_5 - t_6$	S ₁ S ₄	D _b D _c	S ₁ S ₄	D _a D _c

The power transferred during each of the modes given in figure 2 is expressed in equation (5.1).

$$P = \begin{cases} \frac{V_o V_g}{2n\pi^2 f_s L} \left[\theta_3 \left(\pi - \gamma - \frac{\theta_3}{2} \right) \right], & \text{for } 0 < \theta_3 < \gamma < 1, \\ \frac{V_o V_g}{2n\pi^2 f_s L} \left[\theta_3 (\pi - \theta_3) - \frac{\gamma^2}{2} \right], & \text{for } 0 < \gamma < \theta_3 < 1. \end{cases} \quad (5.1)$$

5.2.2 Fourier Series Based Harmonic Analysis of HFL Voltage and Current

The high frequency voltages across the transformer windings can be mathematically represented through the Fourier series expansion of three-level square wave signals as:

$$\begin{cases} V_p(t) = \sum_{m=1,3,5,\dots} \frac{4V_g}{m\pi} \cos\left(\frac{m\theta_1}{2}\right) \sin(m\omega_o t), \\ V_s(t) = \sum_{m=1,3,5,\dots} \frac{4V_o}{nm\pi} \cos\left(\frac{m\theta_2}{2}\right) \sin(m(\omega_o t - \phi)). \end{cases} \quad (5.2)$$

Where m represents the harmonic number, $\omega_o = 2\pi f_s$ with f_s being the converter's switching frequency. Power flow control can be performed by either adjusting the phase shift ϕ or altering the amplitude of the fundamental components of the two H-bridge voltages using θ_1 and θ_2 , where $0 \leq \theta_1 \leq \pi$, $0 \leq \theta_2 \leq \pi$, and $-\pi \leq \phi \leq \pi$. Since the voltages V_p and V_s are periodic functions, they can be written in phasor form with RMS values as:

$$\begin{cases} \dot{V}_p = \sum_{m=1,3,5,\dots} \frac{2\sqrt{2}V_g}{m\pi} \cos\left(\frac{m\theta_1}{2}\right), \\ \dot{V}_s = \sum_{m=1,3,5,\dots} \frac{2\sqrt{2}V_o}{m\pi} \cos\left(\frac{m\theta_2}{2}\right) [\cos(m\phi) - j\sin(m\phi)]. \end{cases} \quad (5.3)$$

From (5.3), the inductor current phasor is obtained as:

$$\begin{aligned} \dot{I}_L &= \frac{\dot{V}_p - \dot{V}_s}{jm\omega_o L} \\ &= \sum_{m=1,3,5,\dots} \frac{2\sqrt{2}}{m^2\pi\omega_o L} \left[V_o \cos\left(\frac{m\theta_2}{2}\right) \sin(m\phi) \right. \\ &\quad \left. + j \left(V_o \cos\left(\frac{m\theta_2}{2}\right) \cos(m\phi) - V_g \cos\left(\frac{m\theta_1}{2}\right) \right) \right]. \end{aligned} \quad (5.4)$$

The time domain representation of the inductor current phasor in (5.4) is given by:

$$i(t) = \sum_{m=1,3,5,\dots} \frac{4\sqrt{A^2 + B^2}}{m^2\pi\omega_o L} \sin[m\omega_o t + \tan^{-1}(A/B)]. \quad (5.5)$$

Where:

$$\begin{cases} A = V_o \cos\left(\frac{m\theta_2}{2}\right) \cos(m\phi) - V_g \cos\left(\frac{m\theta_1}{2}\right), \\ B = V_o \cos\left(\frac{m\theta_2}{2}\right) \sin(m\phi). \end{cases} \quad (5.6)$$

Using (5.3) and (5.4), the complex apparent power at the output of FB1 can be obtained as:

$$S = \sum_{m=1,3,5,\dots} \dot{V}_p \dot{I}_L^* = P + jQ. \quad (5.7)$$

Where P and Q respectively denote the active and reactive power flow in the converter and are given as:

$$\left\{ \begin{aligned} P &= \sum_{m=1,3,5,\dots} P_m = \sum_{m=1,3,5,\dots} \frac{8V_g V_o}{nm^3 \pi^2 \omega_o L} \cos\left(\frac{m\theta_1}{2}\right) \cos\left(\frac{m\theta_2}{2}\right) \sin(m\phi), \\ Q &= \sum_{m=1,3,5,\dots} Q_m \\ &= \sum_{m=1,3,5,\dots} \frac{8V_g}{m^3 \pi^2 \omega_o L} \left[V_g \cos^2\left(\frac{m\theta_1}{2}\right) \right. \\ &\quad \left. - \frac{V_o}{n} \cos\left(\frac{m\theta_1}{2}\right) \cos\left(\frac{m\theta_2}{2}\right) \cos(m\phi) \right]. \end{aligned} \right. \quad (5.8)$$

Unlike the active power, the reactive power doesn't only occur between voltage and current of the same harmonics but also due to a difference in harmonic number [492,493]. The mismatch reactive power is given by:

$$\begin{aligned} Q_{m_1 \neq m_2} &= V_{p-m_1} I_{L-m_2} \\ &= \sum_{m_2=1,3,5,\dots} \frac{8V_g \sqrt{A(m_2)^2 + B(m_2)^2}}{m_1 m_2^2 \pi^2 \omega_o L} \cos\left(\frac{m_1 \theta_1}{2}\right) \end{aligned} \quad (5.9)$$

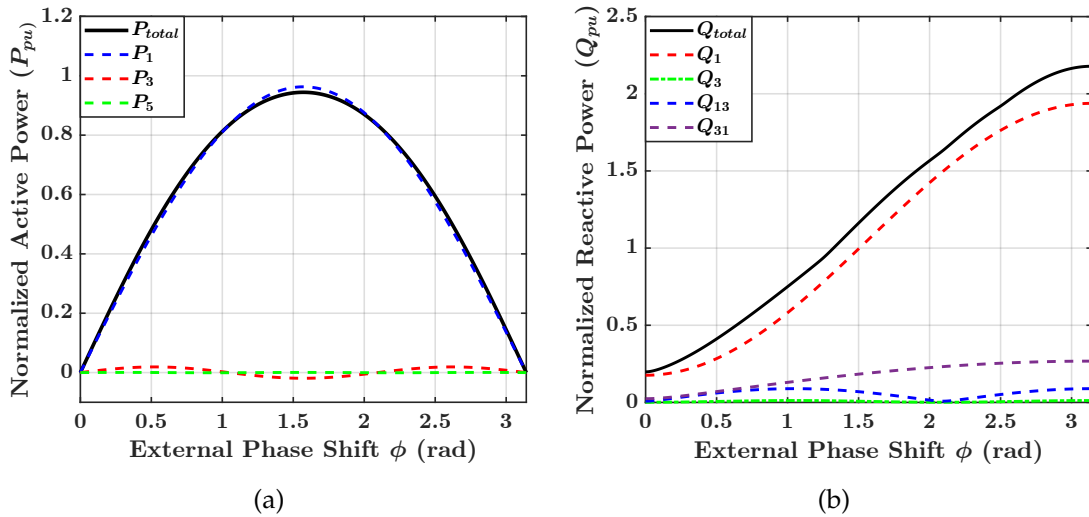


Figure 5.3: Normalized active power harmonic contributions as a function of external phase shift (a) Variation of normalized reactive power with external phase shift.

Normalized plots of active power and reactive power, as described by equations (5.8) and (5.9), can be used to observe how each harmonic component, together with the total power, varies with the external phase shift. Figure 5.3 illustrates this for the DPS case, with power normalized by $P_N = \frac{V_g V_o}{8f_s L}$. Figure 5.3a shows the normalized active power variation where P_{total} is the overall normalized active power, and P_1 , P_3 , and P_5 are respectively the 1st harmonic (fundamental), 3rd harmonic, and 5th harmonic components. It can be observed that the active power is symmetrical around $\phi = \pi/2 = 1.6$ rad, with the maximum occurring at this point, which is less than one for DPS. Moreover, the fundamental component is the one largely responsible for active power transfer as higher-order harmonic contributions are almost negligible.

Figure 5.3b shows the variation of normalized reactive power with external phase shift under DPS modulation, where all harmonic components are again normalized by $P_N = \frac{V_g V_o}{8f_s L}$. Q_{total} is

the overall normalized reactive power, while Q_1 and Q_3 are respectively the fundamental and third harmonic components of the unified reactive power. Q_{13} is the mismatch or cross-term reactive power generated by the fundamental voltage and the 3rd harmonic current, while Q_{31} is the mismatch reactive power due to the 3rd harmonic voltage and fundamental current. It is observable that reactive power contributions from the fundamental current (Q_1 , Q_{31} , Q_{51} , etc.) increase steadily as the external phase shift angle increases within the range $[0, \pi]$. Moreover, the fundamental reactive power component exhibits the highest amplitude, making it the dominant factor in representing the total reactive power.

Reactive power circulation increases the apparent power and RMS current, which subsequently raises power losses and the capacity demands of the DAB converter. This is a key factor behind the high circulating currents and reduced efficiency in the DAB converter. From (5.8) and (5.9), the magnitude of the apparent power is given by

$$S = \sqrt{\sum_{m=1,3,5,\dots} P_m^2 + \sum_{m=1,3,5,\dots} Q_m^2 + \sum_{m=1,3,5,\dots} Q_{m_1 \neq m_2}^2}. \quad (5.10)$$

Finally, the global HFL power factor, λ , can be computed from (5.8) and (5.10) and is given by

$$\lambda = \frac{P}{S}. \quad (5.11)$$

Using equation (5.11), power factor curves for varying internal and external phase shift angles can be derived as shown in Figure 5.4. Figure 5.4a is a 3D surface plot showing how the power factor evolves with both internal phase shift angles (θ_1 and θ_2) at three distinct external phase shift angles (ϕ). It is observable that for any given external phase shift, there exists an optimum combination of θ_1 and θ_2 which maximizes the power factor, hence minimizing reactive power dissipation. Choosing any two angles from Figure 5.4a, plots of power factor variation with ϕ for SPS, DPS, EPS, and TPS modulation schemes can be obtained, as seen in Figure 5.4b. The plots indicate that as ϕ increases from 0 to $\frac{\pi}{2}$, the power factor initially increases and then gradually decreases for all four modulation schemes, showing that there is an optimal ϕ which produces the highest power factor.

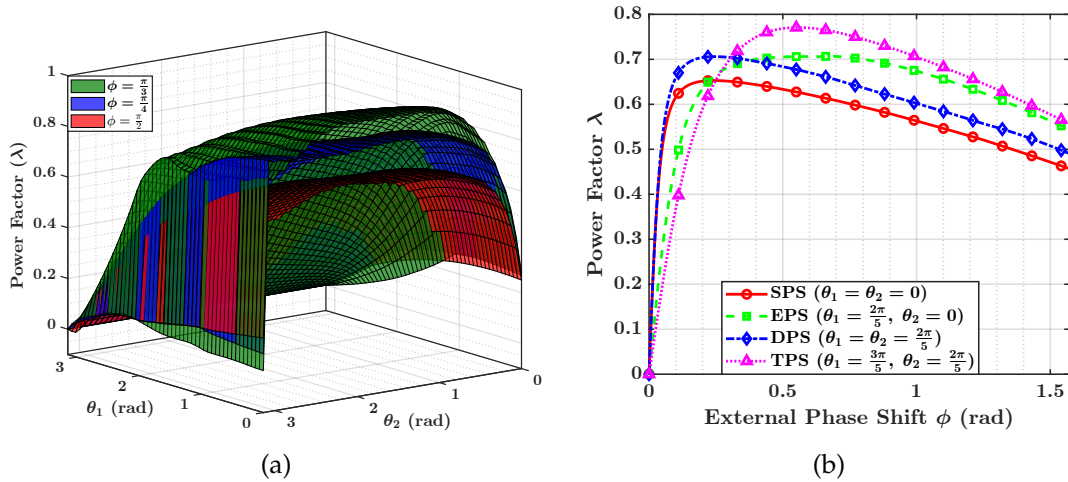


Figure 5.4: (a) Variation of power factor with internal and external phase shift angles (b) variation of power factor with external phase shifts under different modulation schemes.

In SPS, the external phase shift, ϕ , is used solely to control power flow, so it can't be used to determine the optimal point for maximum power factor. However, in the parameter design process, the inductance is typically chosen to ensure that the converter operates at the optimum ϕ during rated conditions. For EPS, DPS, and TPS, ϕ not only controls the magnitude and direction of power flow but also allows θ_1 and θ_2 to regulate the power factor. This enables the minimization of circulating current, maximization of power factor, and, consequently, maximum transmission efficiency. This is further confirmed from the plots in Figure 4b which shows that DPS, EPS, and TPS schemes can achieve higher power factors compared to SPS if properly designed. Therefore, determining the optimal internal phase shift angles is crucial for maximizing the power factor.

5.3 Vector Control based on LADRC

The suggested control system employed for the battery charging is depicted in Figure 5.5. It comprises of an external LADRC voltage loop that creates the reference battery current for the internal LADRC battery current loop. This loop in turn produces the reference current for the innermost inductor current LADRC loop which controls the decoupled inductor current. Additionally, a novel feedforward loop is integrated into the output of the external voltage loop for dynamic performance enhancement. The output of the inductor current LADRC loop is sent to a block that calculates the optimum internal and external phase shift angles, which are then used by the DPS modulator to regulate power flow. Table 5.2 shows the DAB converter's design specifications for the control system design. The operational principle of LADRC has already been discussed in Section 4.4.2.1.

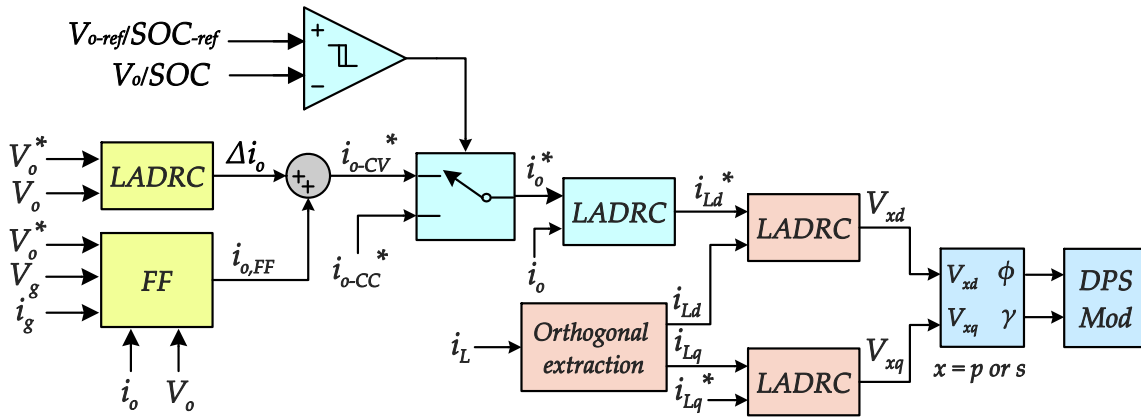


Figure 5.5: Proposed battery charging control system with three-loop configuration.

5.3.1 DPS Modulation

Figure 5.6a shows the three-level DPS modulator. It contains a triangular carrier generator that generates a triangular waveform ranging from 0 to 2π . This carrier signal is then phase-shifted with both the internal and external phase angles before being fed into a sinusoidal signal generator, which outputs a signal ranging from -1 and 1. This signal is then passed to a comparator, which generates the relevant PWM signals for each full-bridge pair with a fixed

Table 5.2: DAB converter specifications.

Parameter	Value
Input voltage (V_g)	756 V
Battery nominal voltage (V_o)	900 V
Switching frequency (f_s)	100 kHz
Leakage inductance (L)	1.8 μ H
Rated Power (P_o)	250 kW
Parasitic resistance of inductor and transformer (r_L)	50 m Ω
Drain-source on resistance of MOSFET (R_{ds-on})	35 m Ω
Transformer turns ratio ($n_p : n_s$)	5 : 6
Output filter capacitor (C_f)	200 μ F
Filter capacitor ESR (r_c)	50 m Ω

duty ratio of 50%. Figure 5.6b shows an example implementation where $\gamma = 0.1\pi$ and $\phi = 0.3\pi$. The sinusoidally generated signals can be observed as phase shifted relative to one another and fed to their corresponding comparators to produce phase-shifted modulating signals for each full bridge. The overall outcome is the generation of a three-level square wave voltage profile at both ends of each full bridge as shown in the figure.

5.3.2 Extraction of Inductor Current Orthogonal Components

The inductor current vector control loop design begins with the extraction of the inductor current orthogonal components as illustrated in Figure 5.7.

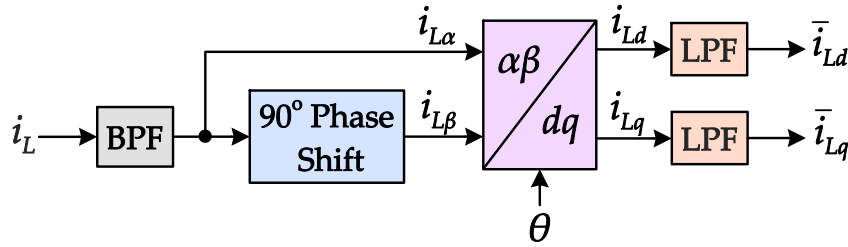


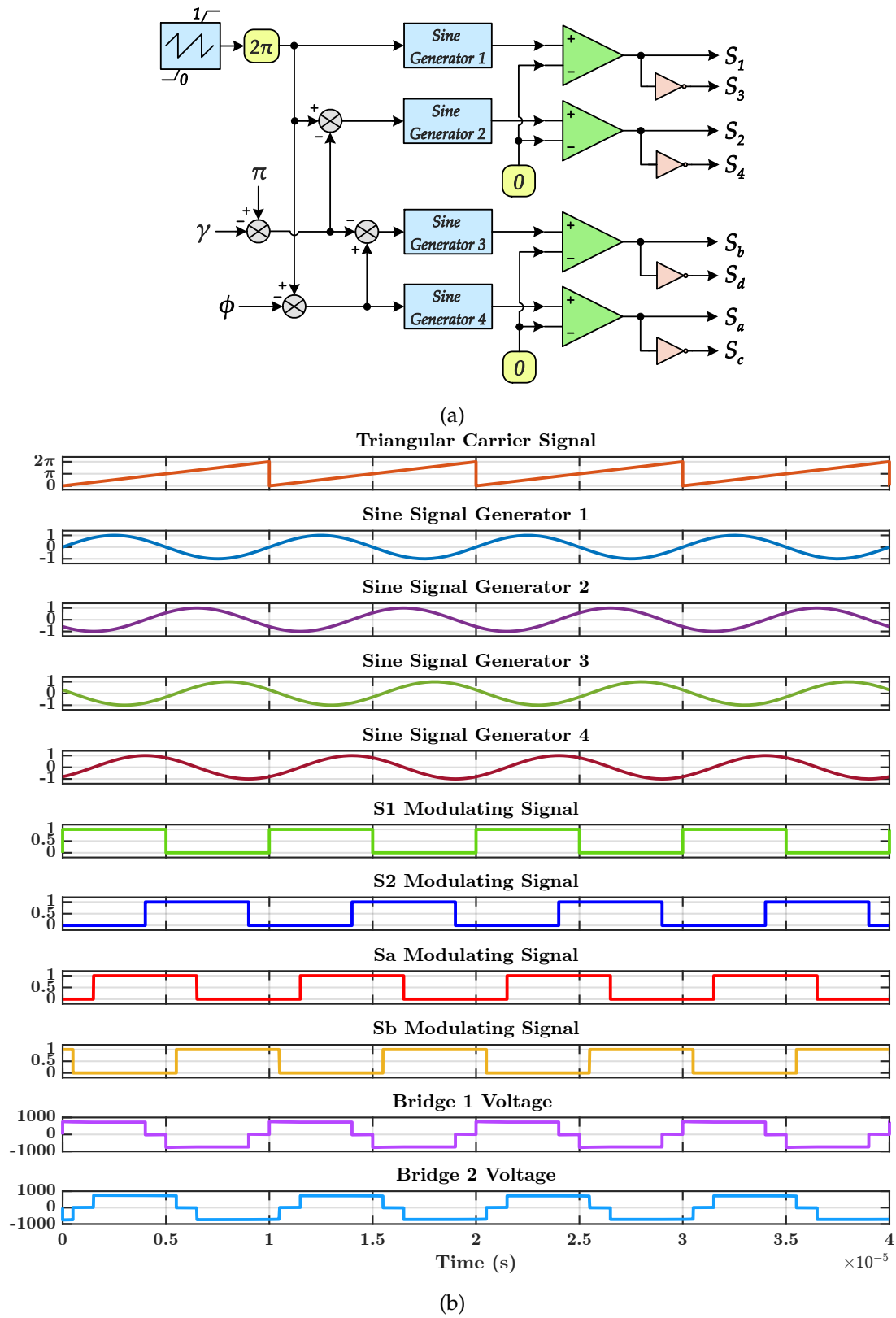
Figure 5.7: Block diagram showing the extraction of the inductor current active and quadrature components.

As can be observed, the measured inductor current is initially fed through a bandpass filter (BPF) to extract its fundamental component and suppress higher-order harmonics. A second-order BPF is employed, and its transfer function is defined by (5.12) [494, 495]:

$$H(s) = \frac{K \left(\frac{\omega_c}{Q} \right) s}{s^2 + \left(\frac{\omega_c}{Q} \right) s + \omega_c^2}, \quad (5.12)$$

where K represents the DC gain of the filter, ω_c denotes the center or resonant frequency, and Q refers to the quality factor. The bandwidth (BW) is related to Q and ω_c as expressed in (5.13):

$$BW = \frac{\omega_c}{Q} = \omega_H - \omega_L, \quad (5.13)$$



where ω_H and ω_L represent the high and low filter cut-off frequencies in radians per second, respectively. The relationship between ω_c , ω_H , and ω_L is described in (5.14):

$$\omega_c = \sqrt{\omega_H \omega_L}. \quad (5.14)$$

The design of the BPF is done using equations (5.12)–(5.14) together with the parameters in Table 5.3.

Table 5.3: Bandpass filter specifications.

Filter parameter	Value
DC gain (K)	1
Quality factor Q	5
Centre frequency (f_c)	100 kHz

Figure 5.8a shows the BPF's frequency response for Q values of 0.5, 1, 2, 5, 10, and 20. It is observed that the larger the Q value, the better the BPF's pass-band performance (higher selectivity), but the permissible frequency range decreases. Furthermore, Figure 5.8b depicts the BPF's unit step response for the same Q values. As Q increases, there's a decrease in the initial system overshoot, while the attenuation time and oscillations increase, thus affecting the DAB converter's dynamic performance during sudden load changes. Based on these observations, $Q = 5$ has been chosen as a suitable compromise between enhanced system dynamic performance and the BPF's signal attenuation capabilities.

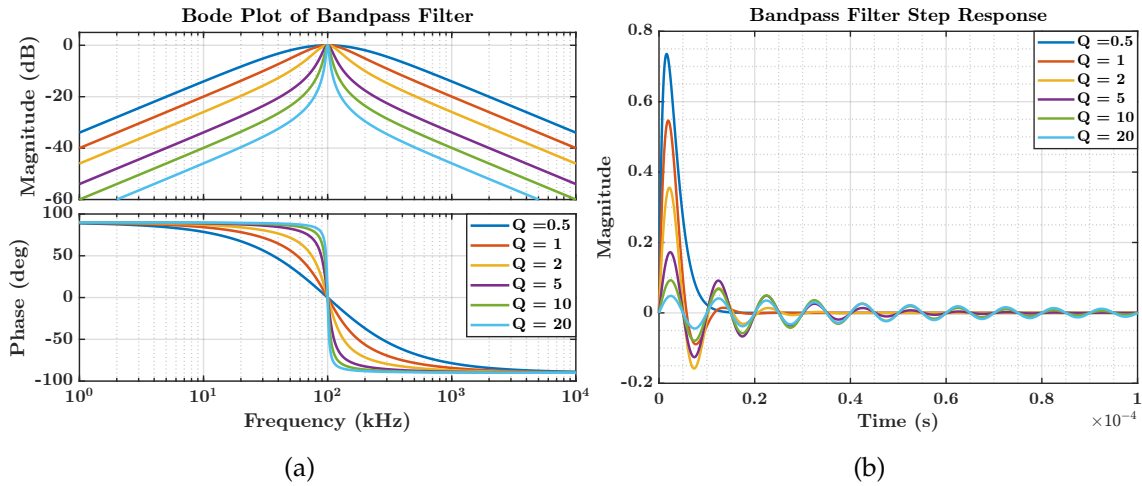


Figure 5.8: BPF response for various Q values: (a) Frequency response; (b) unit step response.

Once the inductor current's fundamental component has been extracted, an orthogonal current signal is created by introducing a 90° phase shift delay to it. Following this, a coordinate transformation from the stationary frame ($\alpha\beta$) to the synchronous rotating frame (dq), known as the Park transform, is applied to obtain the direct and quadrature components of the inductor current, thus enabling the decoupled and independent control of the active and reactive power in the DAB converter. This transformation is expressed by (5.15) [496, 497]:

$$\begin{bmatrix} i_{L_d} \\ i_{L_q} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} i_{L_\alpha} \\ i_{L_\beta} \end{bmatrix}. \quad (5.15)$$

To perform the $\alpha\beta$ - dq transformation, an instantaneous phase angle (θ) is required, and this is given by (5.16):

$$\theta = \int \omega_s(t) dt. \quad (5.16)$$

To suppress any noise that may occur at the output of the $\alpha\beta$ - dq coordinate transformation, a second-order low pass filter (LPF) is employed to extract the DC components $\bar{i}_{L_d}$ and $\bar{i}_{L_q}$. The LPF transfer function used is given in (5.17):

$$G(s) = \frac{K\omega_c^2}{s^2 + \left(\frac{\omega_c}{Q}\right)s + \omega_c^2}. \quad (5.17)$$

The design coefficients for the LPF are provided in Table 5.4.

Table 5.4: Low pass filter specifications.

Filter parameter	Value
DC gain (K)	1
Quality factor Q	1
Centre frequency (f_c)	100 kHz

Figure 5.9a shows the LPF's frequency response for Q values of 0.5, 1, 2, 5, 10. It can be observed that a higher Q value results in greater resonant peak. Moreover, Figure 5.9b shows the LPF's unit step response for the same Q values. As Q increases, there is a noticeable rise in the system oscillations, overshoots, and response times which negatively affects the DAB converter's dynamic performance particularly during system disturbances. Consequently, $Q = 1$ has been chosen as a suitable compromise, balancing improved system dynamic performance and the LPF's signal attenuation capabilities.

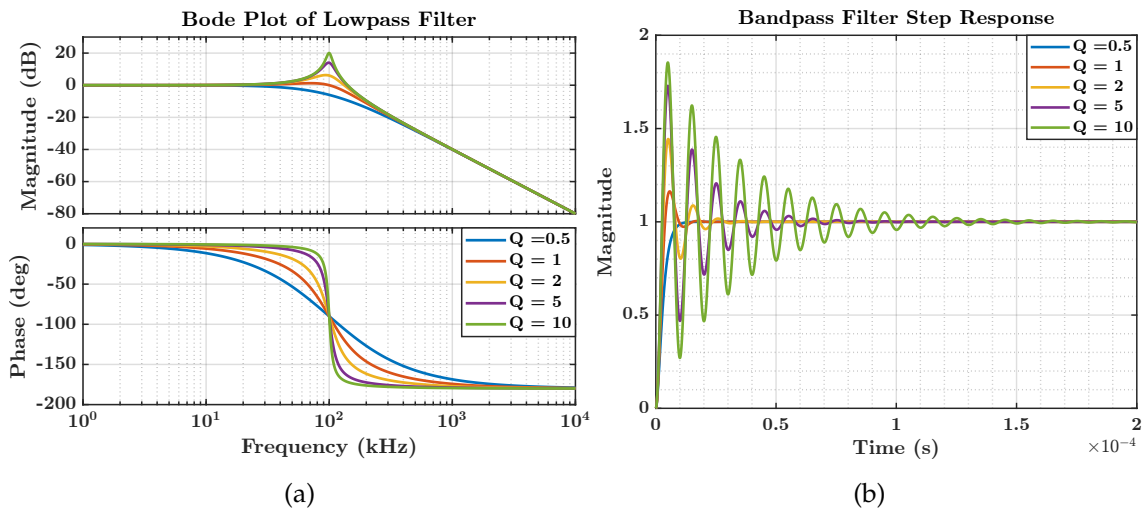


Figure 5.9: LPF response for various Q values: (a) Frequency response; (b) unit step response.

5.3.3 LADR-based Inductor Current Control

The LADRC-based control of inductor current starts with the inductor current derivative dynamic equation derived from the DAB equivalent circuit in Figure 5.1a, expressed as:

$$\frac{di_L}{dt} = \frac{v_p}{L} - \frac{i_L r_L}{L} - \frac{v_s}{L}. \quad (5.18)$$

To decouple (5.18), an intuitive approach is to employ GAM based on the complex exponential Fourier series expansion of periodic time-dependent variables, which has been introduced in Section 4.3.2.1. By applying GAM equation (4.28) to (5.18), the following expression is obtained:

$$\frac{d\langle i_L \rangle_1}{dt} = -j\omega \langle i_L \rangle_1 + \langle \frac{di_L}{dt} \rangle_1 = -j\omega \langle i_L \rangle_1 + \frac{\langle v_p \rangle_1}{L} - \frac{\langle i_L r_L \rangle_1}{L} - \frac{\langle v_s \rangle_1}{L}. \quad (5.19)$$

Letting $\langle i_L \rangle_1 = i_{Ld} + ji_{Lq}$, $\langle v_p \rangle_1 = v_{pd} + jv_{pq}$, and $\langle v_s \rangle_1 = v_{sd} + jv_{sq}$, and simplifying (5.19), results in the decoupled system of equations in (5.20):

$$\begin{cases} \frac{di_{Ld}}{dt} = \omega i_{Lq} + \frac{v_{pd}}{L} - \frac{r_L i_{Ld}}{L} - \frac{v_{sd}}{L}, \\ \frac{di_{Lq}}{dt} = -\omega i_{Ld} + \frac{v_{pq}}{L} - \frac{r_L i_{Lq}}{L} - \frac{v_{sq}}{L}. \end{cases} \quad (5.20)$$

The set of equations in (5.20) can be reformulated in a form appropriate for LADRC depending on the control objective as follows:

$$\begin{cases} \frac{di_{Ld}}{dt} = -\frac{v_{sd}}{L} + f(\omega, v_{pd}, i_{Ld}, i_{Lq}), \\ \frac{di_{Lq}}{dt} = -\frac{v_{sq}}{L} + f(\omega, v_{pq}, i_{Ld}, i_{Lq}), \end{cases} \quad (5.21)$$

or

$$\begin{cases} \frac{di_{Ld}}{dt} = \frac{v_{pd}}{L} + f(\omega, v_{sd}, i_{Ld}, i_{Lq}), \\ \frac{di_{Lq}}{dt} = \frac{v_{pq}}{L} + f(\omega, v_{sq}, i_{Ld}, i_{Lq}). \end{cases} \quad (5.22)$$

The set of equations in (5.21) and (5.22) take the form $\dot{y} = bu + f$, thus their tuning adheres to the concepts outlined in Section 4.4.2.1. The control variables in (5.21) (v_{sd} and v_{sq}) and (5.22) (v_{pd} and v_{pq}) are employed to derive the internal and external phase shift angles in a simple and optimal manner to regulate power flow.

5.3.4 Phase Angle Determination for Reactive Power and RMS Inductor Current Minimization

The analysis performed in Section 5.2.2 showed that the fundamental components of active and reactive power dominate, significantly outweighing those of higher-order harmonics, and can be closely used to approximate the actual active and reactive power with minimal error. Therefore, to simplify the analysis, only the fundamental components are considered to determine the optimal phase angles which minimize the reactive power and RMS inductor current value.

To minimize or eliminate the reactive power, it is necessary to ensure that the reactive component of inductor current (i_{Lq}) should be equal to zero. At this moment, the inductor current is represented only by its active component (i_{Ld}) whose phase is the same as that of either

the primary voltage (V_p) or secondary voltage (V_s) depending on the chosen control objective from (5.21) and (5.22). This condition is graphically represented in the phasor diagrams given in Figure 5.10 where the inductive resistive has been neglected for simplified analysis.

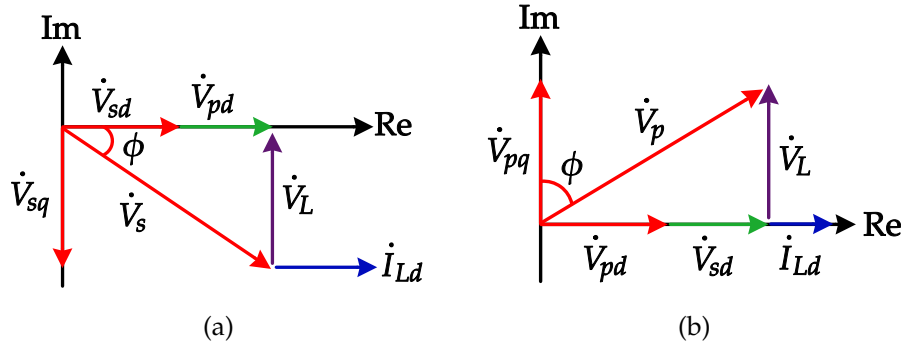


Figure 5.10: Phasor diagrams for DAB positive power flow in DPS: (a) control objective is controlling magnitude and phase of inductor secondary voltage (b) control objective is controlling magnitude and phase of inductor primary voltage with 90° axis rotation.

Considering the first case given in Figure 5.10a, whose control objective is to generate the reference inductor secondary voltage as defined by equation (5.21), the required external phase shift (ϕ) for DPS power flow control and internal phase shift (γ) derived from the Fourier series expansion in (5.2) for secondary voltage magnitude control, are given in equation (5.23):

$$\left\{ \begin{array}{l} \phi = \tan^{-1} \left(\frac{v_{sq}}{v_{sd}} \right), \\ \gamma = \left\{ \begin{array}{l} \pi - 2 \sin^{-1} \left(\frac{\pi \sqrt{v_{sd}^2 + v_{sq}^2}}{4V_o} \right), \\ 2 \cos^{-1} \left(\frac{\pi \sqrt{v_{sd}^2 + v_{sq}^2}}{4V_o} \right). \end{array} \right. \end{array} \right. \quad (5.23)$$

For the second case shown in Figure 5.10b, whose objective is generating the reference dq components of inductor primary voltage as mathematically expressed in (5.22), the required internal and external phase shifts which minimize reactive power are given by (5.24):

$$\left\{ \begin{array}{l} \phi = \frac{\pi}{2} - \tan^{-1} \left(\frac{v_{pq}}{v_{pd}} \right), \\ \gamma = \left\{ \begin{array}{l} \pi - 2 \cos^{-1} \left(\frac{\pi \sqrt{v_{pd}^2 + v_{pq}^2}}{4V_g} \right), \\ 2 \sin^{-1} \left(\frac{\pi \sqrt{v_{pd}^2 + v_{pq}^2}}{4V_g} \right). \end{array} \right. \end{array} \right. \quad (5.24)$$

Thus, both the reactive current and peak input/inductor current of the DAB converter can be effectively controlled by regulating the magnitude of the fundamental component of both the primary and secondary voltages. This approach simplifies the analysis, since the same method

can be efficiently applied across various operating states, removing the need for complicated control functions found in typical time-domain optimization problems.

5.3.5 LADRC-based Output Current Loop Control

This loop regulates the output current, thus the battery average current, and produces the reference active inductive current for the LADRC-based inductor current control loop. The relationship between the DAB converter's output and inductor currents is given by:

$$i_o = \frac{Si_L}{n} \quad (5.25)$$

where n denotes the transformer turns ratio and S is the switching function of full bridge 2, as given in (5.26):

$$S(t) = \begin{cases} 1, & \gamma + \phi \leq \omega t < \pi + \phi - \gamma, \\ -1, & \pi + \gamma + \phi \leq \omega t < 2\pi + \phi - \gamma, \\ 0, & \text{otherwise.} \end{cases} \quad (5.26)$$

Substituting (5.18) into the time derivative of (5.25) results in (5.27):

$$\frac{di_o}{dt} = \frac{Sv_p}{nL} - \frac{Si_L r_L}{nL} - \frac{Sv_s}{nL}. \quad (5.27)$$

Applying the GAM equation (4.28) to (5.27) yields the following expression:

$$\frac{d\langle i_o \rangle_0}{dt} = \frac{\langle Sv_p \rangle_0}{nL} - \frac{r_L \langle Si_L \rangle_0}{nL} - \frac{\langle Sv_s \rangle_0}{nL}. \quad (5.28)$$

Using (5.28) and the GAM equation (4.29), the resulting equation is:

$$\begin{cases} \langle i_L S \rangle_0 = \underbrace{\langle i_L \rangle_0 \langle S \rangle_0}_{=0} + \langle i_L \rangle_1 \langle S \rangle_{-1} + \langle i_L \rangle_{-1} \langle S \rangle_1 \\ = 2 [\text{Re}(\langle i_L \rangle_1) \text{Re}(\langle S \rangle_1) + \text{Im}(\langle i_L \rangle_1) \text{Im}(\langle S \rangle_1)] . \end{cases} \quad (5.29)$$

Letting $\langle S \rangle_1 = p_x + jp_y$, leads to $\langle i_L S \rangle_0 = 2 (i_{Ld} p_x + i_{Lq} p_y)$. The other products can then be obtained in a similar way and are given in (5.30):

$$\begin{cases} \langle Sv_p \rangle_0 = 2 (v_{pd} p_x + v_{pq} p_y) , \\ \langle Sv_s \rangle_0 = 2 (v_{sd} p_x + v_{sq} p_y) . \end{cases} \quad (5.30)$$

Equation (5.28) can then be finally simplified to:

$$\frac{d\langle i_o \rangle_0}{dt} = \left(-\frac{2r_L p_x}{nL} \right) i_{Ld} + \frac{2}{nL} [(v_{pd} - v_{sd}) p_x + (v_{pq} - v_{sq} - 2i_{Lq} r_L) p_y] . \quad (5.31)$$

Equation (5.31) can be expressed as $\dot{y} = bu + f$, facilitating the application of LADRC as given in (5.32). The LADR-based output current controller tuning adheres to the same principles outlined in Section 4.4.2.1.

$$\frac{d\langle i_o \rangle_0}{dt} = -\frac{2r_L p_x}{nL} i_{Ld} + f(v_{pd}, v_{sd}, v_{pq}, v_{sq}, p_x, p_y, i_{Lq}). \quad (5.32)$$

The exponential Fourier series expansion of (5.26) results in the real and imaginary components of $\langle S \rangle_1$, which are given in (5.33):

$$\begin{cases} p_x = -\frac{2}{\pi} \cos\left(\frac{\gamma}{2}\right) \sin(\phi), \\ p_y = -\frac{2}{\pi} \cos\left(\frac{\gamma}{2}\right) \cos(\phi). \end{cases} \quad (5.33)$$

5.3.6 Battery Voltage Loop Control Based on LADRC

This controller controls the battery voltage during the CV mode of battery charging. For LADRC realization, the dynamic equation of the output capacitor voltage derivative is necessary and is given by:

$$\frac{dv_c}{dt} = \frac{i_o}{C} - \frac{i_b}{C} = \frac{i_o}{C} + f(i_b), \quad (5.34)$$

Since (5.34) is already in the form $\dot{y} = bu + f$, the capacitor voltage v_c can then be directly regulated to generate the output current i_o setpoint using the LADRC approach described in Section 4.4.2.1.

5.3.7 Proposed Feedforward for Dynamic Performance Enhancement

The transition from CC to CV introduces a significant system disturbance, leading to poor voltage and current dynamic performances. To improve the dynamic response, increase efficiency, and ensure a seamless transition from CC to CV, a feedforward compensation (FF block), as seen in Figure 5.5, has been introduced at the output of the external voltage loop controller which generates a feedforward current (I_{of}). In this section, a novel feedforward expression is proposed which is suitable for both three-level and two-level phase-shift modulated systems, and it's described next.

A linear droop control technique has been employed to obtain the reference input current signal of the controller. Let $Q(V_o^*, i_{in}^*)$ be a fixed point on a non-vertical line, L_1 , with slope k , and $P(V_o, i_{in})$ be an arbitrary point on L_1 as depicted in Figure 5.11a. Then based on linear algebra, the slope of L_1 is expressed as:

$$k_u = \frac{i_{in}^* - i_{in}}{V_o^* - V_o} \implies i_{in}^* = k_u(V_o^* - V_o) + i_{in}, \quad (5.35)$$

The slope k_u represents a conductance that can be regarded as either the input conductance of the converter (k_{u1}) or the output load conductance (k_{u2}). As a result, i_{in}^* can have two distinct values depending on k , as given by the following:

$$i_{in}^* = \begin{cases} k_{u1}(V_o^* - V_o) + i_{in}, & \text{for } k_{u1} = \frac{i_{in}}{V_{in}}, \\ k_{u2}(V_o^* - V_o) + i_{in}, & \text{for } k_{u2} = \frac{i_o}{V_o}. \end{cases} \quad (5.36)$$

The expression in (5.36) can then be used to obtain a new feedforward term for the output current as follows:

$$i_{of1}^* = \left[\left(\frac{V_o^*}{V_o} \right)^a \left(\frac{i_{in}^*}{i_{in}} \right)^b \right] i_o \quad (5.37)$$

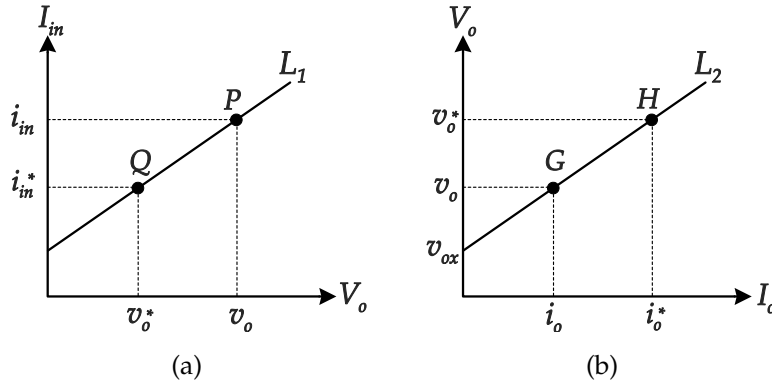


Figure 5.11: Relationship between: (a) input current and output voltage; (b) output voltage and output current.

where a and b are acceleration factors that control the speed at which the converter shifts from CC to CV mode.

Applying a similar droop technique as before, another feedforward term is obtained from the linear relationship between output voltage and current as seen in Figure 5.11b. The slope of the line L_2 is:

$$k_v = \frac{V_o^* - V_{ox}}{i_o^*} = \frac{V_o}{i_o} \quad (5.38)$$

The second feedforward expression can then be obtained from (38) and is given in (39):

$$i_{of2}^* = \left(\frac{V_o^* - V_{ox}}{V_o} \right) i_o \quad (5.39)$$

where V_{ox} represents the system's nominal output voltage. Assuming that at a given time instant, the system's nominal output voltage matches its instantaneous output voltage (i.e. $V_{ox} = V_o$), then (5.39) can be simplified to:

$$i_{of2}^* = \left(\frac{V_o^* - V_o}{V_o} \right) i_o \quad (5.40)$$

By combining (5.37) and (5.40), the overall robust feedforward expression can be derived and is given in (5.41) which effectively mitigates system disturbances and enhances system dynamics:

$$i_{of}^* = i_{of1}^* + i_{of2}^* = \left\{ \left[\left(\frac{V_o^*}{V_o} \right)^a \left(\frac{i_{in}^*}{i_{in}} \right)^b + \left(\frac{V_o^* - V_o}{V_o} \right) \right] \right\} i_o \quad (5.41)$$

5.4 Numerical Verifications

MATLAB/Simulink is employed to verify the various DPS-based DAB control techniques presented in this chapter. Moreover, Table 5.5 lists the parameters for the three-loop controller and the corresponding feedforward constants.

Table 5.5: Vector Control parameters.

Description	Parameter	Value
LADRC for inductor current	ω_{c1}, ω_{o1}	5000 rad/s, 20000 rad/s
LADRC for output current	ω_{c2}, ω_{o2}	2000 rad/s, 6000 rad/s
LADRC for output voltage	ω_{c3}, ω_{o3}	1000 rad/s, 3000 rad/s
Feedforward parameters	a, b	4, 4

The battery charging process begins with a constant current of 270 A, followed by a constant voltage of 900 V. Figure 5.12 depicts the DAB inductor current along with its decoupled alpha and beta components during the second charging phase, showing that the beta component is phase-shifted by 90° from the alpha counterpart as anticipated.

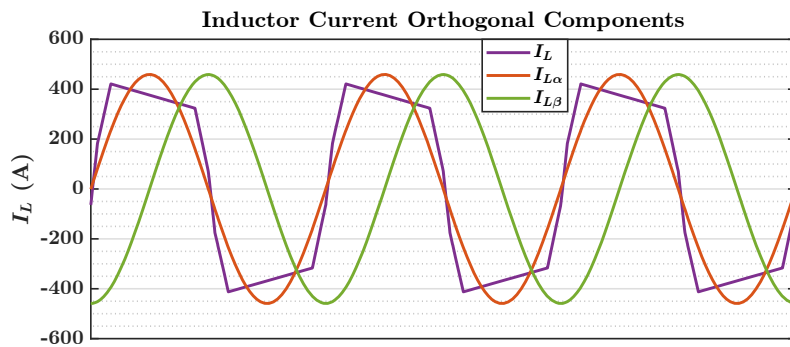


Figure 5.12: Inductor current and its decoupled components.

Following the decoupling of the alpha and beta inductor current components, a Park transform is applied to obtain the active and reactive components of the inductor current, thus facilitating the independent and decoupled control of the DAB's active and reactive power.

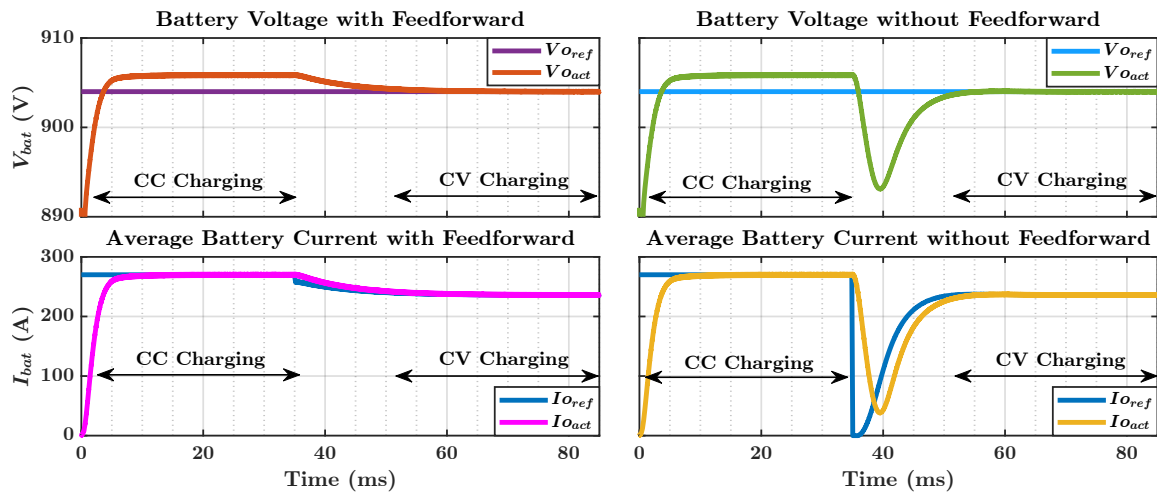


Figure 5.13: Battery voltage (**top**) and average battery current (**bottom**) with (**left**) and without (**right**) feedforward.

Figure 5.13 depicts the actual and reference battery voltage as well as the average battery current, for each charging mode, with and without the suggested droop-based feedforward

approach. In both scenarios, the battery is first charged at a CC of 270 A, with no voltage control. At $t = 35$ ms, the charging mode changes to CV, and the battery voltage begins to be controlled at 904 V. However, in the absence of the suggested feedforward technique, the battery current and voltage dip significantly during the switch from CC to CV lasting 20 ms. With the proposed approach, a very smooth and seamless transition from CC to CV is observed, lasting only 8 ms.

A similar behavior is noticed in the dq -axis control loop of the inductor current, as shown in Figure 5.14. In this loop, the q -axis component is set to a reference value of zero to minimize the converter's reactive power dissipation. As seen, without the proposed approach, the q -axis exhibits a significant overshoot of 30 A during the transition from CC to CV, requiring approximately 20 ms for the q -axis component to regain its control. In contrast, with the proposed method, the overshoot in the q -axis component is significantly reduced to just 3 A, allowing the system to regain control in just 8 ms. The d -axis inductor current follows the pattern of the output battery current since its setpoint comes from the external battery output current loop. Thus, huge dips are also noticed during the CC-CV transition period without the feedforward but are eliminated when the feedforward is applied.

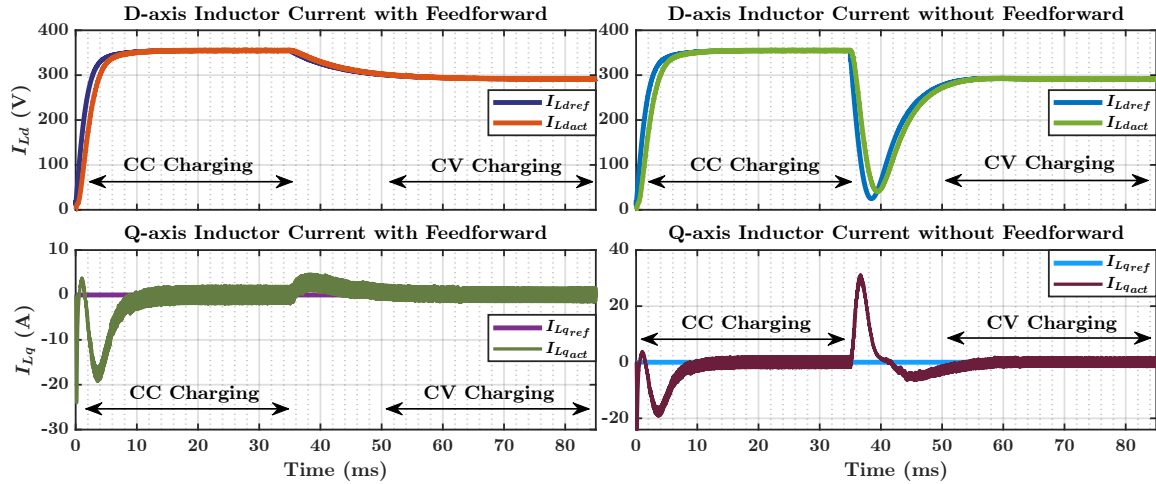


Figure 5.14: DQ-axis inductor current control with and without the proposed feedforward technique.

The overall impact of the transition from CC to CV on the converter is illustrated in the input current and inductor current waveforms in Figure 5.15. Without the proposed approach, a large dip is observed in both the inductor and input currents, while the application of the proposed technique results in a smooth transition in their waveforms. The switch from CC to CV represents an abrupt change in load demand, leading to significant changes in system dynamics. Since the control strategy doesn't take into consideration this mode change, the abrupt transition creates a mismatch between the expected and actual conditions of the controller. This discrepancy causes a rapid fluctuation in the battery output current, resulting in a sharp drop. However, this issue is mitigated by implementing the proposed feedforward scheme, which anticipates the transition and adjusts the control effort in advance, minimizing the impact of the mode change and enhancing system stability.

Next, the impact of the acceleration factors (a and b) on the converter's battery current and voltage dynamic performance is examined. The results obtained are presented in Figure 5.16. It is

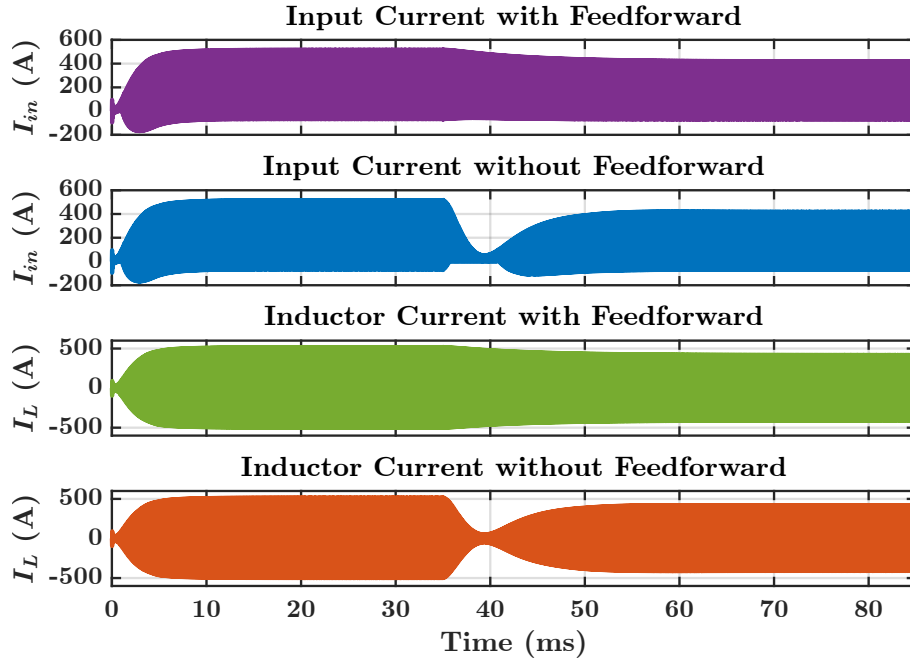


Figure 5.15: Input and Inductor current transient waveforms with and without the proposed feedforward technique.

clear that for both the battery current and voltage, the changeover time from CC to CV decreases as the acceleration factors increase, in this instance from 4 to 6. Therefore, a higher acceleration factor results in a faster transition speed, enabling quicker elimination of disturbances of any type.

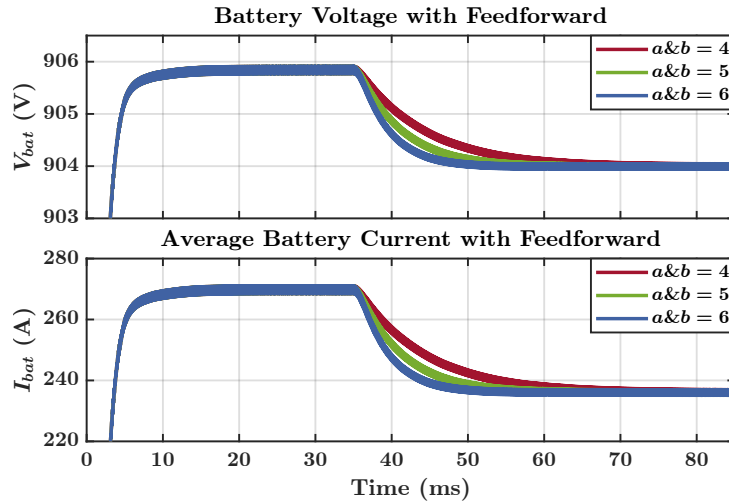


Figure 5.16: Effect of acceleration factor on dynamic performance.

In the simulations conducted previously, the control parameters specified in Table 5.5, including the proportional gain and ADRC bandwidths, were selected to achieve optimal transient and steady-state performance, in accordance with the design guidelines outlined in Section 4.4.2.1. However, in practical scenarios, these parameters are typically determined based on the converter's power rating, expected disturbances and the dynamic behavior of the EV battery model. It is thus essential for the observer's bandwidth to be sufficiently wide to

effectively track disturbances but not so wide that it introduces significant noise issues.

Finally, a comparison is made between LADRC and the PI controller, both designed with the same BWs, and the results obtained with and without the proposed feedforward technique are depicted in Figure 5.17. Without feedforward, both controllers exhibit significant dips in battery current and voltage during the change from CC to CV. However, the LADRC transitions to CV mode and reaches steady state more quickly, with smaller dips compared to the PI controller. As can be observed, implementing the proposed feedforward control scheme effectively eliminates the voltage and current dips during the mode change for both the controllers, with both demonstrating similar transition times thereby highlighting the strength of the proposed feedforward scheme.

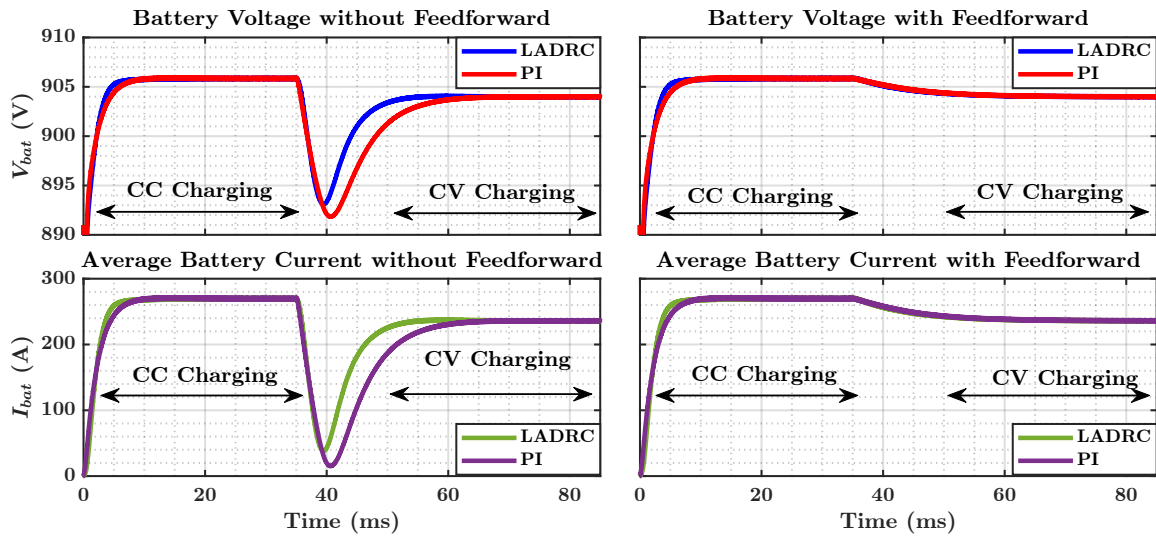


Figure 5.17: Comparison of PI and LADRC: Battery voltage (**top**) and average battery current (**bottom**) without (**left**) and with (**right**) feedforward.

As demonstrated, the LADRC outperforms the PI controller when feedforward isn't applied during the transition between charging modes. This superiority can be attributed to the inherent characteristics of LADRC, which effectively estimates and rejects disturbances through its ESO, allowing it to adapt rapidly to dynamic changes such as sudden changes in reference modes. However, when the feedforward control is incorporated into both the PI and LADRC systems, it directly predicts the transition and provides a corrective input. This reduces the necessity for corrective actions from both controllers, leading to comparable performance for both.

5.5 Conclusion

This chapter has outlined the design and dynamic control of a DAB-based battery charging system utilizing DPS modulation. Moreover, an extensive LADRC modeling of each of the three loops comprising the entire control system was developed. Additionally, a vector control approach was employed to decouple and control the orthogonal components of the inductor current, while a Fourier series-based method was used to obtain the optimal phase shift angles for controlling the converter's power flow and minimizing reactive power, providing a simpler

alternative to conventional piecewise time-domain approaches. Furthermore, a novel droop-based feedforward control was introduced to ensure smoother transitions between CC and CV charging modes, along with an analysis of how acceleration factors in the feedforward expression impact the converter's dynamic performance. Additionally, comparisons between the LADRC and PI controller revealed that LADRC achieves superior performance in terms of transition time and voltage/current dips in the absence of any feedforward control, owing to its ESO.

For practical implementation of the proposed control schemes, it is crucial to ensure that the controller cannot only accommodate the wide variations in voltage and current typically encountered in EV charging systems, but also the diverse battery models available in the market. Moreover, the use of LADRC presents challenges in properly tuning the ESO gains in real-time, given the non-linear behavior exhibited by batteries during charging. These issues can be effectively addressed through optimization algorithms like simulated annealing, genetic algorithms, bee algorithms and learning-based techniques that adaptively set the controller parameters to eliminate all system uncertainties. Additionally, the conventional LADRC implemented in this chapter necessitates accurate measurement of system states and lumped disturbances, which can be difficult in noisy, real-world conditions. To address this issue, techniques such as resonant ESO, model-compensated ESO, linear-Nonlinear ESO or cascaded ESO can be employed to maintain a balance between estimation accuracy and noise reduction. Furthermore, with proper tuning, the proposed LADRC system can handle small signal transmission delays commonly encountered in practical EV charging applications. However, in cases where time delays are significant, approaches like polynomial-based predictive ADRC (PP-ADRC), Smith predictor-based ADRC (SP-ADRC) and predictor observer-based ADRC (PO-ADRC) can be utilized to enhance the performance of traditional ADRC methods.

Chapter 6

Modular DAB System Design, Modelling and Control

6.1 Introduction

To meet the diverse charging needs of EVs in fast DC charging applications, converters must be designed to handle high power levels. However, these high power demands result in significant voltage and current stresses on power electronic components, which can also increase costs. It is therefore crucial to reduce these stresses by selecting suitable topologies or appropriate switching techniques [498]. Three approaches can be considered to solve these issues. The first approach involves using semiconductor devices with high voltage/current ratings integrated into different converter topologies with series/parallel configurations. However, series connections can lead to uneven voltage distribution across switches due to variations in parameters such as switching delays, leakage inductance, and switch output capacitance. To prevent failures, voltage balancing techniques are thus required. The second approach uses multilevel converters to reduce voltage stress. However, this approach requires a sufficient number of levels to be effective, which can be limited by the large number of additional components such as clamping diodes or flying capacitors, and the increased control complexity [499, 500]. The third approach involves cascading power converters in various modular or multicell configurations like input-series-output-parallel (ISOP), input-series-output-series (ISOS), input-parallel-output-parallel (IPOP), and input-parallel-output-series (IPOS), as shown in Figure 6.1. Converter modularization enables cost reduction, improves system fault tolerance (and thus reliability) due to redundancy, and improve scalability depending on power transfer demand. Modularization also facilitates thermal management since each module handles only a portion of the total power. This power division allows for the use of lower-rated power switches, which support higher switching frequencies. As a result, overall converter efficiency improves due to reduced losses, and the transformer size can be decreased with higher switching frequencies [501, 502].

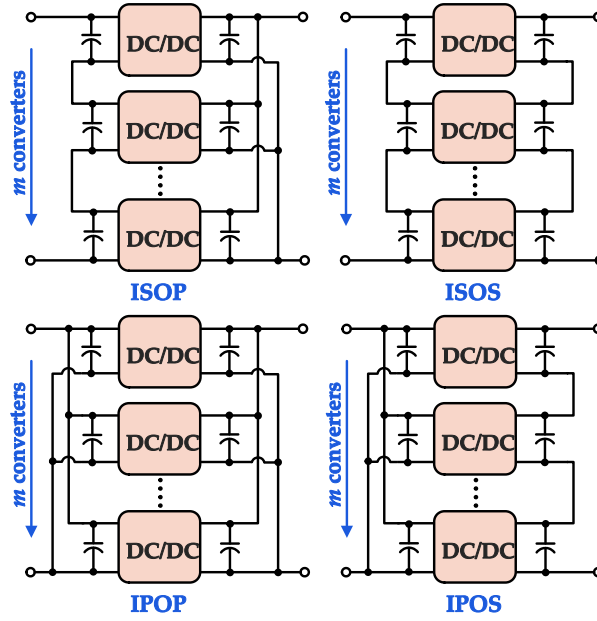


Figure 6.1: Different connection schemes for modular DC-DC converters..

In practice, mismatches in intermediate DC-link capacitors, DAB storage inductors and transformer parameters (like leakage inductance and resistance) across different DAB modules cause variations in the module voltages and currents. Without a proper power balancing approach, these deviations can increase over time, potentially destabilizing the system. Moreover, these imbalances lead to higher electrical and thermal stress on the semiconductor switches, the generation of circulating currents, increased risk of device failure from overheating, higher system losses, and reduced overall efficiency [503–505]. To avoid these issues and ensure stable operation of each module within the modular configuration, the equilibrium among modules must be guaranteed through the implementation of adequate power sharing strategies such as input current sharing (ICS), output current sharing (OCS), input voltage sharing (IVS), and output voltage sharing (OVS), while also meeting the EV battery's CC-CV charging requirements. All of these requirements increases the control effort of the controller. Additionally, to minimize the impact of IVS, ICS, OCS, or OVS power sharing control loops on the output voltage and inner current loops, it is necessary to decouple these control loops.

To achieve power sharing among modules, various control schemes have been developed which can be categorized into two main groups: natural power balance methods and those with specific power sharing loops. The simplest approach within the first category is the common duty ratio control scheme [506], where the same duty ratio is applied to all modules, stabilizing the overall system. Despite its implementation simplicity, parameter mismatches between modules can result in poor sharing accuracy, with larger mismatches leading to worse performance. Besides, this approach leads to poor system steady-state and dynamic characteristics. In [507], common phase shift (CPS) control is used for power sharing in ISOP DAB converters employing SPS modulation. The study claims that stability can be ensured even with parameter mismatches when dead time is considered, while natural power and voltage sharing is achieved in [508] using only a common synchronization signal across modules in the ISOP/IPOP configuration. CPS control has also been proposed in [509] for a modular multiactive bridge (MMAB) employing

DPS modulation to enhance efficiency through an optimal power loss optimization strategy. Decentralized IVS or OCS control strategies, such as input voltage droop control and output current inverse droop control, have also been proposed for ISOP systems to achieve power sharing [510,511]. These decentralized IVS control schemes change the output characteristics of each module to automatically achieve IVS and OCS [512,513], improving reliability by eliminating the need for communication between modules.

The second category includes specified control schemes designed to guarantee accurate power sharing, even when module parameters are mismatched. They can be divided into three subcategories: (i) input side sharing control schemes (ii) output side sharing control schemes and (iii) combined input and output sharing control schemes. A master–slave control scheme proposed in [514] to achieve accurate OVS for IPOS modular systems, adding an input current loop to reduce dynamic overshoot of the output voltage and enhance fault tolerance. IVS is also achieved for ISOP DAB converters in [515] by reshaping the input impedance using a small-signal positive virtual input impedance. A duty cycle exchange control scheme for input series-connected systems is proposed in [516] to improve stability and dynamic response, although it is less suitable for multi-module systems due to its complexity. Moreover, [517] proposes an output current-differential (OCD) control scheme with a master–slave structure to accurately implement OCS in ISOP systems. Here, all control and sampling circuits are located on the output side, thus simplifying the design by eliminating isolation requirements. In addition, [518] presents an input-oriented power sharing control method with fast-dynamic response for ISOP DAB DC-DC converter, allowing flexible module input voltage adjustments for optimal power sharing and output voltage stability under changing input and load conditions. Finally [519], proposes a new power sharing controller based on closed-loop neural network (NN) for IPOS/ISOP DAB converters, to ensuring uniform current/voltage sharing among the modules taking into account the bi-directional power flow characteristic of the converter, possible parameter mismatches and fault scenarios at module and converter levels.

Moreover, the power balancing schemes mentioned above rely on numerous high-bandwidth sensors which not only add to the cost but also introduce noise, requiring significant calibration and filtering efforts [520]. Additionally, high-speed analog-to-digital converters (ADC) are required to process the sensor data. For precise measurements, the ADC sampling rate generally needs to be at least four times higher than the switching frequency. However, this becomes challenging to achieve, particularly when the switching frequency approaches the hundreds of kHz range, where high-speed ADCs become more costly and difficult to implement.

To minimize the number of sensors, ADRC-based observers have shown great effectiveness as highlighted in [521–523]. However, these studies mainly focus on basic converters, with limited application to more advanced modular topologies. Moreover, the load current observer design in these works lead to errors between actual and estimated load currents, and system transient performance hasn't been thoroughly addressed. Disturbance observer [524,525], and current observer-based SMC [526,527] have also been proposed as sensor reduction techniques, but they rely highly on accurate model parameters. Also, an extra PI controller is required, with its gains needing precise tuning to achieve optimal performance. Consequently, when parameter mismatches occur, system performance degrades significantly. In [528], an approach for predicting load current in DAB converters is proposed, though it involves a complex design

for the damping coefficient and does not consider parameter mismatches in the feedback signal. The sensorless current sharing technique described in [529] enhances dynamic performance, but as switching frequencies increase, pulse width and current sharing errors also rise. In [530], an inductor current envelope tracking method is introduced to estimate inductor current without requiring a current sensor, but determining an accurate current boundary demands precise knowledge of the magnetic core and operating conditions.

Furthermore, in modular DAB converter design, voltage ripple plays a key role in determining the size of the input and output filter components, which also depend on the switching frequency and load voltage. Generally, very low voltage ripple is crucial for allowing the use of smaller filter capacitors and reducing the current handling needs of the switches. A common strategy to accomplish this is interleaving, where the switching signals of each module are phase-shifted by an optimal angle [531]. However, the benefits of interleaving are restricted only to power levels close to rated conditions since switching losses in the converter legs tend to surpass conduction losses at light load situations. An interleaved converter's efficiency decreases when all of its modules are operated at light load since the ripple current stays high across all of them. To enhance modular DC-DC converter efficiency at light load, phase shedding could be employed, but the ripple-canceling effect of interleaving diminishes when some modules are disconnected at medium to light load, leading to higher input and output current ripples [532]. This can result in exceeding the maximum voltage and current ripple standards required for EV battery chargers, increasing EMI noise and accelerating battery degradation [533].

To tackle this problem, [534] suggested using larger output capacitance with smaller phases to meet the current and voltage ripple requirements. However, this approach is inefficient since it increases system costs and filter size, while basically eliminating the advantage of using an interleaved topology. In addition, [535] recommended raising the switching frequency when the number of phases is reduced at light loads; however this approach results in higher power losses as frequency rises, eliminating the efficiency-enhancing benefits of phase-shedding.

Inspired by these previous works and their shortcomings, this chapter aims to:

1. Use the SPS control method to analyze how reactive current, current stress, RMS current levels, power losses, and power conversion efficiency vary across the modular DAB converter topologies (shown in Figure 6.1) for offboard EV battery charging. The efficiency is estimated by assessing the converter power losses under different operating conditions using a thermal model. Furthermore, a generalized control system for the modular topologies is also developed, containing three key parts:
 - (a) The first controls the CC-CV battery charging process.
 - (b) The second introduces two feedforward loops to improve the converter's dynamic response to both input voltage and load disturbances.
 - (c) The third tackles the power balance needs across the converter's modules.
2. Propose a technique to achieve high conversion efficiency at medium to light loads while minimizing ripple. The suggested system uses an adaptive rotational technique which helps to evenly distribute the electro-thermal stresses on the various converter modules thus improving reliability and longevity. A phase number selector is also included to

dynamically adjust the phase shifts between the DAB modules, ensuring the merits of interleaving are achieved even at low power. Furthermore, an OCS approach is provided to meet the power balancing needs of the different DAB modules.

3. Propose an improved ESO for estimating battery current for use in fast charging of EVs with a 3-module IPOP DAB architecture. The suggested observer contributes to reducing the number of sensors in systems with two or more modules by two. Furthermore, a feedforward approach is used to enhance the converter's dynamic response during battery charging.

The rest of this chapter is organized as follows: Section 6.2 compares the performance of several modular DAB converter topologies for battery charging. This part will include thermal modelling for efficiency determination, as well as modular DAB modelling to enable power balancing control, followed by numerical validations. Section 6.3 describes the adaptive phase shedding and interleaving technique for improving efficiency and ripple in modular DAB. The interleaving principle of a modular IPOP DAB converter will be discussed first, followed by the proposed control technique and numerical validation. Section 6.4 describes the sensor reduction control technique in modular DAB, along with the novel LESO that accomplishes this goal while section 6.5 concludes the work.

6.2 Performance Evaluation of Various Modular DAB Topologies

6.2.1 Electro-thermal Modelling for Efficiency Determination

A thermal model of the DAB converter is developed in MATLAB/Simulink to evaluate the efficiency of the modular system using the CAB760M12HM3 MOSFET module. The analysis focuses on power losses in the semiconductor devices and passive components, while transformer losses are excluded.

6.2.1.1 Semiconductor Losses

These losses primarily comprise switching and conduction losses in the MOSFET and its body diode. Equations (6.1) and (6.2) respectively provide the average conduction losses in the MOSFET and body diode.

$$P_{cm} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_{ds}(t) I_{ds}(t) dt = R_{ds(on)}(I_{ds}, T_j) \frac{1}{T_{sw}} \int_0^{T_{sw}} I_{ds}^2(t) dt \quad (6.1)$$

$$P_{cd} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_f(t) I_f(t) dt \quad (6.2)$$

where V_{ds} and I_{ds} represent the MOSFET's drain-source voltage and drain current, respectively, whereas V_f and I_f represent the diode's forward voltage and current, respectively, and all of these parameters are affected by the junction temperature T_j . T_{sw} represents the switching period. V_{ds} is determined using lookup table interpolation of I_{ds} and T_j from datasheet curves. Similarly, V_f is derived using lookup table interpolation of I_f and T_j .

The switching losses consist of turn-ON/turn-OFF VI overlap loss (E_{VI}), E_{oss} , and E_{qoss} losses as shown in Figure 6.2. Voltage and current overlap losses are present only in hard switching cases and are defined by the overlap area between the voltage and current waveforms. Consequently, these losses occur during both the turn-ON and turn-OFF phases of a transistor. The drain-source capacitances (C_{oss}) give rise to E_{oss} and E_{qoss} losses, both of which take place solely during the turn-ON process.

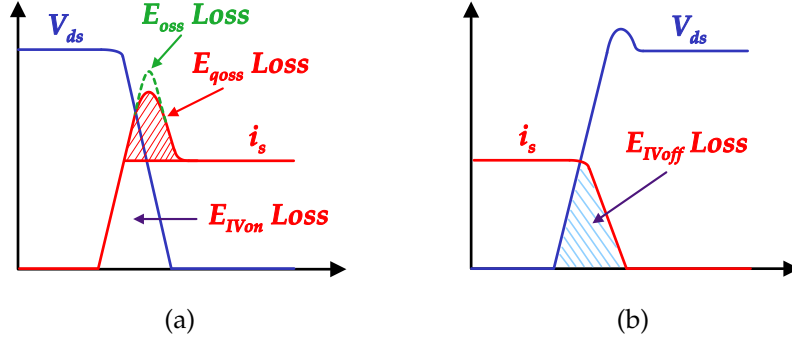


Figure 6.2: Switching power losses: (a) Turn-on losses (b) Turn-off losses

E_{oss} is due to the transistor capacitance C_{oss} . At turn-ON, the transistor closes, causing its drain-source voltage to decrease, leading to the discharge of the capacitance C_{oss} through the transistor. E_{oss} is computed by (6.3).

$$E_{oss} = \int_0^{V_{dc}} V_{ds}(t) C_{oss}(V_{ds}) dV_{ds} \quad (6.3)$$

where V_{dc} is the DC bus voltage. The complementary transistor's C_{oss} capacitor generates E_{qoss} . The C_{oss} capacitor needs to be charged because the transistor is off. Therefore, additional losses result from the charging current I_{qoss} flowing through the active complementary transistor.

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}(t)) C_{oss}(V_{ds}) dV_{ds} = V_{dc} Q_{oss} - E_{oss} \quad (6.4)$$

The total MOSFET turn-ON and turn-OFF energies are determined by:

$$\begin{cases} E_{on} = E_{VIon} + E_{oss} + E_{qoss}, \\ E_{off} = E_{VIoff}. \end{cases} \quad (6.5)$$

From (6.5), the switching losses in the MOSFET and body diode are expressed by (6.6) and (6.7), respectively.

$$P_{sm} = (E_{on} + E_{off}) F_{sw} \quad (6.6)$$

$$P_{sd} = E_{rr} F_{sw} \quad (6.7)$$

Where E_{on} and E_{off} denote the MOSFET turn-ON and turn-OFF energies, respectively, while E_{rr} is the reverse recovery energy of the diode. These energies are all dependent on the device's current, junction temperature, gate resistance, and voltage across its terminals. These characteristics are generally found in the manufacturer's datasheet and can be used to

create lookup tables for predicting the different switching energies and corresponding power losses [536, 537].

From (6.1)–(6.7), the total MOSFET and body diode losses can be derived, and this is given by (6.8):

$$\begin{cases} P_m = P_{cm} + P_{sm}, \\ P_d = P_{cd} + P_{sd}, \\ P_t = P_m + P_d. \end{cases} \quad (6.8)$$

The total semiconductor losses in (6.8) are then fed into a 5th–order Foster type network as shown in Figure 6.3. The RC parameters for this network are obtained from the thermal impedance curves of the MOSFET and body diode in the datasheet, using curve fitting in MATLAB with the CFTOOL. The thermal interface material (TIM) is modeled by a first-order Foster network, while the thermal network between the heat sink (HS) and ambient is simplified using thermal resistance.

The two heat sources, P_m and P_d , are the MOSFET chips and the diode chips, respectively. Although a Cauer thermal model can provide an accurate representation of physical structures, its complicated mathematical formulation makes it less practical. Moreover, Foster models achieve comparable accuracy in estimating junction temperature; therefore, this work employs the Foster thermal network.

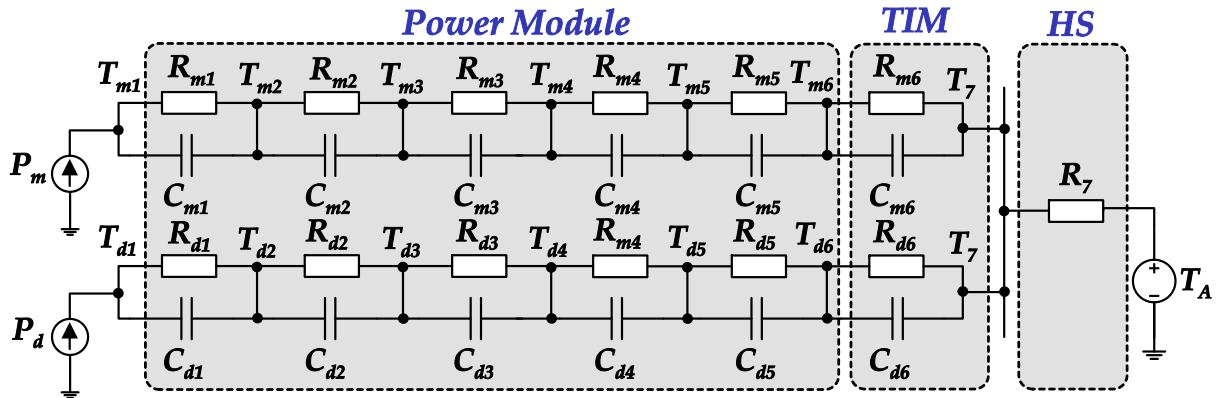


Figure 6.3: Foster type (Pi model) thermal network.

The self-heating state-space thermal model of the Foster network for the MOSFET and body diode is respectively given by (6.9) and (6.10). This model enables the MOSFET and diode junction temperatures (T_{m1} and T_{d1} , respectively) to be easily estimated and fed back into the various blocks used to calculate the individual losses.

$$\begin{cases} \frac{dT_m}{dt} = \begin{bmatrix} -\frac{1}{R_{m1}C_{m1}} & 0 & \cdots & 0 \\ 0 & -\frac{1}{R_{m2}C_{m2}} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -\frac{1}{R_{m6}C_{m6}} \end{bmatrix} T_m + \begin{bmatrix} \frac{1}{C_{m1}} & 0 & 0 \\ \frac{1}{C_{m2}} & 0 & 0 \\ \vdots & \vdots & \vdots \\ \frac{1}{C_{m6}} & 0 & 0 \end{bmatrix} U, \\ T_{m1} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} T_m + \begin{bmatrix} R_7 & R_7 & 1 \end{bmatrix} U. \end{cases} \quad (6.9)$$

$$\begin{cases} \frac{dT_d}{dt} = \begin{bmatrix} -\frac{1}{R_{d1}C_{d1}} & 0 & \cdots & 0 \\ 0 & -\frac{1}{R_{d2}C_{d2}} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -\frac{1}{R_{d6}C_{d6}} \end{bmatrix} T_d + \begin{bmatrix} 0 & \frac{1}{C_{d1}} & 0 \\ 0 & \frac{1}{C_{d2}} & 0 \\ \vdots & \vdots & \vdots \\ 0 & \frac{1}{C_{d6}} & 0 \end{bmatrix} U, \\ T_{d1} = [1 \ 1 \ 1 \ 1 \ 1 \ 1] T_d + [R_7 \ R_7 \ 1] U. \end{cases} \quad (6.10)$$

where $T_m = [T_{m12}, T_{m23}, T_{m34}, T_{m45}, T_{m56}, T_{m67}]^T$, $T_d = [T_{d12}, T_{d23}, T_{d34}, T_{d45}, T_{d56}, T_{d67}]^T$, and $U = [P_m, P_d, T_A]^T$. T_{mpq} and T_{dpq} respectively denote the MOSFET and body diode temperature difference across nodes p and q of the thermal network in Figure 6.3. From (6.9) and (6.10), the combined cross-coupling extended state-space can be derived and is given in (6.11), where $T_k = [T_m \ T_d]^T$.

$$\begin{cases} \frac{dT_k}{dt} = \begin{bmatrix} -\frac{1}{R_{m1}C_{m1}} & 0 & 0 & 0 & \cdots & 0 \\ 0 & \ddots & 0 & \vdots & \cdots & 0 \\ \vdots & 0 & -\frac{1}{R_{m6}C_{m6}} & 0 & \vdots & 0 \\ 0 & \vdots & 0 & -\frac{1}{R_{d1}C_{d1}} & 0 & \vdots \\ 0 & \cdots & \vdots & 0 & \ddots & 0 \\ 0 & 0 & \cdots & 0 & 0 & -\frac{1}{R_{d6}C_{d6}} \end{bmatrix} T_k + \begin{bmatrix} \frac{1}{C_{m1}} & 0 & 0 \\ \vdots & \vdots & \vdots \\ \frac{1}{C_{m6}} & 0 & 0 \\ 0 & \frac{1}{C_{d1}} & 0 \\ \vdots & \vdots & \vdots \\ 0 & \frac{1}{C_{d6}} & 0 \end{bmatrix} U, \\ \begin{bmatrix} T_{m1} \\ T_{d1} \end{bmatrix} = \begin{bmatrix} 1 & 1 & \cdots & 1 & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 1 & 1 & \cdots & 1 \end{bmatrix} T_k + \begin{bmatrix} R_7 & R_7 & 1 \\ R_7 & R_7 & 1 \end{bmatrix} U. \end{cases} \quad (6.11)$$

The time-domain equivalent thermal impedance of the MOSFET and body diode is determined using equation (6.12). It is important to note that to properly curve-fit the impedances, negative RC values may emerge. Although these don't pose mathematical difficulties, they can cause problems for circuit simulators. This can be resolved by employing positive RC values while subtracting the temperature contribution from that section of the RC circuit. Consequently, the Foster network won't have negative RC values, but a part with a negative temperature contribution [538]. Another approach to deal with negative RC values is to represent the thermal impedance in the frequency domain as given by (6.13), which represents the Foster model in partial fraction expansion form.

$$Z_{th(j-c)}(t) = \frac{T_j - T_c}{P_t} = \sum_{i=1}^n R_i \left(1 - e^{-\frac{t}{R_i C_i}} \right) \quad (6.12)$$

$$Z_{th(j-c)} = \frac{T_j - T_c}{P_t} = \sum_{i=1}^n \frac{R_i}{1 + s\tau_i}. \quad (6.13)$$

6.2.1.2 Passive Component Losses

Passive power losses primarily come from the equivalent series resistance (ESR) of the inductor and the ESR of input/output filter capacitors. The DC power losses across the inductor (P_{L-DC})

and the input/output filter capacitor (P_{C-DC}) are respectively given by:

$$P_{L-DC} = I_{L-RMS}^2 R_{L-DC} \quad (6.14)$$

$$P_{C-DC} = I_{Cin-RMS}^2 R_{Cin} + I_{Cout-RMS}^2 R_{Cout} \quad (6.15)$$

Using equations (6.8), (6.14), and (6.15), the approximate total converter losses can be evaluated from which the efficiency can be easily calculated as given in (6.16). The block diagram summarizing the whole efficiency computation process is given in Figure 4.

$$\begin{cases} P_{loss} = P_t + P_{L-DC} + P_{C-DC}, \\ \eta = \frac{P_{out}}{P_{out} + P_{loss}}. \end{cases} \quad (6.16)$$

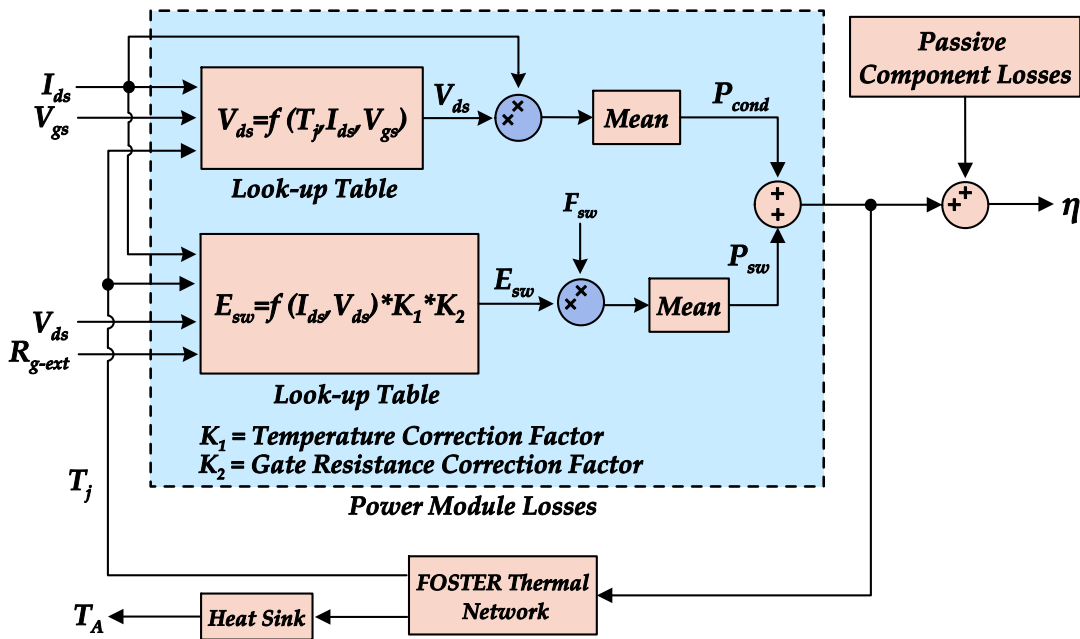


Figure 6.4: Block diagram of electro-thermal model for determining efficiency.

6.2.1.3 Thermal Model Validation

To verify the developed electro-thermal model, open loop simulations are performed in MATLAB/Simulink for different phase shifts, using the DAB converter specifications given in Table 4.6 and a $10\ \Omega$ resistive load. The results for a single switching device are compared with those obtained using PLECS in-built thermal analysis tool and are shown in Figure 6.5.

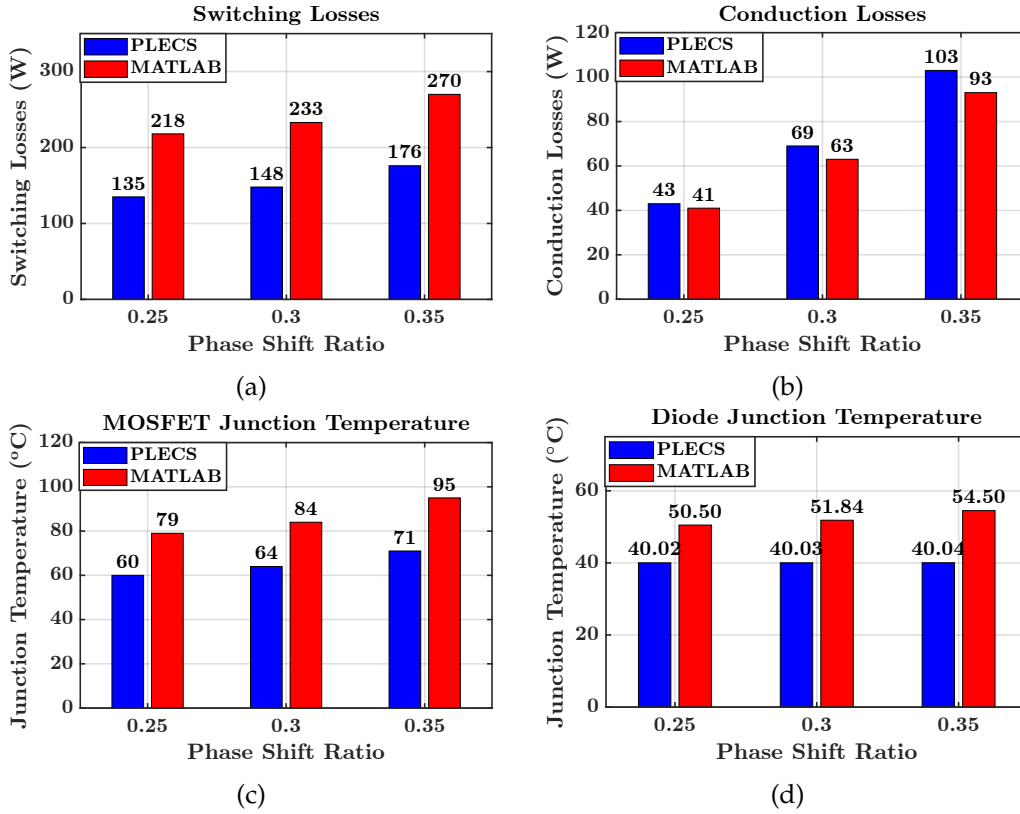


Figure 6.5: Thermal model comparative results: (a) Switching losses (b) Conduction losses (c) MOSFET junction temperature (d) Diode junction temperature.

Figure 6.5 shows that the conduction losses from both simulations are very similar, while the switching losses, MOSFET and diode junction temperatures show some little discrepancies with the MATLAB values typically higher than those from PLECS. These variations are considered acceptable and can be used to estimate the converter's efficiency, which will be useful in the proceeding sections.

6.2.2 Power Balance Decouple Control Strategy of Modular DAB Based on GAM

In this section, power sharing for a 3-module IPOP DAB is examined, beginning with the GAM model of a single DAB presented in Section 4.3.2, which yielded the state-space equations in equation (4.47). From this equation, the transfer function of the phase-shift to input current for a single module can be easily derived in the form shown in (6.17).

$$\begin{bmatrix} \hat{i}_g \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Q(s) & R(s) & T(s) \\ U(s) & V(s) & W(s) \end{bmatrix} \begin{bmatrix} \hat{\phi}_g \\ \hat{\phi}_b \\ \hat{\phi} \end{bmatrix} \quad (6.17)$$

If the first DAB module is set as the reference converter, then the perturbations in input current in any DAB module with reference to DAB module 1 can be obtained as:

$$\hat{i}_{gj} = T(s) (\hat{\phi}_j - \hat{\phi}_1) + \hat{i}_{g1} \quad (6.18)$$

Assuming that $\hat{i}_g = 0$, then $\sum_{j=1}^3 \hat{i}_{gj} = 0$. Using this, equation (6.18) becomes:

$$\hat{i}_{gj} = T(s) \left(\hat{\phi}_j - \frac{1}{3} \sum_{j=1}^3 \hat{\phi}_j \right) \quad (6.19)$$

Equation (6.19) can be written in the form of a matrix as follows:

$$\begin{bmatrix} \hat{i}_{g1} \\ \hat{i}_{g2} \\ \hat{i}_{g3} \end{bmatrix} = T(s) \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} \quad (6.20)$$

As already seen in the previous chapters, the battery charging strategy adopted in this work embeds the CC charging within the CV charging. It is therefore necessary to derive the small signal relationship between the output current and individual phase shifts. Assuming that $\hat{v}_g = 0$ and using equation (6.17), the following can be derived:

$$\hat{i}_o = W(s) \sum_{j=1}^3 \hat{\phi}_j \quad (6.21)$$

In order to uniformly distribute the input currents of an N -module DAB system, $N - 1$ input current control loops can be used in addition to the output current control loop. Considering the current scenario of 3 DAB modules, the matrix equation fulfilling these objectives can be derived from equations (6.20) and (6.21) as follows:

$$\begin{bmatrix} \hat{i}_{g1} \\ \hat{i}_{g2} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{2T(s)}{3} & -\frac{T(s)}{3} & -\frac{T(s)}{3} \\ -\frac{T(s)}{3} & \frac{2T(s)}{3} & -\frac{T(s)}{3} \\ W(s) & W(s) & W(s) \end{bmatrix} \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} = Q(s) \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} \quad (6.22)$$

As observed from (6.22), the controlled quantities and control variables form an interconnected MIMO system. To simplify this into a SISO system, decoupling is necessary. This can be accomplished by expressing $Q(s)$ as the product of two fictitious matrices, with one of them being a diagonal matrix, as shown in (6.23).

$$Q(s) = X(s)Y(s) = \begin{bmatrix} T(s) & 0 & 0 \\ 0 & T(s) & 0 \\ 0 & 0 & 3W(s) \end{bmatrix} Y(s) \quad (6.23)$$

Inserting equation (6.23) into equation (6.22) gives:

$$\begin{aligned} \begin{bmatrix} \hat{i}_{g1} \\ \hat{i}_{g2} \\ \hat{i}_o \end{bmatrix} &= \begin{bmatrix} T(s) & 0 & 0 \\ 0 & T(s) & 0 \\ 0 & 0 & 3W(s) \end{bmatrix} Y(s) \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} \\ &= \begin{bmatrix} T(s) & 0 & 0 \\ 0 & T(s) & 0 \\ 0 & 0 & 3W(s) \end{bmatrix} \begin{bmatrix} \Delta\hat{\phi}_1 \\ \Delta\hat{\phi}_2 \\ \Delta\hat{\phi}_o \end{bmatrix} \end{aligned} \quad (6.24)$$

The system in equation (6.24) can now be considered as three decoupled SISO systems where each controlled quantity depends only on a single control signal and each control signal affects only one controlled quantity. A new set of control variables is introduced such that the condition in (6.25) is satisfied.

$$Y(s) \begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} = \begin{bmatrix} \Delta\hat{\phi}_1 \\ \Delta\hat{\phi}_2 \\ \Delta\hat{\phi}_o \end{bmatrix} \quad (6.25)$$

From equation (6.23), matrix $Y(s)$ can be derived as:

$$Y(s) = X(s)^{-1}Q(s) = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \quad (6.26)$$

Using equations (6.26) and (6.25), the phase shifts can easily be derived from the new set of control variables as:

$$\begin{bmatrix} \hat{\phi}_1 \\ \hat{\phi}_2 \\ \hat{\phi}_3 \end{bmatrix} = Y(s)^{-1} \begin{bmatrix} \Delta\hat{\phi}_1 \\ \Delta\hat{\phi}_2 \\ \Delta\hat{\phi}_o \end{bmatrix} = \begin{bmatrix} \Delta\hat{\phi}_1 + \Delta\hat{\phi}_o \\ \Delta\hat{\phi}_2 + \Delta\hat{\phi}_o \\ -(\Delta\hat{\phi}_1 + \Delta\hat{\phi}_2) + \Delta\hat{\phi}_o \end{bmatrix} \quad (6.27)$$

From (6.24) and (6.27), the generalized decoupled three-loop power balance control diagram shown in Figure 6.6a is derived, which is equivalent to the configuration shown in Figure 6.6b. In Figure 6.6, the reference control signal P_t denotes the total input/output voltage/current mean values, which must be distributed across all modules, while P_k ($k = 1, 2, \dots, q$) denotes the measured input or output variable for each module. Details of these control signals are provided in Table 6.1.

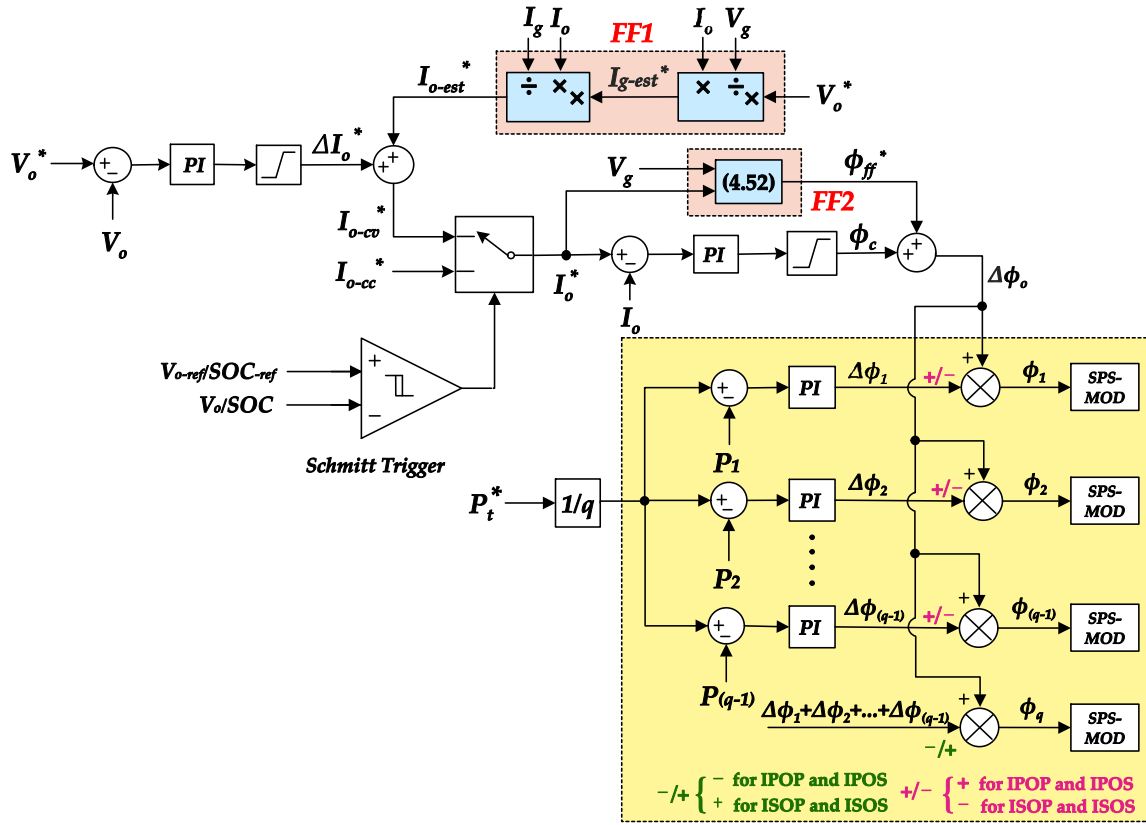
In Figure 6.6, two feedforward loops, FF1 and FF2, are included to enhance the system's dynamic response during the CC-CV battery charging process. These feedforward loops increase the system's resilience and robustness against input voltage fluctuations, load disturbances and other unforeseen disturbances. The expressions for these feedforward loops, derived in Section 4.4.1.1, are given in equations (4.51) and (4.57).

Table 6.1: Control Signal Representation for Modular DAB Systems

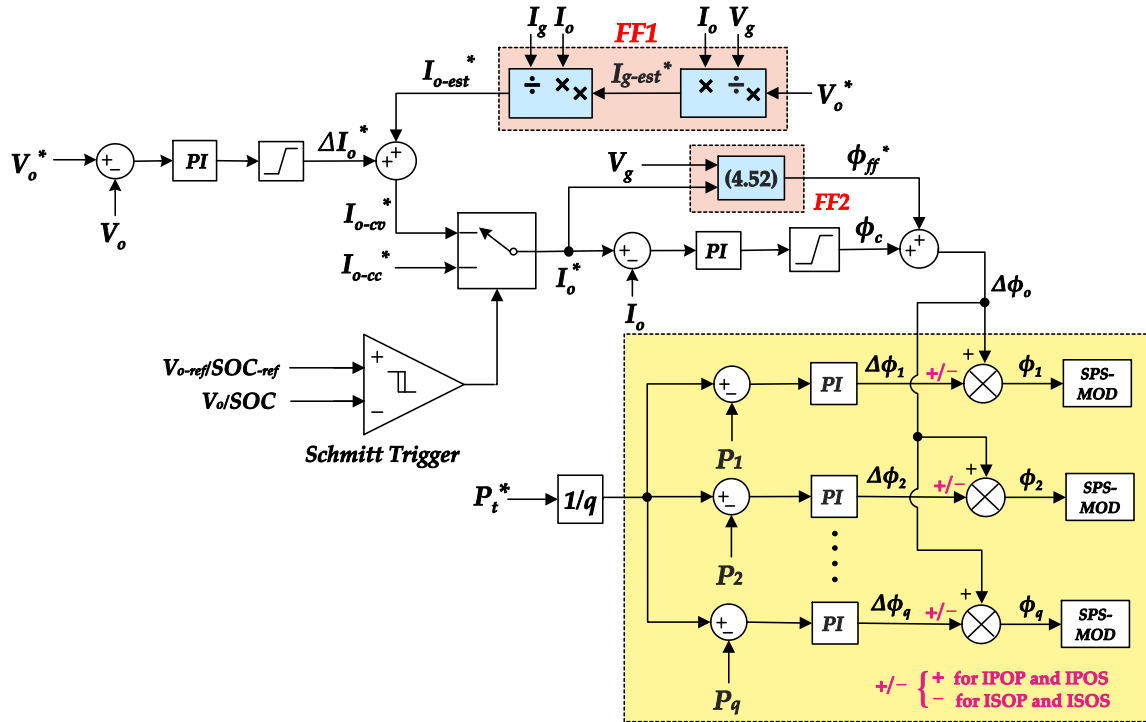
Configuration	$P_k (k = 1, 2, \dots, q)$	P_t
ISOP	V_{ink} or I_{ok}	V_{in} or I_o
ISOS	V_{ink} or V_{ok}	V_{in} or V_o
IPOP	I_{ink} or I_{ok}	I_{in} or I_o
IPOS	I_{ink} or V_{ok}	I_{in} or V_o

6.2.3 Comparative Results Through Numerical Simulations

By using the control diagram depicted in Figure 6.6, an IPOP modular SPS-modulated DAB-based battery charging system has been developed and implemented in MATLAB/Simulink following



(a)



(b)

Figure 6.6: Generalized power sharing control scheme for modular DAB converters (a) Decoupled triple-closed loop control strategy (b) Triple closed loop equivalent control strategy.

the specifications outlined in Table 6.2 for the various modular topologies shown in Figure 6.1. Moreover, the PI controllers are designed using MATLAB's `SISOTOOL`.

Table 6.2: Modular DAB converter System specifications

Paramater	Value
Input voltage (V_{in})	750 V
Battery nominal voltage (V_o)	900 V
Rated power per module (P_{rm})	85 kW
Number of modules	3
switching frequency (f_{sw})	100 kHz

The IPOP modular DAB converter's power balancing loop is first investigated with inductor and transformer parameter mismatches while charging the battery at a CC of 200 A, followed by CV of 900 V. The ICS power balancing scheme (PBS) is implemented to achieve power balance among the different modules. The results are shown in Figure 6.7, and it can be seen that in the absence of the PBS, i.e. when common phase shift angle control is used, the average input and output currents per module are significantly different. However, implementing the previously mentioned PBS results in equal average input and output current values in each module during each charging mode. A similar observation can be seen in Figure 6.8, where the actual output, input and inductor currents per module (zoomed in over two switching cycles) differ when common phase shift angle control is utilized but become balanced when the proposed PBS is applied.

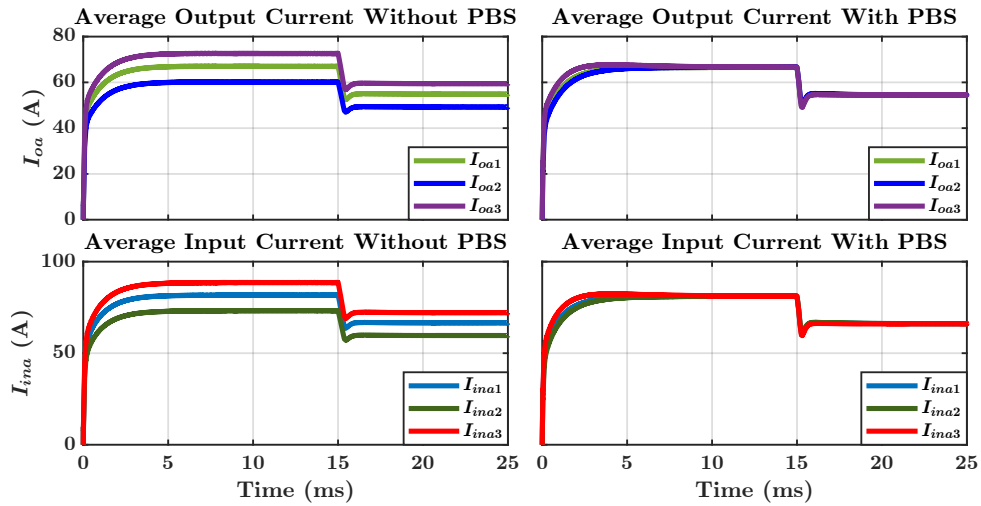


Figure 6.7: Average output current (**top**) and average input current (**bottom**) per module without (**left**) and with (**right**) PBS.

Figure 6.9 shows the RMS inductor current across different modular converter configurations when charging the battery initially at a CC of 200 A, followed by and a CV of 900 V. Throughout each charging phase, the peak and RMS inductor currents are highest with the ISOS topology, followed by ISOP, then IPOS, and lowest with the IPOP topology. This shows that circulation currents and reactive power backflow are greatest with the ISOS configuration and lowest with

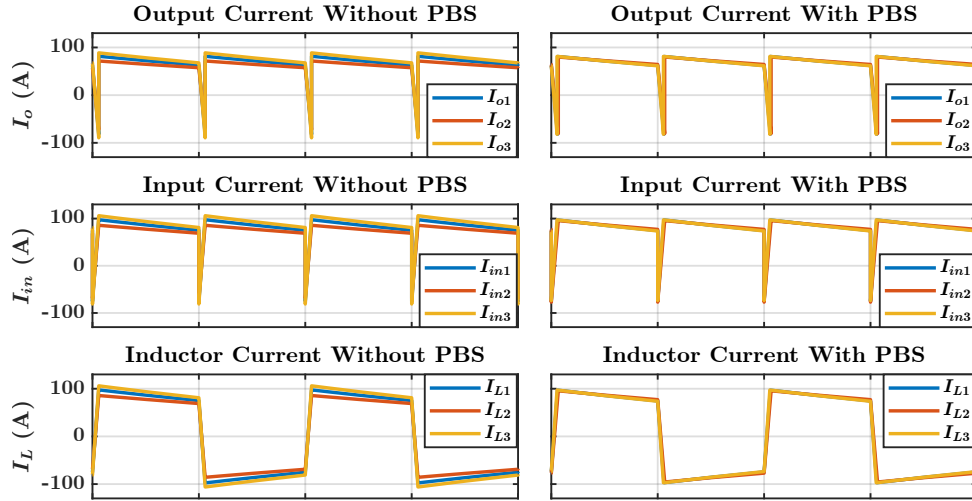


Figure 6.8: Output current (**top**), input current (**middle**) and inductor current (**bottom**) per module without (**left**) and with (**right**) PBS.

the IPOP topology for the same power demand.

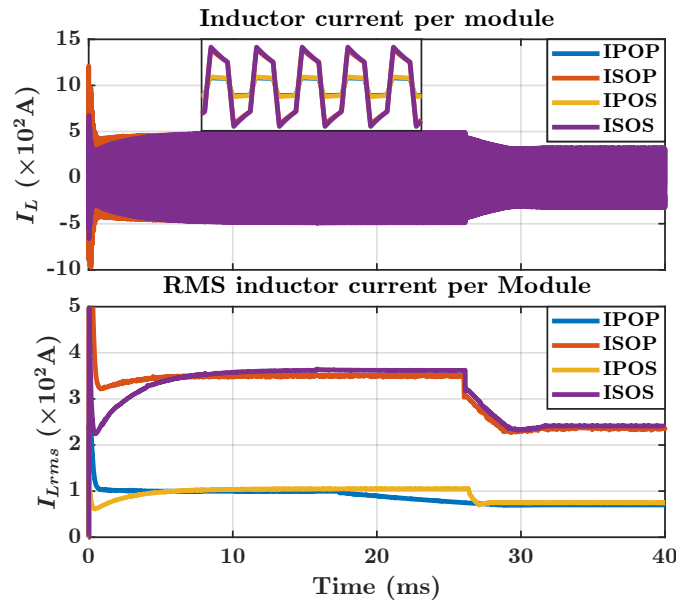


Figure 6.9: RMS inductor current in various modular DAB topologies.

It can be inferred from Figure 6.9 that because the ISOS topology has the highest reactive power circulation, its total power losses will be highest amongst other modular topologies with the least occurring when the IPOP topology is used, as confirmed in Figure 6.10 which shows the variation of total power losses across the different modular topologies during the charging process, where all converters operate at the same setpoint.

Since the IPOP converter has the lowest power losses, its efficiency is expected to be the highest, whereas the ISOS topology will exhibit the lowest efficiency. As shown in Figure 6.10, the IPOP converter achieves an efficiency of around 95.6% during the CC charging phase, but the ISOS topology has a steady state efficiency of only 84.1% at the same CC charging operating point. The converter's efficiency is not constant since the junction temperature rises constantly

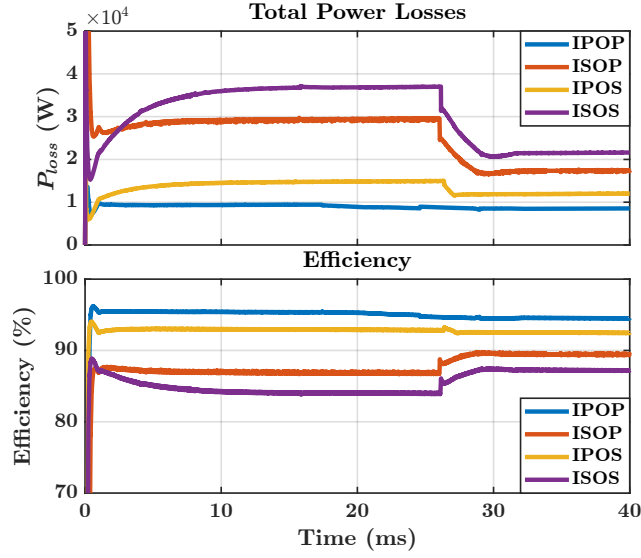


Figure 6.10: Total power losses (**top**) and efficiency (**bottom**) of various modular converters.

during operation, leading to a steady decrease in efficiency at any given operating point.

6.3 Dynamic Phase Shedding and Interleaving Approach for Modular DAB Converters

6.3.1 Fundamental Interleaving Concept in Modular DAB Converters

As discussed in Section 6.1, modular converters operating in high-power regions are frequently interleaved to increase the ripple frequency thereby reducing the stress on input and output filters and allowing smaller filters to be employed. Interleaving is achieved by applying a phase shift between each module. For a modular DAB converter, this phase shift is $180^\circ / q$, where q represents the number of modules connected in series or parallel at the input and output. By applying this phase shift across modules, the ripple frequency increases to $2qF_{sw}$, where F_{sw} is the converters' switching frequency.

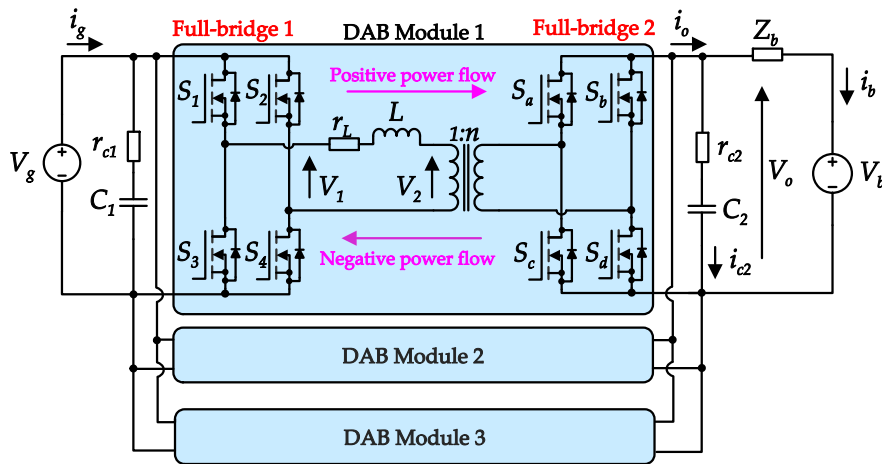


Figure 6.11: Modular IPOP DAB converter.

In this study, three DAB modules ($q = 3$) are employed in an IPOP configuration at full power as shown in Figure 6.11, resulting in a required phase shift of 60° between each module. To perform interleaving, the PWM switching pulses for the primary and secondary full bridges of DAB module 2 are phase-shifted by 60° , while those of DAB module 3 are phase-shifted by 120° . DAB module 1 acts as the reference module, hence no additional phase shift is applied to its full bridges. Consequently, the input and output filter capacitors observe a ripple current frequency of $6F_{sw}$ as shown in Figure 6.12, which reduces the input and output current ripple to one-third of the ripple seen at each individual DAB module's input and output.

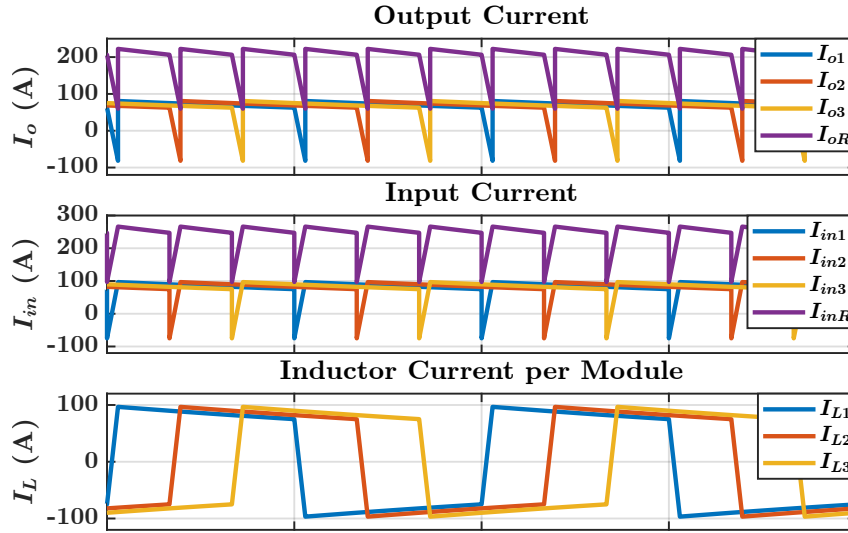


Figure 6.12: Interleaving principle in modular DAB converter.

6.3.2 Functioning of the Proposed Adaptive Phase Shedding and Interleaving Strategy

Figure 6.13 presents the power loss and efficiency curves for the DAB module with varying number of modules across different load conditions operating under SPS modulation. The points where these curves intersect represent the optimal threshold values, derived from the loss analysis outlined in Section 6.2.1, where the efficiency increases by adding or removing a module. The parameters used for computing the efficiency curves of the DAB module are listed in Table 6.3.

Figure 6.13 shows that using all three modules to charge the EV battery at high power yields high overall efficiency since the conduction losses, which are the primary source of losses, are minimized by evenly distributing the output current across all three phases. However, at light load, each module handles significantly smaller power, and if all three modules continue to operate, switching losses, reverse recovery-losses and inductor losses become more significant, leading to lower overall system efficiency. Therefore, selectively enabling or disabling phases in each module based on load conditions can improve efficiency.

In the conventional static phase-shedding and interleaving (SPS&I) control shown in Figure 6.14a, the first few phases of each DAB module remain active during light to medium load conditions, while other phases are switched ON or OFF depending on the load current. This

Table 6.3: DAB converter specifications for single module.

Parameter	Value
Input voltage (V_{in})	756 V
Battery nominal voltage (V_o)	900 V
Switching frequency (f_s)	100 kHz
Leakage inductance (L)	2.6 μ H
Rated Power per module (P_{rm})	850 kW
Parasitic resistance of inductor and transformer (r_L)	50 m Ω
Drain-source on resistance of MOSFET (R_{ds-on})	35 m Ω
Transformer turns ratio ($n_p : n_s$)	5 : 6
Output filter capacitor (C_{fo})	200 μ F
Input filter capacitor (C_{fi})	400 μ F
Filter capacitor ESR (r_c)	50 m Ω

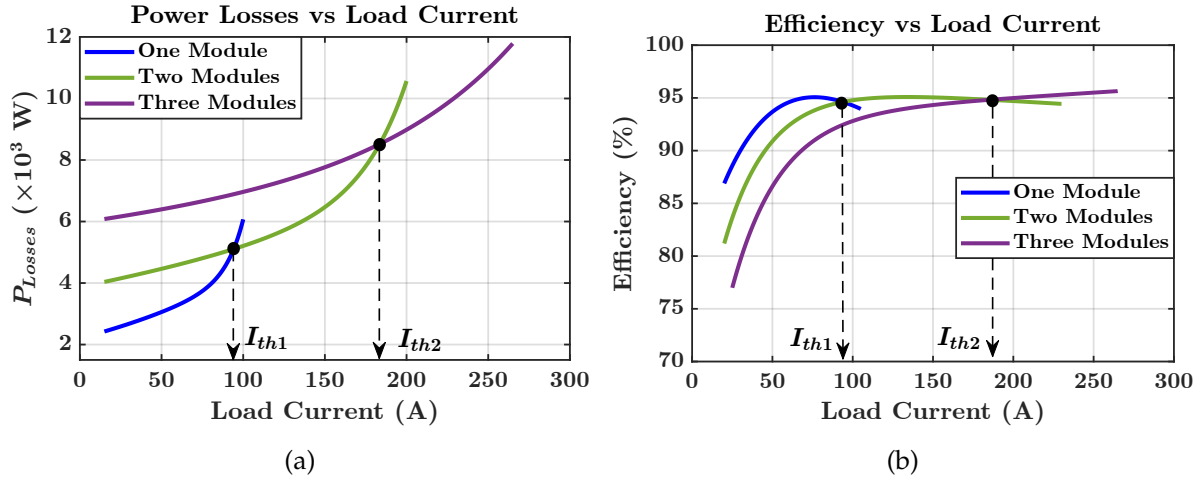


Figure 6.13: (a) Power losses and (b) Efficiency of IPOP DAB converter with different number of modules in operation.

results in uneven electrical and thermal stress among converter phases, which can reduce system reliability due to accelerated aging effects. Such aging can lead to inductor current imbalance, further decreasing efficiency and diminishing ripple cancellation. To extend the lifespan of the DAB switching devices and enhance the reliability of the battery charging system, it is crucial to avoid high electro-thermal stress. Hence, a rotational phase-shedding and interleaving (RPS&I) technique, as shown in Figure 6.14b, is adopted to evenly distribute electro-thermal stress across all modules under light, medium and heavy load conditions.

The proposed rotating module-shedding and interleaving control strategy is shown in Figure 6.15 and is based on the observations in Figure 6.13. The control system has three primary functions: CC-CV battery charging, which includes two feedforward loops (FF1 and FF2) to enhance the system's dynamic response, the OCS loop for module power balancing, and a function block that executes the adaptive rotational module-shedding and interleaving algorithm. The suggested phase-shedding method aims to reduce total power losses while enhancing

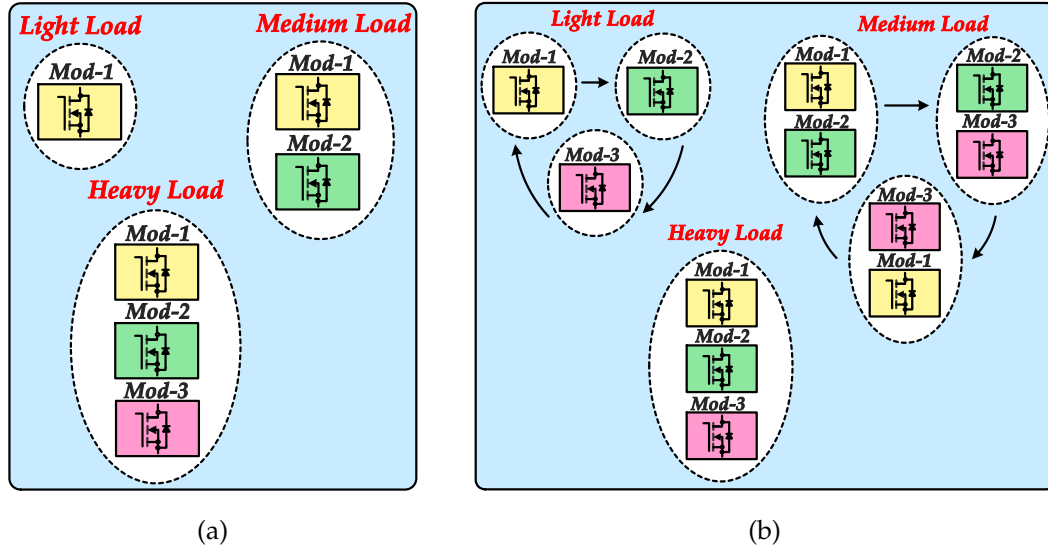


Figure 6.14: (a) Static phase shedding technique (b) Rotational phase shedding technique.

efficiency by dynamically adjusting the configuration of active phases. The feedforward loop expressions, as derived in Section 4.4.1.1, are provided in equations (4.52) and (4.58).

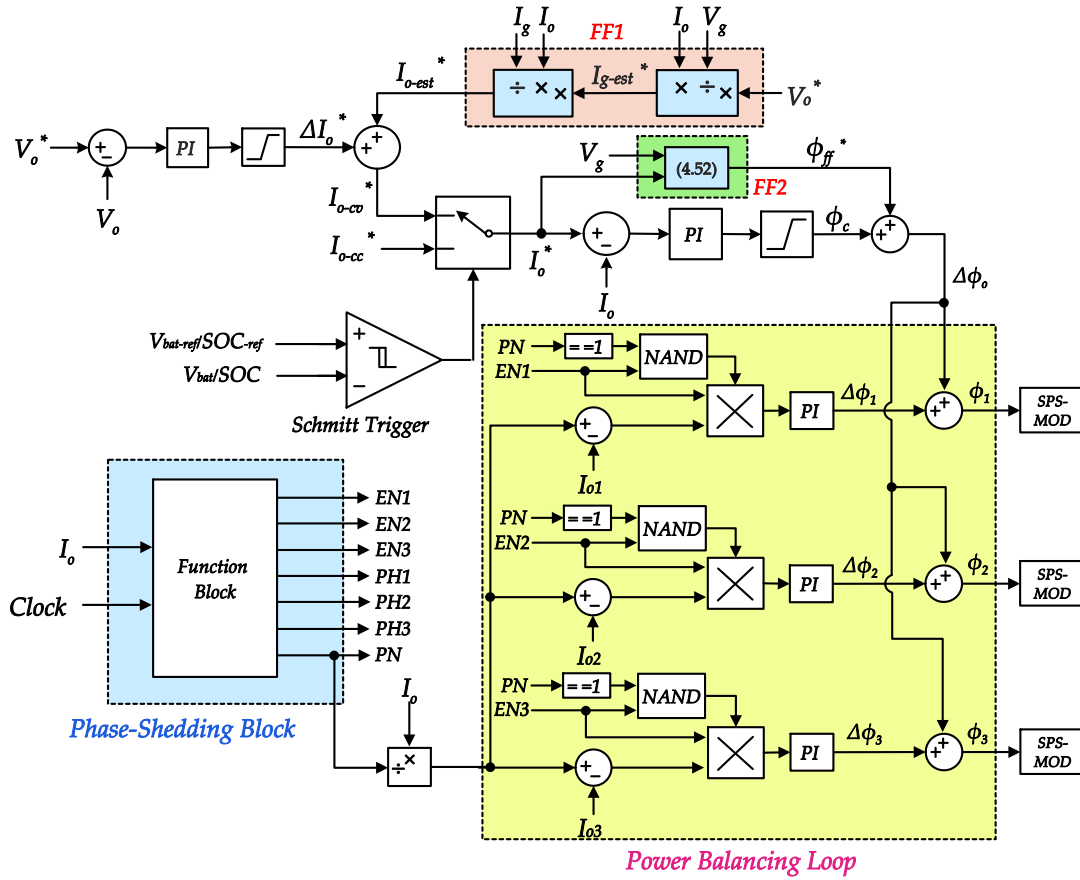


Figure 6.15: Schematic diagram of proposed module shedding and interleaving control alongside power balance and battery charge control.

From the offline loss analysis, the optimal load current threshold values (I_{th1} and I_{th2}) are

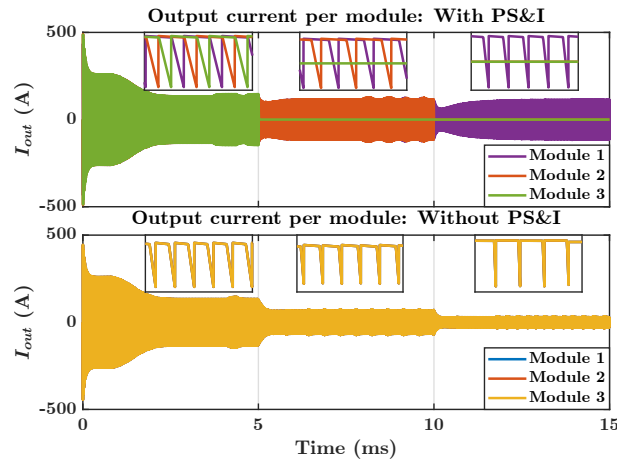


Figure 6.17: Output current per module with and without module shedding and interleaving.

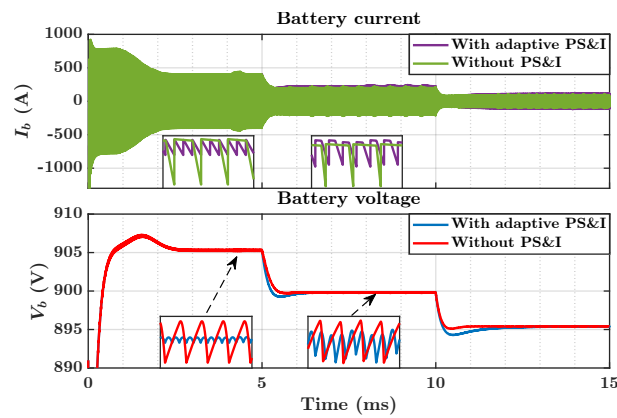


Figure 6.18: Battery current and voltage with and without module shedding and interleaving.

Figure 6.18 shows the effect of interleaving on battery current and voltage responses. As observed, the static PS&I technique, reduces peak-peak current and voltage ripples since the ripple frequency is three times greater than without the PS&I algorithm during the first period of operation and two times higher during the second phase. According to Figure 6.19, employing this PS&I technique results in an increase in operation efficiency across the converter's entire operation range as compared to not using it.

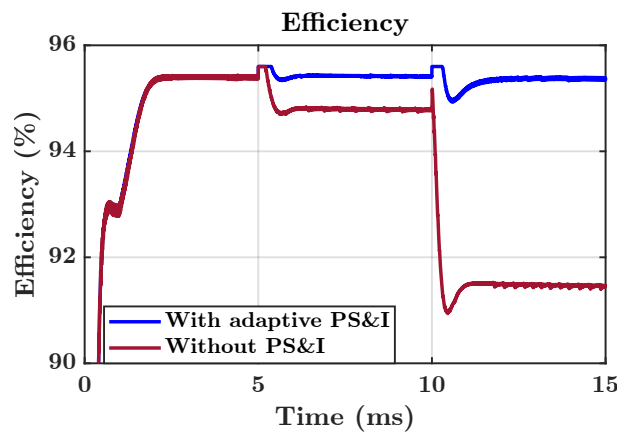


Figure 6.19: Overall system efficiency with and without module shedding and interleaving.

The proposed rotational PS&I scheme is tested by charging the battery at three CC values: 160 A, 260 A and 80 A, as shown in Figure 6.20. During the first 20 ms, the battery current is controlled at 260 A and two modules operate at medium load. Moreover, module enabling and disabling occurs every 5 ms as observed in the small overshoots found in the magnified segment of the figure.

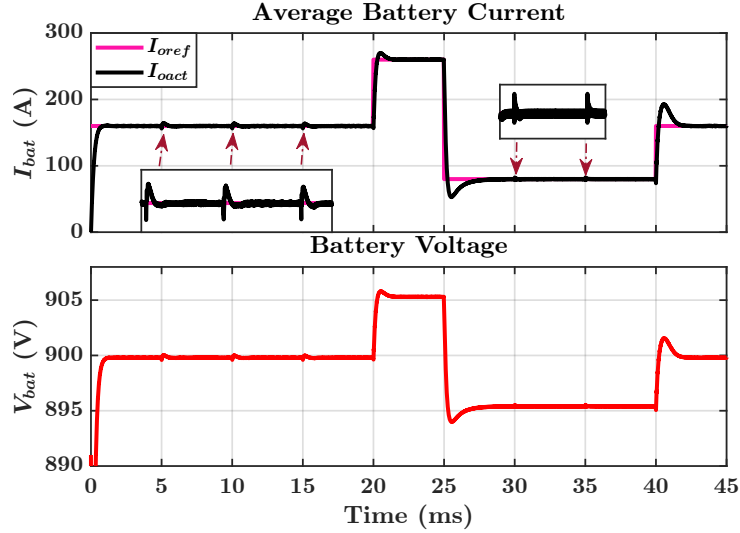


Figure 6.20: Average battery current (**top**) and battery voltage (**bottom**) during RPS&I.

Figure 6.21 shows that in the interval 0 – 5 ms, only modules 1 and 2 operate; in the interval 5 – 10 ms, only modules 2 and 3 operate; in the interval 10 – 15 ms, only modules 3 and 1 operate and the cycle repeats in the interval 15 – 20 ms. Figure 6.21 also shows that during this first 20 ms period, the currents of the active modules remain balanced, even with parameter mismatches, ensuring equal power sharing. Furthermore, the two active modules are interleaved for ripple reduction, as shown in the inductor current waveforms in Figure 6.22.

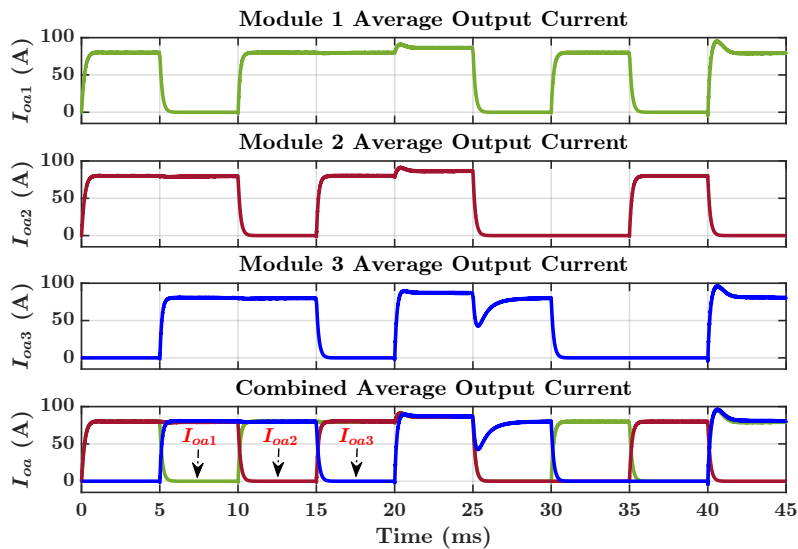


Figure 6.21: Average output current per module during RPS&I.

At the end of the medium load phase, the control switches to charging the battery at CC of 260

A in the interval 20 – 25 ms as shown in Figure 6.20. Since this is a heavy load scenario, all three modules are enabled, as observed in Figure 6.21, and the power balancing loop also guarantees that the currents in all three modules are of equal magnitude. Moreover, the appropriate phase-shift is applied to these three modules to enable ripple minimization through interleaving, as can be seen in the corresponding period in Figure 6.22.

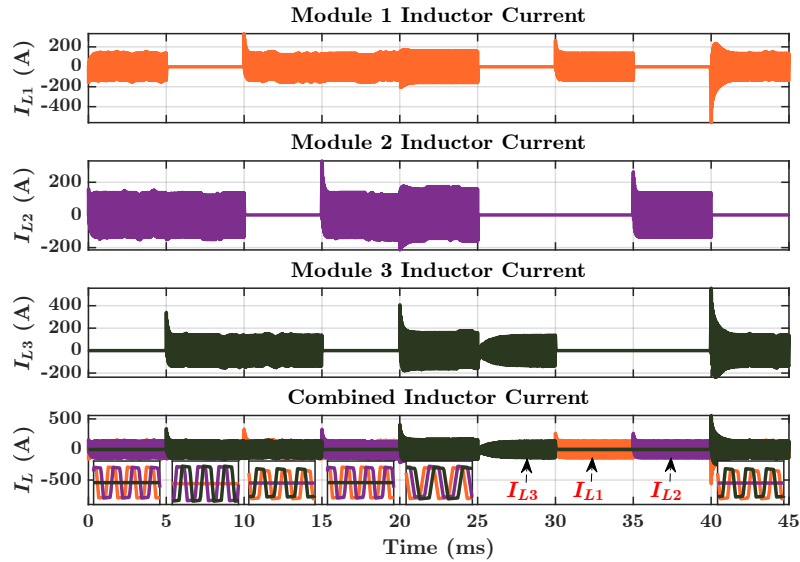


Figure 6.22: Inductor current per module during RPS&I.

At $t = 25$ ms, the control changes to CC of 80 A. This being a light load condition means that only one module is required to achieve maximum operational efficiency. Therefore, module connection and disconnection occur every 5 ms, as observed in the interval 25 – 40 ms. Since only one module works throughout this time, no phase interleaving can be performed. In the interval 40 – 45 ms, battery charging returns to a CC of 160 A, requiring only two modules, and the control logic disconnects module 2 and re-activating modules 1 and 3, with phase interleaving again applied as observed in Figure 6.22.

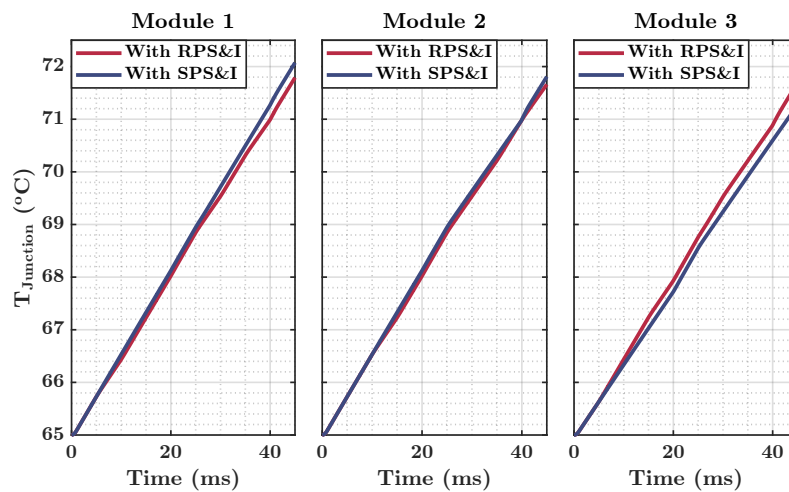


Figure 6.23: Junction Temperature evolution across modules with RPS&I and SPS&I schemes.

The small overshoots visible in Figure 6.20 can be decreased further by reducing the time

constant of the exponential enabling signal adopted in this work, as well as by properly tuning the controller. On the other hand, huge overshoots in the actual inductor currents seen in Figure 6.22 can be reduced by applying suitable soft start and soft shutdown techniques.

Figure 6.23 shows that applying the RPS&I scheme helps to reduce the junction temperature rise across modules 1 and 2 in comparison to the case with SPS&I. Even though module 3 shows a higher temperature with RPS&I, this is just because of the manner in which the simulations were carried out since module 3 works alternately at all load conditions in the RPS&I scheme whereas it works only in the medium and heavy load conditions in the SPS&I scheme.

6.4 Sensor Reduction Technique in Modular DAB Battery Charging System

6.4.1 Proposed Control Strategy

The sensor reduction approach is based on the use of a LESO to estimate the battery current using information from already measured state variables. The LESO starts with the output capacitor's voltage derivative dynamic equation, which is based on applying KCL to the modular IPOP converter's output stage, as seen in Figure 6.24. This equation is given by (6.28).

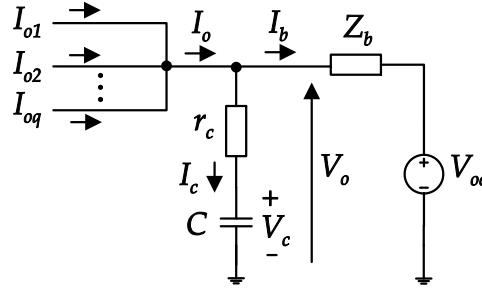


Figure 6.24: Equivalent circuit of output stage of IPOP DAB converter.

$$\begin{aligned} \frac{dV_c}{dt} &= \frac{I_o}{C} - \frac{I_b}{C} \\ &= \frac{V_{in}}{2nf_s C} \sum_{m=1}^q \frac{D_m(1-D_m)}{L_m} + F \end{aligned} \quad (6.28)$$

Where $D_m = \frac{\phi_m}{\pi}$ and $F = -\frac{I_b}{C}$. This study focuses on a three-module IPOP DAB system, thus $q = 3$.

The small-signal form of the capacitor voltage derivative in (6.28) can be expressed as shown in (6.29).

$$\frac{d\hat{V}_c}{dt} = b\hat{u} + \hat{F} \quad (6.29)$$

where $b = [b_1, b_2, b_3]$ and $\hat{u} = [\hat{d}_1, \hat{d}_2, \hat{d}_3]'$, with $b_j \forall j \in [1, 3]$ defined as:

$$b_j = \frac{V_{in} D_j (1 - 2D_j)}{2nf_s C L_j} \quad (6.30)$$

In (6.29), $\hat{V}_c$ is considered as a state variable and represented as $x_1 = \hat{V}_c$, while $\hat{F}$ is taken as an augmented state variable expressed as $x_2 = \hat{F}$. Moreover, the time derivative of x_2 is denoted by h . Based on this analysis, the state-space model derived from (6.29) is given in (6.31), where g is a 1×3 zero vector.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b \\ g \end{bmatrix} \hat{u} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h \quad (6.31)$$

The conventional LESO can be constructed from (6.31) as follows:

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} b \\ g \end{bmatrix} u + \begin{bmatrix} n_1 \\ n_2 \end{bmatrix} [x_1 - z_1] \quad (6.32)$$

where z_1 and z_2 are respectively the estimated values of x_1 and x_2 , while $[n_1, n_2]^T$ is the Luenberger observer gain vector, designed using the pole placement method as described in Section 4.4.2.1. The estimated battery current, I_{b_est} , is then computed from z_2 as $I_{b_est} = -Cz_2$.

The error state-space equation can be derived by subtracting (6.32) from (6.31), yielding the following:

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} -n_1 & 1 \\ -n_2 & 0 \end{bmatrix}}_T \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h \quad (6.33)$$

According to control theory, the matrix T will be Hurwitz stable if all the roots of its characteristic polynomial, $\lambda(s)$, lie in the left half-plane. If the ESO poles are designed to be all positioned at $-\omega_o$ (ω_o is the observer bandwidth), expression (6.34) is obtained, from which the observed gains can be derived as $n_1 = 2\omega_o$ and $n_2 = \omega_o^2$.

$$\lambda(s) = |sI - A| = s^2 + sn_1 + n_2 \equiv (s + \omega_o)^2 \quad (6.34)$$

The standard LESO described above assumes that the system disturbance is constant, but in reality, it varies over time due to large changes in the plant model, leading to considerable estimation errors of the system states and disturbances. Moreover, the time delays produced by signal transmission lead to extra estimation errors [539].

To better predict x_2 and, consequently, the battery current, an enhanced ESO is proposed, as shown in (6.35), which introduces a new fictitious variable k_2 to provide an initial estimate of x_2 and subsequently z_2 to supplement k_2 and provide a more accurate estimate of x_2 .

$$\begin{cases} \dot{z}_1 = k_2 + n_1(x_1 - z_1) + bu + M, \\ M = \rho_1(u(t) - u(t-h)) + \rho_2(x_1(t) - x_1(t-h)), \\ \dot{k}_2 = n_2(x_1 - z_1), \\ \dot{z}_2 = k_2 + \rho_3 x_1 + \frac{d^\mu(x_1 - z_1)}{dt^\mu} + n_1(x_1 - z_1) \end{cases} \quad (6.35)$$

In (6.35), $h > 0$ is a constant artificial delay chosen arbitrarily to ensure the exponential stability of the error dynamics. Properly tuning the parameters ρ_1 , ρ_2 , and ρ_3 significantly enhances the observation performance. The gains n_1 and n_2 are the same as in the traditional ESO.

Furthermore, the proposed improved ESO incorporates a fractional-order derivative (FOD) operator, s^μ . Implementing FODs involves considerably higher computational complexity than integer-order transfer function models due to their irrational nature. Therefore, FODs are typically approximated by higher-order rational transfer functions, which maintain a constant phase curve within a specific frequency range. Numerous strategies for implementing FODs in both frequency and time domains have been proposed in the literature [540].

In this study, Carlson's method derived from the regular Newton iterative process has been selected to implement the FOD found in the enhanced ESO and is presented next. Let $G(s)$ be a rational function and $H(s)$ be a fractional-order transfer function, where $H(s) = [G(s)]^r$ and $r \in \mathbb{R}$. $H(s)$ can then be recursively approximated as given in (6.36).

$$\begin{cases} H_i(s) = H_{i-1}(s) \frac{G(s) + p[H_{i-1}(s)]^x}{pG(s) + [H_{i-1}(s)]^x}, \\ \text{where } p = \frac{1-r}{1+r}, x = \frac{1}{r}, H_0(s) = 1 \end{cases} \quad (6.36)$$

In this work, the first-order derivative is considered in (6.35), hence $\mu = 1$. As a result, s^1 is implemented using (6.36) by expressing it as $s^1 = s^{0.5}s^{0.5}$, where $r = 0.5$ and $G(s) = s$. The approximation performance can be considerably improved by increasing the number of iterations since the ripples in both the phase and magnitude responses are significantly reduced as shown in Figure 6.25.

The limitation of the Carlson method is that x can only have integer values, i.e., $x \in \{\pm 2, \pm 3, \pm 4, \dots\}$, hence, it is not possible to obtain the approximate transfer function of $[G(s)]^r$ directly $\forall r \in (0, 1)$.

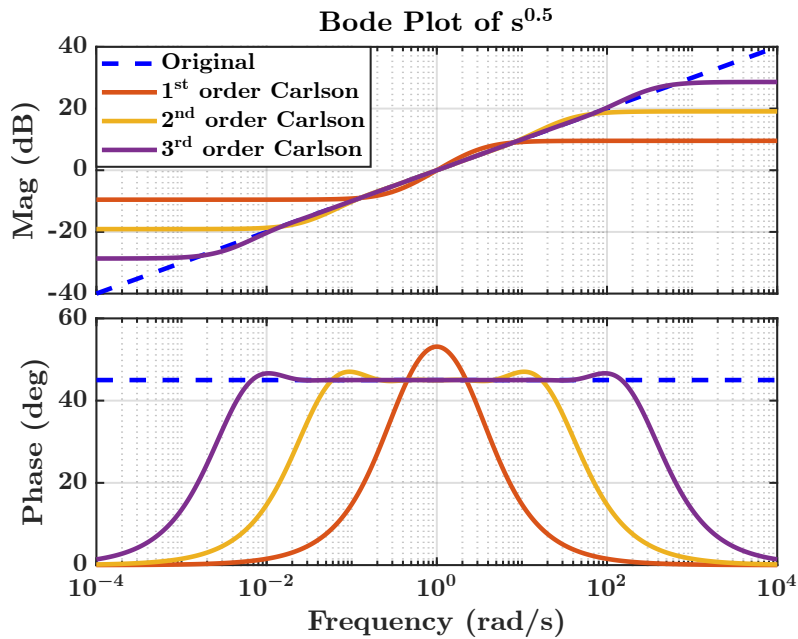


Figure 6.25: Bode diagram of first, second and third order Carlson approximation of $s^{0.5}$.

Figure 6.26 shows the proposed enhanced ESO-based sensor reduction control scheme for battery charging consisting of two feedforward loops (FF1 and FF2) for dynamic performance enhancement and an OCS loop performing power balancing.

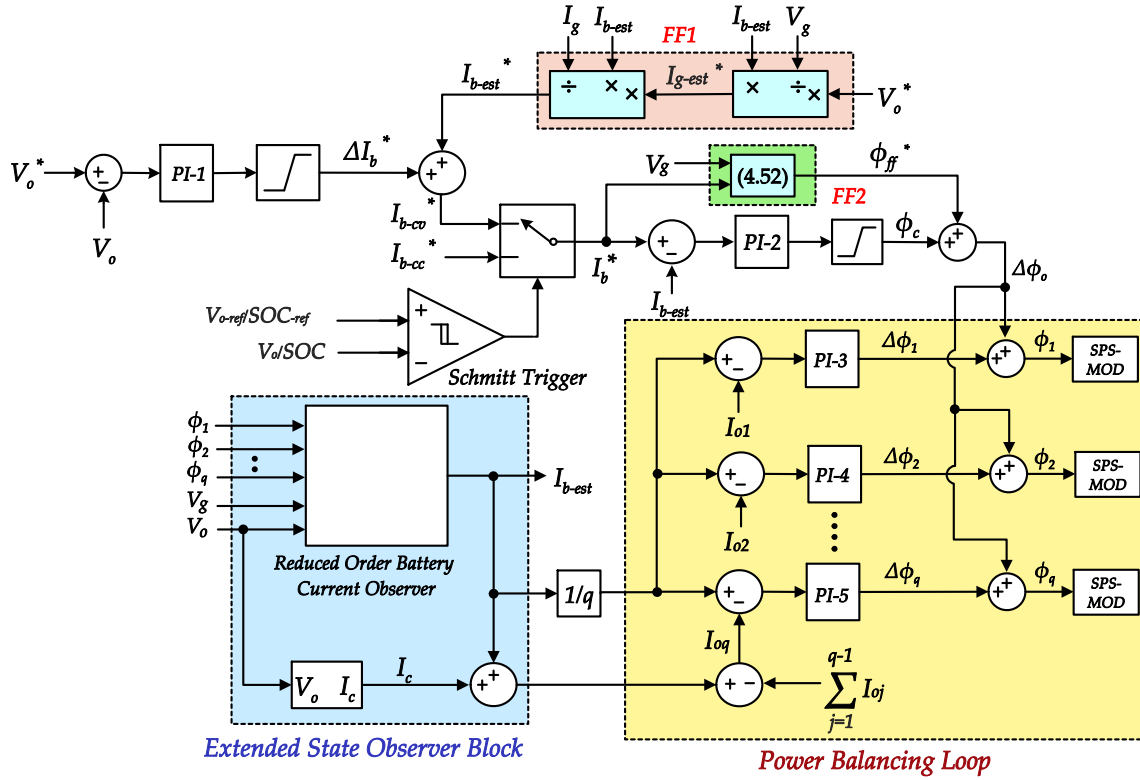


Figure 6.26: Proposed Sensor reduction technique for modular IPOP DAB converter.

6.4.2 Numerical Validation

MATLAB/Simulink is used to demonstrate the effectiveness of the proposed control scheme present in Figure 6.26. The DAB specifications and controller parameters are the same as those outlined in Sections 6.3.2 and 6.3.3 respectively. The observer bandwidth is chosen to be 6×10^4 rad/s.

The proposed ESO and feedforward control techniques are verified in the presence of small variations in inductor and transformer parameters while charging the battery at a CC of 200 A and then CV of 900 V. Figure 6.27 shows the results for both the conventional ESO and the proposed ESO, along with the effects of the proposed feedforward system on the battery charging system's dynamic performance.

Figure 6.27a reveals that the current estimation error during the CC charging stage is 5.5 A with the conventional ESO, which decreases significantly to roughly 0.5 A when the suggested enhanced ESO is used. It is also noticed that during the CV stage, the Luenberger-based conventional ESO has an estimation error of 3.6 A, which is reduced to 0 A by the suggested ESO. Additionally, the switch from CC to CV charge mode requires around 4 ms with the conventional ESO, whereas this time reduces to just 2 ms with the proposed ESO. Thus, the implementation of the proposed LESO drastically decreases the current estimation error (Δi_b) and shortens the transition time (Δt) from CC to CV charging mode while maintaining inductor current balance in each DAB module, as observed in Figure 6.27b. Furthermore, feedforward compensation independently minimizes the current dips during the CC-CV transition for both the conventional and proposed ESOs.

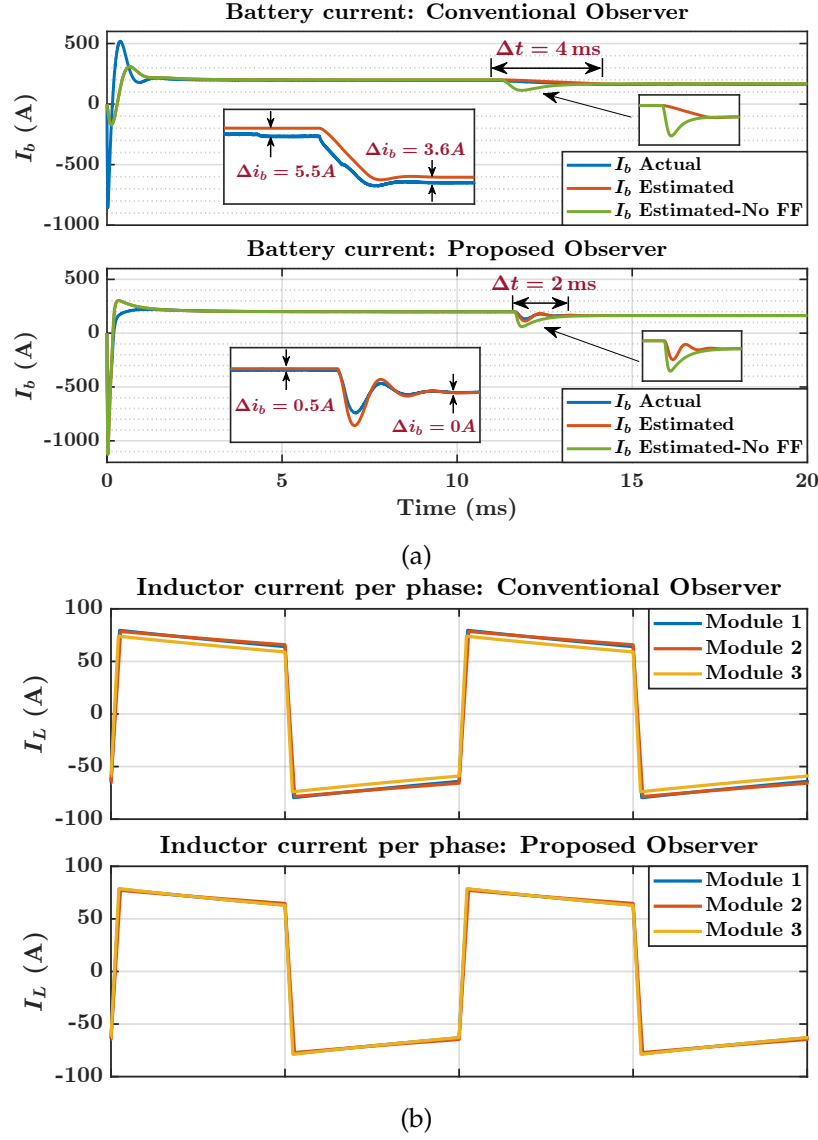


Figure 6.27: (a) Battery current with proposed and conventional observer (b) Inductor currents with proposed and conventional observer.

6.5 Conclusion

This chapter presented the performance of various modular DAB topologies for high-power EV battery charging in Section 6.2 beginning with proposing and developing an electro-thermal model which was used for module junction temperature estimation and efficiency determination. Following this, a generalized control scheme for modular DAB converter was introduced, derived from the DAB converter's GAM. This generalized control scheme improves module stability and reliability as power balance across modules is ensured at all times. Simulations revealed that the IPOP converter outperforms the other three modular topologies, achieving the highest efficiency, lowest power losses, and lowest circulation current when operating under the same conditions with SPS modulation. In terms of control complexity, the ISOS topology is the most challenging, followed by ISOP, IPOS and finally IPOP.

To further improve modular converter efficiency during light to medium loads, both rotational

and static phase-shedding and interleaving schemes were implemented. As was seen, the RPS&I technique demonstrated an advantage in reducing thermal stress and wear on the converter by evenly distributing operating time across all modules, a feature lacking in the conventional SPS&I scheme. In any case, both schemes aid in enhancing converter efficiency while minimizing current and voltage ripples.

Finally, a LESO was presented in Section 6.4 to estimate battery current in modular systems, which improves observation performance by incorporating a fractional-order term and state delays to better handle variable system disturbances. As a result, this LESO design offers greater flexibility, significantly reducing current estimation error compared to the typical LESO. The enhanced LESO also enhances dynamic response speed, while the presented feedforward control mitigates current undershoots. Overall, the enhanced ESO-based battery charging system is quite robust to system parameter variations and provides fast disturbance estimation and elimination. Additionally, the proposed ESO-based control strategy allows for the elimination of two sensors, thus saving costs.

Chapter 7

Conclusions

7.1 Introduction

Beginning with a comprehensive literature review of ESSs used in EVs in Chapter 2 as well as the different power electronic converter architectures and topologies used in EV charging stations in Chapter 3, this work has explored and addressed some key problems in the modelling, design, control, and operation of the DAB converter for high-power EV charging applications. The research has considerably advanced various elements of DAB-based EV battery charging systems such as improving dynamic response during high-power charging, minimizing component stress for increased reliability, and optimizing modular architectures for scalable deployment.

This chapter provides a summary of the findings and main contributions in Section 7.2 as well as proposes possible areas of improvement for future work in Section 7.3. Finally, Section 7.4 provides a final perspective on the overall impact of the research carried out in the context of EV deployment.

7.2 Summary of Findings and Main Contributions

This thesis has made substantial contributions in multiple areas, from advanced DAB modeling to innovative control strategies and efficiency optimization. Each of these contributions has been developed to address specific challenges in high-power DC-DC conversion using the DAB converter for EV charging, and are summarized below:

7.2.1 Comprehensive Modeling of the DAB Converter System

- ◆ Developed a detailed second-order Thevenin model for battery representation and parameter extraction. This is crucial for high-accuracy simulations and control design, particularly under varying charging conditions.
- ◆ Enhanced the DAB converter's GAM by incorporating parasitic resistances of the output filter capacitor, which are typically neglected but shown to significantly impact the converter's dynamic behavior.

7.2.2 Innovative Control Strategies

- Introduced a cascaded two-loop control system integrating feedforward and PI control, demonstrating improved robustness against input voltage disturbances and load variations and helping to provide a smooth transition from CC to CV during the battery charging process thus improving the state of health of the battery.
- Proposed and analyzed novel model-independent LADRC-based robust control methodologies and its non-linear variant (NLADRC) to address limitations in conventional PI-based controllers such as poor disturbance rejection, complicated design process and susceptibility to system parameter variations.
- Proposed droop-based LADRC techniques to ensure smooth transitions between CC and CV charging modes, enhancing system stability and robustness across all operating points.
- Proposed an improved NLADRC utilizing sigmoid functions, and validated to outperform conventional LADRC in handling non-linearities, parameter variations, and both variable and unknown disturbances.
- An enhanced LESO was proposed incorporating fractional-order terms and state delays, achieving superior observation performance and disturbance rejection, better battery current estimation accuracy and sensor cost reduction in modular systems.

7.2.3 Dynamic Optimization in DAB Control

- Explored the use of vector control techniques to decouple orthogonal current components, providing independent and precise power flow and reactive power control.
- Utilized Fourier series-based frequency-domain methods for optimizing phase shift angles in DPS-modulated DAB converters, thus simplifying power flow control and minimizing reactive power compared to conventional time-domain piecewise approaches.

7.2.4 Modular Converter Efficiency and Reliability

- Proposed and validated electro-thermal models for DAB converters, enabling accurate junction temperature estimation and efficiency calculations.
- Conducted a comparative analysis of modular DAB topologies, identifying the IPOP configuration as the most efficient in terms of power losses, circulation current, and thermal performance.
- Introduced innovative phase-shedding and interleaving techniques (RPS&I) to improve efficiency and reduce thermal stress during light-to-medium load conditions.
- Proposed a generalized modular control scheme ensuring power balance and stability across DAB converter modules, contributing to enhanced system reliability.

7.2.5 Practical Implications for EV Charging

- It was demonstrated that the proposed control strategies are robust to wide voltage and current variations in EV battery systems and compatible with diverse battery models.
- Finally, this work addressed challenges of controller tuning in noisy environments by suggesting optimization algorithms (e.g. genetic algorithms) and advanced ESO techniques to balance noise reduction and estimation accuracy.

7.3 Possible Improvements and Future Directions

From the research carried out in this thesis, there exist possibilities to extend the work done and improve its applicability. Some of the further research directions which have been identified are summarized below:

7.3.1 Controller Optimization

Adaptive and learning-based tuning methods like reinforcement learning can be implemented to dynamically adjust control parameters in real-time, thus improving adaptability to evolving EV battery technologies.

7.3.2 DAB Converter Scalability and Modularity

Further studies on modular DAB systems should focus on hybrid interconnection strategies combining the strengths of ISOS, ISOP, IPOS and IPOP configurations to achieve optimal efficiency and reliability in ultra-fast charging networks.

7.3.3 Enhanced Thermal Management

More advanced thermal management techniques, including active cooling and real-time thermal balancing, could be incorporated to extend the lifespan of power modules and improve system reliability.

7.3.4 EV Battery Cell Balancing and Integration to BMS

Future research should explore energy-efficient, dynamic, and modular cell balancing techniques. Moreover, the integration of cell balancing with SOC estimation in a unified BMS algorithm will optimize both functions in real-time, thus ensuring better performance and longevity of the battery system.

7.3.5 Experimental Validation

Conduct large-scale hardware prototyping and testing under real-world conditions to validate the proposed control and design strategies and fine-tune them for practical deployment.

7.4 Final Remarks

The results presented in this thesis considerably advance the field of DAB converters for EV fast charging, offering innovative modeling approaches, optimized control strategies, and practical design solutions. By addressing key challenges such as efficiency, dynamic performance, and robustness, this work lays a strong foundation for the development of next-generation EV charging infrastructure. The proposed solutions not only enhance the viability of EVs by improving charging efficiency and reducing costs but also contribute to the broader goal of sustainable transportation. Future research should expand on these contributions to further implement and optimize DAB-based systems for a greener, more electrified future.

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