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Power Management Circuits for Ultra Low-Power Systems

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Abstract

The demand for portable electronic equipments is increasing in day-to-day life and it spans over an unbounded number of applications, from consumer electronics (smartphones, laptops, etc.), to biomedical electronics (wearable and implantable devices), till sensor networks (WSN and IOT devices). These systems, which are inherently mixed-signal systems, require minimum power consumption to extend the device life-time and reduce the size and weight of the battery.

Reducing power consumption extends the device life-time, but cannot guarantee the complete independence of portable electronic systems. Therefore, Energy Harvesting techniques, which aim to collect energy from the surrounding environment, have emerged as valuable alternative for charging or power supplying of low-power (LP) and ultra low-power (ULP) circuits. The power management section for LP and ULP battery-assisted systems should be designed to both limit power consumption and recover the environmental energy, so as to maximize the autonomy of portable electronic systems.

This thesis focuses on the study of the power management for low-power and ultra low-power systems and the design and implementation of a radio frequency (RF) harvester and a ULP programmable voltage reference.

In particular, a survey of the RF electromagnetic field power availability in different environments has been carried out to assess whether this source can recharge or directly supply ultra low-power integrated sensor nodes. The measurement campaign has confirmed that the RF field is ambient-dependent, not controllable and not predictable. However, the survey has also demonstrated that a sizeable RF energy level is available in some of the investigated environments and could be harvested to recharge a low-power sensor node.

Based on these measurements, an RF harvester circuit (HarvIC) has been designed and implemented in ST 65 nm CMOS technology for the power management of an integrated temperature sensor with analog-to-digital converter. The results of transistor-level simulation show that the implemented RF harvester architecture can be effectively used to recover energy in at least two of the investigated environments.

Within the power management subsystem, ULP bandgap circuits must guarantee good performance in terms of temperature coefficient and reference accuracy, with power consumption not exceeding few nanowatts. Moreover, systems on chip require different values of biasing voltages (e.g. to implement low-power design techniques), hence the possibility to program the voltage reference, with limited power consumption, could drastically extend the versatility and the applicability of the bandgap circuit in ULP systems. Based on the above observations, an

innovative ULP bandgap circuit, called PVREF (Programmable Voltage REFerence), has been designed and implemented in TSMC 55 nm CMOS technology. PVREF provides four voltage references, with power consumption of few nanowatts, while guaranteeing large reference programmability and requiring limited silicon area. The PVREF circuit can be considered a cross-over between ultra low-power voltage references and programmable voltage references, with remarkable performance compared with the state-of-the-art of both classes of circuits.
The novel subsystems described in this thesis, HarvIC and PVREF, contribute to the current design trend toward more efficient and smarter power management systems for ULP devices. Moreover, their design, as reported in this dissertation, shows the importance of careful analog circuit design techniques in order to obtain extreme performance levels.

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Chapter 1

Introduction

The computational capacity and the integration capability of Systems On Chip (SOC) have exponentially increased following one of the most durable technology forecast: Moore's Law [1]. The law states that the complexity of a circuit, measured as the number of transistors per chip, doubles every 18 months. Formulated in 1965, it is still valid today. This enormous increase in computational capacity has opened the way to the distributed technology era, but in recent years some limitations are arising. Indeed, MOS device scaling directly lowers the power consumption of digital circuits, but its effect on the analog circuits is much more complicated. Despite the drastic reduction of its application fields in the last fifty years, analog electronics remains the way to interact with the real world, and sensing interfaces will still require for decades high-performance analog circuits [2]. Therefore, decreasing the power consumption of analog circuits without affecting their performance has become an important research topic.

Today, the demand for portable electronic equipments is rising in everyday life and it spans over an almost unbounded number of applications, from consumer electronics (smartphones, laptops, etc.), to biomedical electronics (wearable and implantable devices), till sensor networks (WSN and IOT devices). These systems, which are inherently mixed-signal systems, demand minimum power consumption to extend the device life-time and reduce the size and weight of the battery. In order to limit the

power consumption of these circuits, several strategies can be applied at the different design layers. Thick-oxide and Silicon On Insulator (SOI) technologies aim to limit the leakage currents in the physical junctions. Semiconductor manufacturing companies provide, in some technology nodes, devices with scaled voltage thresholds, allowing the reduction of the power supply with no effect on the transistor performance. The availability of devices with different voltage thresholds permits different voltage supplies across the chip, acting on the power consumption at system level.
Duty-cycle sensor systems support the periodical disabling of entire chip sections and the shutting off of the current consumption by means of power gating [3]. Design techniques such as weak inversion and body bias, operating at transistor level, can also be used to limit the power consumption in the analog domain [4], [5].
Reduction of power consumption permits the extension of the life-time of portable devices, but cannot guarantee the complete independence of these systems. Therefore, Energy Harvesting techniques, which aim to collect energy from the surrounding environment, have emerged as valuable alternative for charging or power supplying of low-power (LP) and ultra low-power (ULP) circuits [6]. Summarizing, the power management section for LP and ULP battery-assisted systems has to be design to both limit the power consumption and recover the environmental energy.
This thesis focuses on the design and implementation of the power management for low-power and ultra low-power systems. In particular, a survey of the radio frequency (RF) electromagnetic field power availability in different environments has been carried out to assess whether this source can recharge or directly supply ultra low-power integrated sensor nodes [7]. Based on the data from the measurements, an RF harvester circuit, embedded in the HarvIC integrated circuit, has been designed and implemented in ST 65 nm CMOS technology for power management of an integrated temperature sensor with analog-to-digital converter. The cascade of an AC-DC converter and a DC-DC boost converter is used, combined with an antenna, to collect the environmental RF field and recharge the accumulator which supplies power to the sensor node.
The measurement campaign has confirmed that the RF field is ambient-dependent, not controllable and not predictable, therefore HarvIC integrates a Maximum Power

Point searching and Tracking system (MPPT) relying on a novel three dimensional search algorithm, to adapt the system to mutable environments and exploit the most promising RF source [8].
At the time of this writing (October 2018) HarvIC is being fabricated. The results of the post-layout simulation, in terms of sensitivity and end-to-end power conversion efficiency, show that the proposed RF harvester architecture can be effectively used in at least two of the investigated environments. Moreover, the MPPT system allows the RF harvester adaptation to mutable environments, drastically expanding its application space, with a negligible impact on the overall power consumption.
In the power management section, bandgap circuits have a fundamental role, providing voltage references constant over temperature. ULP applications, such as sensor nodes or implantable devices, require ULP bandgap circuits, which therefore have become a pressing research topic in analog electronics. ULP bandgap circuits have to guarantee good performance in terms of temperature coefficient (TC) and reference accuracy, with power consumption of few nanowatts. Moreover, systems on chip require different values of biasing voltages (e.g. to implement low-power design techniques), hence the possibility to program the voltage reference, with limited power consumption, can drastically extend the application field of ULP bandgap circuits.
Given the fundamental role of bandgap circuits in power management of ULP systems, in this thesis a novel, advanced programmable voltage reference has been designed. The circuit, called PVREF (Programmable Voltage REFerence), is embedded in the NAMPIC integrated circuit (also currently under fabrication), and has been designed and implemented in TSMC 55 nm CMOS technology. PVREF provides four voltage references, with power consumption of few nanowatts and large reference programmability, while requiring limited silicon area. The system can be considered a cross-over between ultra low-power voltage references and programmable voltage references, with remarkable performance compared with the state-of-the-art of both classes of circuits. PVREF has been designed to be integrated in the power management of ULP systems, with a large range of potential applications from wearable and implantable devices to sensor nodes.

This thesis is organized as follows. In Chapter 2 the surveying of different environments in terms of RF power availability is described and analyzed.
In Chapter 3 an analysis of the ultra low-power RF source is reported, and the architectures of the RF harvester and of the MPPT system, integrated in the HarvIC system, are presented. The RF harvester simulated performance is given and compared with the performance of state-of-the-art RF harvester architectures.
Chapter 4 describes the PVREF circuit architecture and it provides post-layout simulations results. PVREF performance indices are here compared with the performance of state-of-the-art ULP voltage references and of state-of-the-art programmable voltage references. Finally, conclusions are presented in Chapter 5.
Appendix A reports the testing strategy for the RF Harvester and its implementation.

Chapter 2

RF Energy Harvesting Survey

Recovery of the environmental energy by means of electronic circuits (Energy Harvesting) so as to provide power supply to low-power devices is one of the major research topics in integrated electronics [9], [10]. The possibility to extend the standalone lifetime of the electronic devices, recharging the power supply accumulator whenever energy is available without a dedicated source, makes this technology suitable for a wide range of applications, such as Wireless Sensor Nodes (WSN) and Internet of Things (IoT).

Among the available energy sources, the radio-frequency (RF) electromagnetic field is an attractive option bearing some advantages compared with other sources. The RF field does not imply a thermal gradient, like in thermoelectric harvesters, which has detrimental impact on the electronic device performance. Moreover, this source is available in both indoor and outdoor environments and it does not require movements or a friction (like electro-mechanic and piezoelectric harvesters) that may shorten the device lifetime. The RF energy can be classified as ambient-dependent, non-controllable and non-predictable [11]. Therefore, the prior study of the RF power distribution in the environment is the basis for a fruitful design of an RF harvester circuit. Metrics like *Sensitivity* (S_{IN}) of the front-end and *Power Conversion Efficiency* (η_{TOT}) are critical and must be optimized to exploit the radio-frequency source.

For example, it has been shown that in the underground stations of a densely popu-

lated and strongly developed urban area such as London or Boston, the RF field can be a competitive harvesting source in terms of recovered DC power, compared with other scavenging techniques, such as thermal human or vibration [10, 12]. However, little information is available on RF energy availability in many other environments. As preliminary step toward the desing of RF harvester, this thesis reports long-term measurements performed by means of a commercial multi-band dipole array antenna in three different environments (here defined as urban, semi-urban and rural) of a limited area in Northern Italy. The aim of this measurement campaign is to verify whether the ambient RF power in a variety of locations can be an effective source for an RF energy harvester.

2.1 Radio-frequency power survey

In order to assess the possibility to exploit the RF electromagnetic field as harvesting source, measurements of RF power availability have been performed in three generic, different environments: a university campus (Parma, Italy), an urban environment (Reggio Emilia, Italy), and a rural location near a small village in the Appennini mountains (Valestra, Italy). These locations mainly differ in the number of nearby transmitting elements and in the density of buildings or natural obstacles that can cause multipath effects, attenuation, and diffraction in the propagation of the RF waves. The urban environment hosts a large number of transmitting elements and is characterized by the high density of buildings, whereas the evaluated rural environment is isolated and surrounded by mountains. The university campus is located midway between the town and the countryside and it can be defined as semi-urban, considering the proximity to many transmitting elements and the scattered locations of buildings.
Maps of the three places which have been considered for the measurements are shown in Fig. 2.1. The position and relative distance of the closest transmitting base-stations (mobile phones networks) are highlighted in the maps [13].

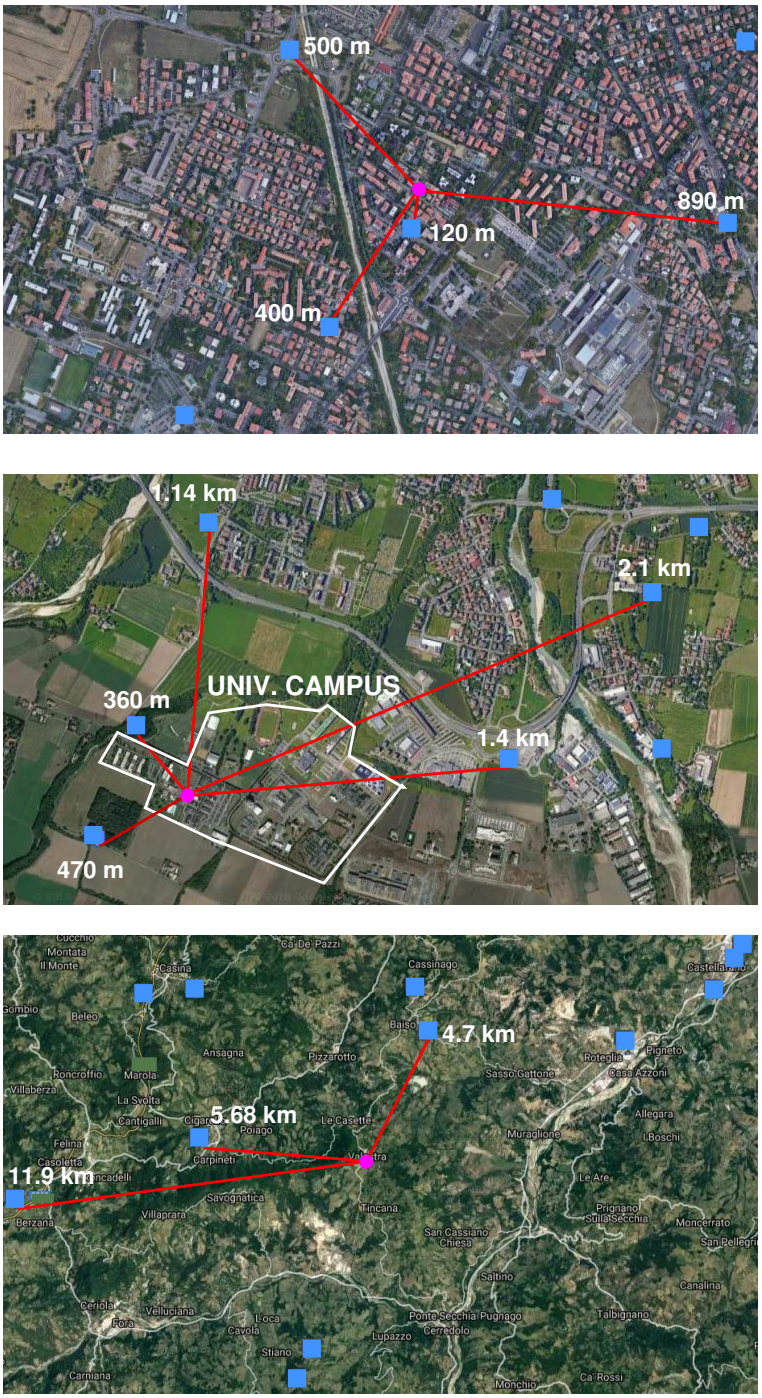

Figure 2.1: Maps of the considered environments. Magenta circle: RX antenna; light-blue rectangles: transmitting base stations in the surroundings; white labels: distance between base station and RX antenna. From top to bottom: Urban environment, University Campus, and Mountain-rural location.

2.1.1 Measurement methodology and setup

Starting from [10, 14, 12], which report results of RF surveys in urban and semi-urban scenarios in Europe, Asia, and USA, and from the mapping of the main transmitting base-station in the considered environments [13], the mobile telephone bands, including, among others, GSM-900, GSM-1800, UMTS (3G), and LTE-2600, have been identified as the most promising ones for RF energy harvesting.
RF power measurements in the UHF range, i.e. from 600 MHz to 2.6 GHz, have been carried out using an Anritsu MS2721B Spectrum Analyzer with an HGO - 4G LTE omnidirectional antenna. The gain of the dipole array G_{ANT} is approximately 5.5 dBi on every investigated sub-band. Recordings were periodically collected by means of a LabVIEW acquisition software. The so acquired measurements have been normalized in order to get an antenna gain of 0 dBi on every sub-band and cable losses have been de-embedded to finally attain the available RF power (P_{AV}). Each fast sequence of measurements on the sub-bands was separated by a time span of some minutes. Since long-term measurements aim at the characterization of the RF ambient power distribution over time, data acquisitions have lasted almost 24 hours in urban and rural locations, and around 6 hours in the semi urban environment. Measurements have been recorded during sunny days.

2.1.2 Results and Evaluations

Two examples of the RF power measurements are shown in Fig. 2.2 and Fig. 2.3. The measured available power spectral density S_{AV} vs. time in urban environment is shown for the 700 MHz to 1 GHz (Fig. 2.2) and the 1.8 GHz to 1.9 GHz (Fig. 2.3) bands.The 700 MHz to 1 GHz band, here labeled GSM-900, is mainly used for the 900 MHz GSM cellular phone communication, while the higher one, labeled GSM-1800, is used for the 1.8 GHz GSM.
In order to obtain the power that can be harvested over each bandwidth, the effect of the matching network placed in between the antenna and the harvesting circuit (i.e. receiver) must be considered. Such circuit is needed to achieve power matching between the source (antenna) and the receiver circuit.

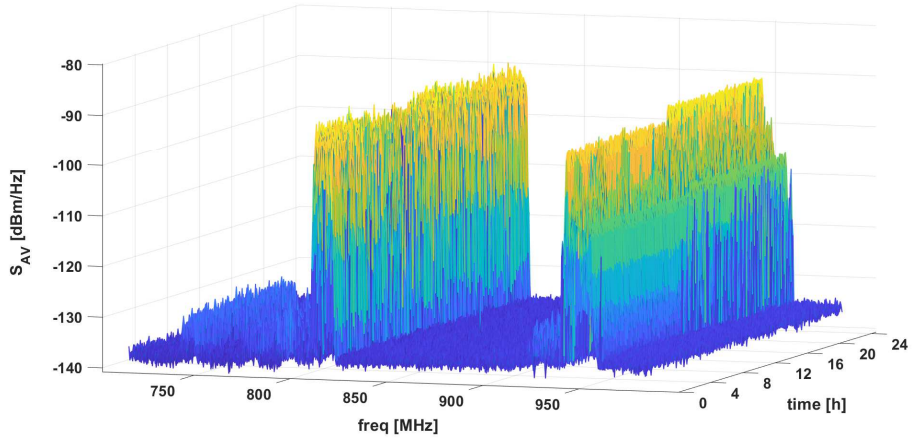

Figure 2.2: Spectral density of the available RF power vs. time in urban environment, over the 900 MHz band.

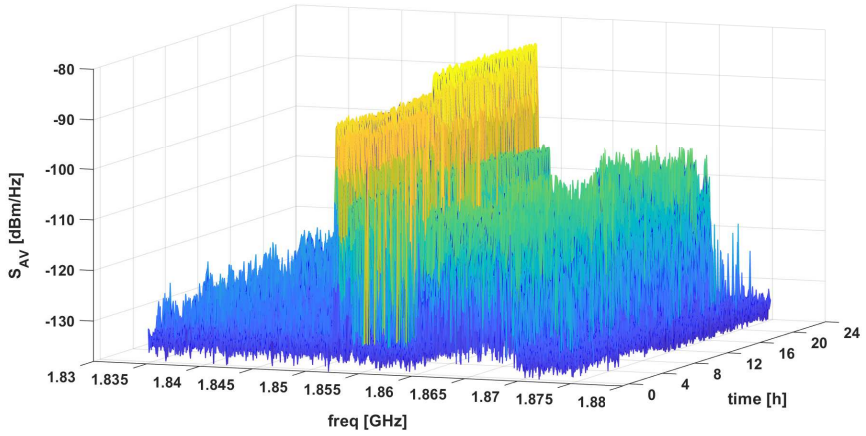

Figure 2.3: Spectral density of the available RF power vs. time in urban environment, over the 1.8 GHz band.

The combination of the antenna, matching circuit, and harverster circuit can be mod-

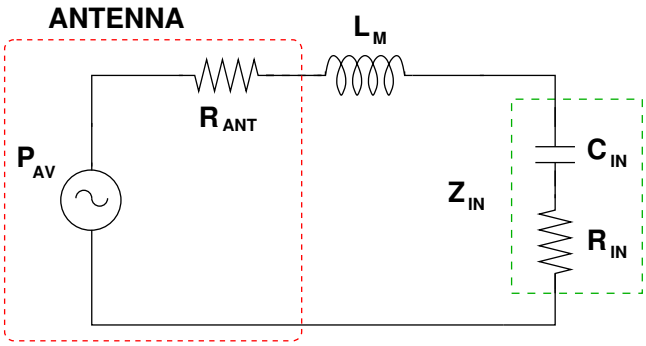

Figure 2.4: *R-L-C* series circuit modelling the matching circuit between antenna and an integrated RF front end.

eled with a *R-L-C* series resonator (Fig. 2.4), with resonance (i.e. center) frequency f_0 and peak-quality factor Q_{LC}:

$$f_0 = \left(2\pi\sqrt{L_M C_{IN}}\right)^{-1} \tag{2.1}$$

$$Q_{LC}(f_0) = \frac{1}{2\pi f_0 C_{IN}\,(R_{IN} + R_{ANT})} \tag{2.2}$$

where C_{IN} and R_{IN} are the input capacitance and resistance of the RF front-end and L_M models the matching inductance. It is worth to mention that this model holds over a relatively small bandwidth across f_0.

The available power which can be collected by a receiver circuit (i.e. P_{AV}) is obtained by integrating the measured power spectral density in Figs. 2.2 and 2.3 over the bandwidth with the specific transfer function, H_{LC} in Fig. 2.5, of the resonator:

$$H_{LC}(\omega) = \frac{\left(\dfrac{\omega}{\omega_0 \cdot Q_{LC}} + 1\right) \cdot Q_{LC}}{\dfrac{\omega^2}{\omega_0^2} + \dfrac{2 \cdot \omega}{\omega_0 \cdot Q_{LC}} + 1} \tag{2.3}$$

$$P_{AV}(f_0) = \int_{f_{min}}^{f_{max}} S_{AV}(f) \cdot H_{LC}(f_0, f)\ df \tag{2.4}$$

The power effectively collected by the receiver circuit, P_{IN}, being equal to P_{AV} under power-matching condition, depends on the value of Q_{LC} and of the center frequency

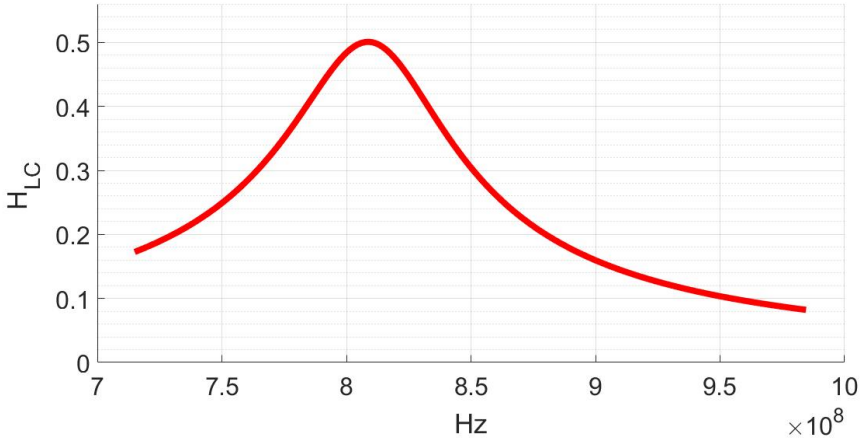

Figure 2.5: Transfer function of the resonator circuit with $f_0 = 810$ MHz

of the equivalent resonator. Tab. 2.1 shows the maximum and average P_{IN} values in long-term recordings for the evaluated scenarios and for three bands of interest: GSM-900, GSM-1800, and LTE. These data have been obtained considering a quality factor $Q_{LC} = 25$ and an optimized center-tuning frequency f_0, in order to extrapolate the maximum harvestable power from each frequency band. The gain of a typical planar antenna ($G_{ANT} \approx 2$ dBi [15, 16]) should be added to the power values in Tab. 2.1.

The lower band clearly overcomes in terms of power availability all the other bands, across the whole day, in two of the three locations. It has to be noticed that the optimum tuning frequency is not constant across space due to different network infrastructure managers. However, two stable peaks centered at about 815 MHz and 940 MHz have been recorded in the urban environment (Fig. 2.2).

The non-predictability of the RF source over time is confirmed by the large standard deviation σ. In Fig. 2.6 the value of P_{IN} vs. time for a full day of recording is shown for both 900 MHz and 1800 MHz bands in the urban environment. Measurements show a sudden increase of the available power at the beginning of the working day.

Table 2.1 shows the large gap between the urban and semi-urban environments and the rural one. Indeed the amount of harvestable RF power is heavily affected by the

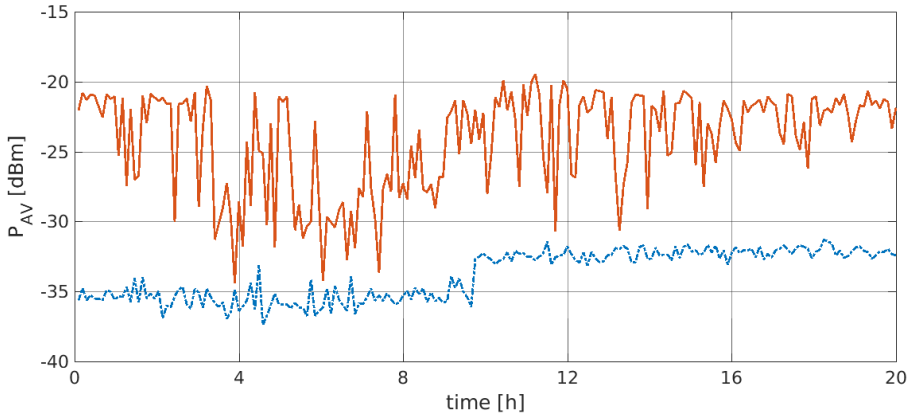

Figure 2.6: Variation of P_{AV} during the day in urban environment, for GSM-900 (red line) and GSM-1800 (blue line) bands.

environment. This difference is due to the lower density of base transceiver stations as well as of user transmitting elements, and to the morphology of the rural environment. From the harvester design point of view, the measured amount of RF power reported in Tab. 2.1 might be sufficient to recharge the supply accumulator of a sensor node in some of the evaluated bands. Considering its larger availability, the GSM-900 band is the most suitable one for the design of an integrated harvester.

Based on the RF power survey, a multi-band system, made by an antenna array, would widen the exploitable RF band, but with an important increase of occupied area [10]. Since the power peaks are not constant across space and time, the integration of an adaptable system to find the maximum available power can greatly improve harvesting performance. Examples of adaptable system for maximum power point tracking (MPPT) are given in [17, 18, 19]. Based on this analysis, the RF harvester design described in the next chapter includes a suitable tracking logic. Adding such feature allows the operation of the harvester across different environments and expands the circuit application space even to those situations where RF field strength and spectrum distribution are not known a priori.

Table 2.1: Summary of the RF survey measurements

Environment	**Band**	**Average P_{IN} [dBm]**	**Maximum P_{IN} [dBm]**	σ **[dBm]**
Urban	GSM-900	-21.3	-19.2	-26.5
	GSM-1800	-32.3	-31.3	-42.5
	LTE	-36	-34	-43.3
Semi Urban	GSM-900	-28.9	-22.3	-28.9
	GSM-1800	-48.8	-43.5	-53.7
	LTE	-40.2	-37	-45.8
Rural	GSM-900	-55	-53	-65.5
	GSM-1800	-70	-45	-58

Chapter 3

HarvIC: RF Harvester Circuit

Recent advances in low-power circuits design have enabled mm-scale wireless systems for wireless sensor networks and implantable devices [20]. Energy harvesting allows ambient energy extraction and represents an attractive option for the powering of these systems. In particular, ambient energy extraction can support battery-powered systems in order to extend their lifetime, coping with the limited energy capacity of the batteries with minimum form factors, and lead to energy-autonomous systems [21].

As illustrated in the previous chapter, the RF electromagnetic field can be a competitive source for the harvesting process. However, the RF field has proved to be non-controllable and non-predictable in terms of available power and frequency carrier. These constraints require the implementation at system level of ultra low-power design techniques in RF Harvester circuits, like duty-cycling or power-gating.

This chapter describes the design in 65 nm CMOS technology of an RF energy harvester to recharge an off-chip charge reservoir (i.e. a large capacitor or a supercapacitor) used for the power supply of an integrated temperature sensor, a Sigma-Delta analog-to-digital converter, and a communication block (Fig. 3.1).

The RF front-end carries out the AC to DC voltage conversion, whereas the power management transfers the energy coming from the antenna to the accumulator. The harvester integrates also a finite state machine (FSM), implemented in the analog

domain, realizing a maximum power point search and track algorithm [8].
The system is designed to enable alternatively the MPPT and the power transfer, in order to adapt the harvesting operation to mutable environments. In current design the duty cycle is provided by an external control, although the internal low frequency oscillator could be used. During the active phase of the the digital section, the FSM tunes the input impedance to maximize the output power delivered by the AC-DC converter, with negligible cost in terms of additional power. In this phase, the buffer capacitor at the output of the AC-DC converter is disconnected.
Many RF harvesting systems have already been presented in literature, e.g. [22, 23, 24]. Despite the non-controllability and the non-predictability of the RF source, almost all proposed RF harvesters treat it as a continuous power source, considering the charge flux at the output of the AC-DC converter constant. However, in typical urban and semi-urban environments the available RF power exhibits significant variations over the day.

This chapter presents an RF harvester circuit composed by an AC-DC converter and a DC-DC converter with auto-adaptive capability to the available antenna power level and to the voltage of the off-chip charge reservoir (i.e. a large capacitor or a super-capacitor). A mathematical model of the interface between the RF rectifier and

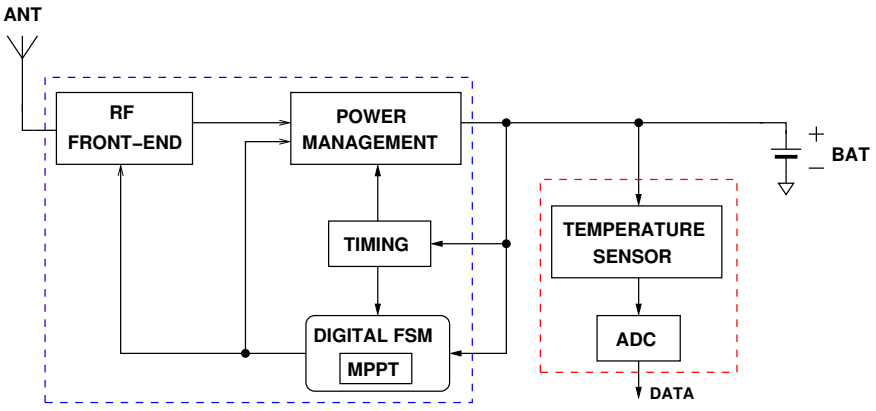

Figure 3.1: Architecture of the proposed sensor node.

the DC-DC converter is provided. The analysis demonstrates that the energy can be efficiently transferred to the external charge accumulator even for extremely low values of available RF power at the antenna terminals, coupling an RF rectifier with a DC-DC converter with strobed input control. Indeed, considering the low availability of RF power and the size of the accumulator, with this control strategy the DC-DC provides to the AC-DC an equivalent load resistance which is only dependent on the input power, the rectifier efficiency and the voltage of th external charge reservoir. This conclusion permits the generalization of the approach to any AC-DC topology.
A strobed DC-DC converter with input control, derived from these results, is proposed. Thanks to the reduced circuit complexity, compared to other harvester implementations, the proposed harvester exhibits a positive energy balance at extremely low levels of RF power.
Post-layout simulation results of the ultra low-power RF harvester, designed in 65 nm CMOS technology, are reported. These results, in terms of sensitivity and end-to-end power conversion efficiency (from RF input to DC output), show that the proposed harvester architecture can be effectively used in some actual daily life environments, including the urban and semi-urban environments investigated in the previous chapter. Finally, the MPPT system integrated in HarvIC is presented in terms of high-level control algorithm, circuit design, and simulation results.

3.1 RF harvester design

An RF harvester circuit is based on an RF rectifier, i.e. an AC-DC converter, a DC-DC converter, and charge storage devices, e.g. capacitors C_H and C_S, as shown in the schematic in Fig. 3.2. The storage device C_S is a large off-chip capacitor (ceramic multi-layer or super-cap) used to provide the power supply for low-power wireless circuits. The latter could be, among others, a WSN or a device for IoT applications. An auxiliary battery V_{AUX} may be introduced to keep the voltage across C_S above the minimum acceptable value for the supply voltage V_{BAT}. Diode D_X can be replaced with a switch driven by a dedicated control circuit.
If the harvested RF energy is enough to supply the sensor node, the power of the

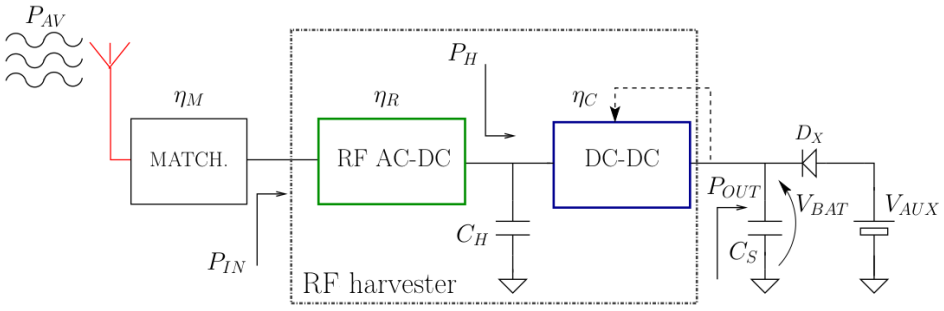

Figure 3.2: Detail of the RF harvester section with charge storage capacitor (C_S).

auxiliary battery is saved and its life-time is significantly increased. However, in order to obtain an effective energy harvesting, a positive balance between the incoming power (P_{IN}) and the energy required for the control circuits of the DC-DC converter must be guaranteed.
The low availability of RF power in generic environments, confirmed by the results of Sec. 2.1.2, represents the main challenge for the design of an RF harvester circuit, which must exhibit:

- A low input power threshold S_{IN} of the RF front-end. Such threshold (i.e. sensitivity) is defined as the minimum input power enabling the RF rectifier.
- A maximum end-to-end power conversion efficiency.
- An ultra low-power consumption.

3.1.1 Radio-frequency Front-End

A non-linear model of the RF rectifier (i.e. RF AC-DC converter) is shown in Fig. 3.3, where the short-circuit output current I_{Hs} is defined as

$$I_{Hs} = \begin{cases} 0 & V_{IN-p} \leq V_{ID} \\ \dfrac{N_R \left(V_{IN-p} - V_{ID}\right)}{R_{Hs}} & V_{IN-p} > V_{ID} \end{cases} \tag{3.1}$$

where N_R is the open-load input-to-output voltage ratio of the rectifier, V_{ID} is the internal voltage drop, and V_{IN-p} is the amplitude of the input sinewave. Resistor R_{Hs} models the internal power consumption effects ascribed to the on-resistance of the rectifying devices and to the circuits implementing the self (partial) cancellation of the threshold voltages [25]. Furthermore, the parameter ΔV is related to the voltage drop across the rectifying device and it is assumed approximately constant in this model.

It is worth to be noticed that the equivalent input resistance R_{IN} exhibits a large dependence on the load resistance R_{LH}, while C_{IN} is mainly due to the ESD protection and pad capacitance [26] and, for this reason, is assumed constant.

An inductive matching network L_M is normally used to achieve the power matching condition (i.e. the matching circuit in Fig. 3.2) and to provide voltage amplification (Fig. 3.3). However, the required inductive contribution to the source impedance may be obtained by slightly detuning the antenna or by means of the T-match technique [15, 16].

As mentioned in section 2.1.2, the *R-L-C* series circuit, composed by the antenna, the matching network and the harvester input impedance, has an overall quality factor Q_{LC} that, at the resonance frequency $f_0 = 1/\left(2\pi\sqrt{C_{IN}L_M}\right)$, is:

$$Q_{LC} = \frac{1}{[R_{ANT} + R_{IN}\,(R_{LH})]} \cdot \frac{1}{2\pi f_0 C_{IN}} \tag{3.2}$$

where R_{ANT} is the radiation resistance of the antenna. The overall quality factor has huge impact on the input peak-value of V_{IN-p}, and on the input sensitivity.

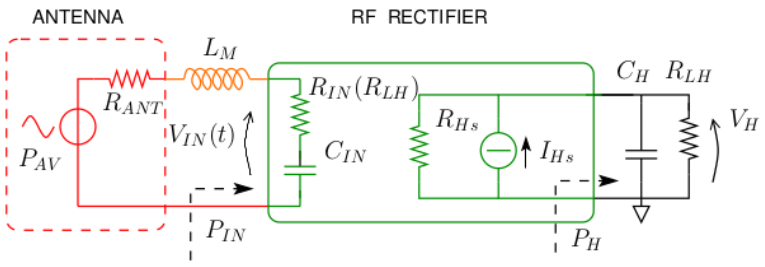

Figure 3.3: Large-signal model of the RF rectifier.

Assuming that the reactance of the RF rectifier and of the antenna (including L_M) are power matched, i.e. $f = f_0$, the value of V_{IN-p} is

$$V_{IN-p} = Q_{LC} \cdot \sqrt{8 \cdot P_{AV} \cdot R_{ANT}} \cdot \sqrt{1 + \frac{1}{Q_{LC}^2} \cdot \frac{R_{IN}(R_{LH})}{R_{ANT} + R_{IN}(R_{LH})}} \tag{3.3}$$

where the last factor can be neglected with standard values of Q_{LC}, i.e. $Q_{LC} > 3$. The non-linear behavior of the RF rectifier generates a lower bound for the peak-input voltage V_{IN-p}, leading to a minimum input power S_{IN} (at $f = f_0$):

$$S_{IN} = \frac{(V_{TH})^2 \cdot R_{IN}(R_{LH})}{2 \cdot Q_{LC}^2 \cdot [R_{ANT} + R_{IN}(R_{LH})]^2} \tag{3.4}$$

where S_{IN} is the input sensitivity of the rectifier. Since R_{IN} exhibits an inverse relationship on R_{LH}, and Q_{LC}, from (3.2), exhibits an inverse relationship on R_{IN}, we can conclude that the higher the delivered power P_H, at some value of the rectified voltage V_H, the higher the power threshold S_{IN}.

From equations (3.2) and (3.4) we also deduce that S_{IN} is decreased by decreasing R_{ANT} and C_{IN}. However, decreasing the value of R_{ANT} below 10 Ω makes the antenna design quite challenging. Furthermore, the value of C_{IN} is lower bounded by the pad, the ESD protections, and the package. Finally, a value of Q_{LC} above few tens makes power matching with the antenna quite difficult unless an auto-tuning facility is added [19].

Many RF rectifiers have been presented in literature, e.g. [25], [27], [28]. In this thesis a Full-Wave Mirror Stacked architecture with threshold voltage compensation [28] has been designed and implemented in ST 65 nm CMOS technology. The half-circuit of the differential single-stage RF rectifier processing the positive half-wave is shown in Fig. 3.4, where $M1$ and $M2$ are, respectively, the rectifying series and shunt devices. The circuit within the dashed shape keeps the bias point of $M1$ at $V_{GS5} \approx V_{TP}$, V_{TP} being the threshold voltage of PMOS devices. Therefore, this circuit implements a threshold-voltage compensation at the cost of some additional current consumption through $M5$ and $R1$. A similar functionality is implemented by $R2$, $C3$, $M6$ in order to compensate the threshold voltage of $M2$. The threshold voltage compensation technique can accurately tracks the process and temperature variation by

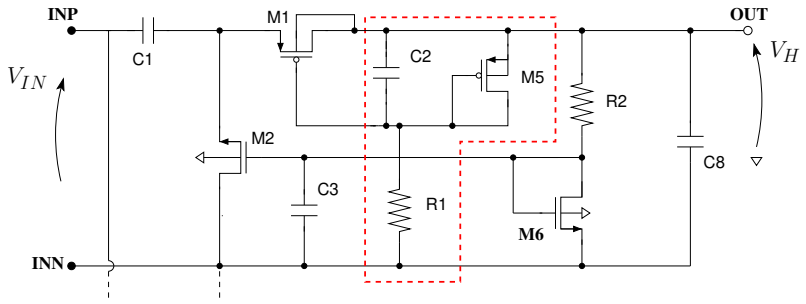

Figure 3.4: Schematic of a half-circuit of the RF rectifier.

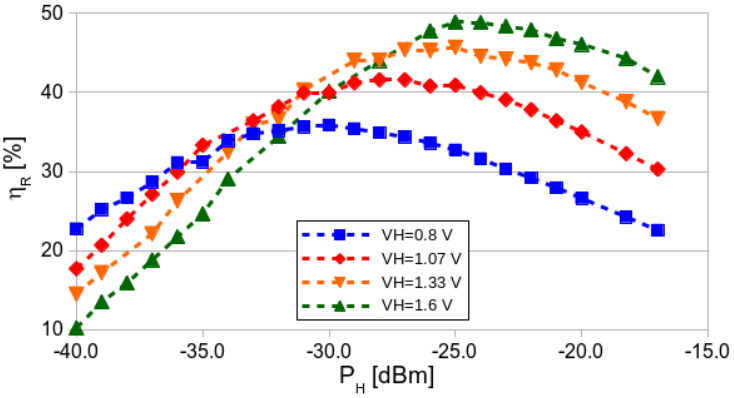

Figure 3.5: Simulated power efficiency η_R vs. delivered power P_H.

matching the rectifying and the biasing devices [28]. Therefore, remarkable efficiency performance can be obtained over the full PVT space.

Post-layout simulation results of the rectifier power efficiency η_R and of the input resistance R_{IN} are shown in Fig. 3.5 and Fig. 3.6. In these simulations, the value of P_{AV} has been adjusted to keep the output voltage V_H constant over the sweep of the load resistance R_{LH}. It has to be noticed that η_R exhibits a positive derivative at low values of delivered DC power, whereas the derivative is reversed at high values of P_H. Indeed, at low P_H the efficiency is mainly limited by the voltage drop ΔV. On the contrary, at higher P_H the series resistance of the rectifying device, modeled by

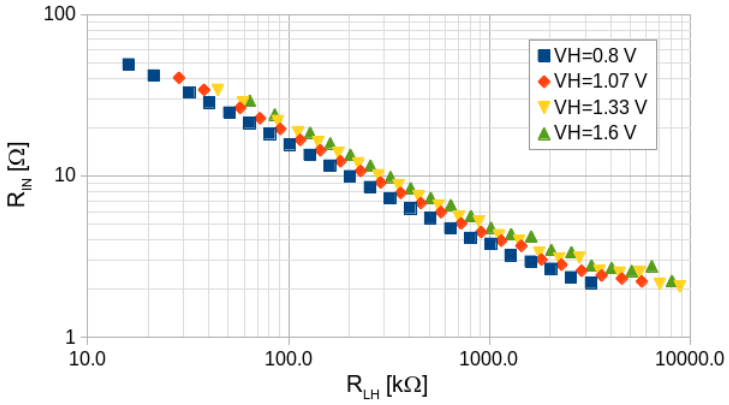

Figure 3.6: Simulated input resistance of the RF rectifier R_{IN} vs. load resistance R_{LH}.

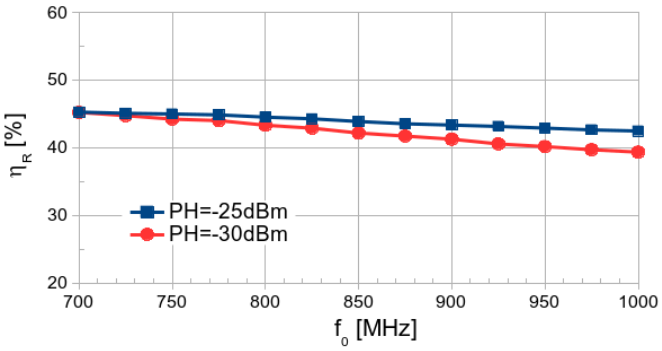

Figure 3.7: Simulated rectifier efficiency η_R over the GSM-900 band, at V_H=1.07 V with R_{LH}=370 kΩ (squares) and R_{LH}=1.14 MΩ (circles).

R_{Hs} in Fig. 3.3, is the dominant effect. The maximum of η_R moves towards higher values of P_H if the DC output voltage is increased. Indeed, the higher V_H, the lower the output current (at the same P_H), thus leading to a lower impact of R_{Hs}.
The plot of R_{IN} vs. R_{LH} in Fig. 3.6 shows that the input resistance exhibits a negligible dependence on the DC output voltage for $V_H > 1.1$ V, while a mild dependence occurs for $V_H < 1$ V. The above simulation extended over the PVT space, with a source

resistance R_{ANT} = 10 Ω, returned a sensitivity of -33 dBm and C_{IN} = 315 fF, with R_{LH} = 3.2 MΩ and V_H = 0.8 V, at 900 MHz.
Fig. 3.7 shows the efficiency performance of the chosen rectifier circuit over the GSM-900 band. The results, reported for P_H = -30 dBm and P_H = -25 dBm, confirm the robustness of this architecture for very low power values of converted power.

3.1.2 Harvested energy from an ultra low-power RF source

In the majority of sensor node or harvesting applications, the voltage at the output of the AC-DC converter V_H has to be pulled up to achieve an effective recharge of the external accumulator. Moreover, achieving high conversion efficiency at relatively high values of V_H and with P_{IN} in the order of μW, poses relevant design issues [25]. DC-DC boost converters with an off-chip inductor are often used in such applications, even though fully integrated inductorless step-up converters have been also reported [29, 30, 31]. A black-box schematic describing the interfacing of the RF rectifier with a step-up converter for ultra low-power sources is shown in Fig. 3.8.
The Norton-equivalent model was used for the output stage of the rectifier for an easier analysis of the system. Resistor R_L is introduced to model the power consumption of the DC-DC converter when enabled. The off-chip charge reservoir C_S can be considered as a voltage source due to its high value, and, therefore, V_{BAT} is approximated as a constant voltage over a short period. The auxiliary battery V_{AUX} is omitted in the analysis. The switch connecting the harvester to the boost converter is introduced

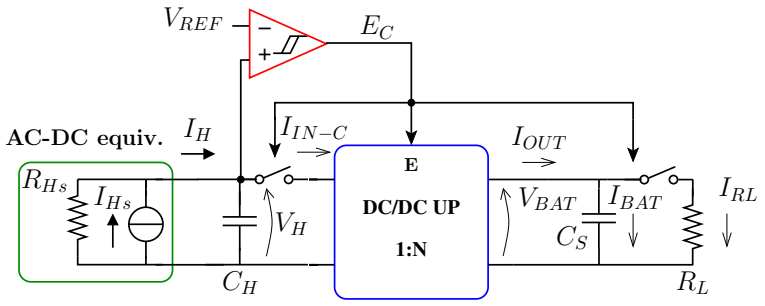

Figure 3.8: Simplified model of the RF harvester for ultra low-power source.

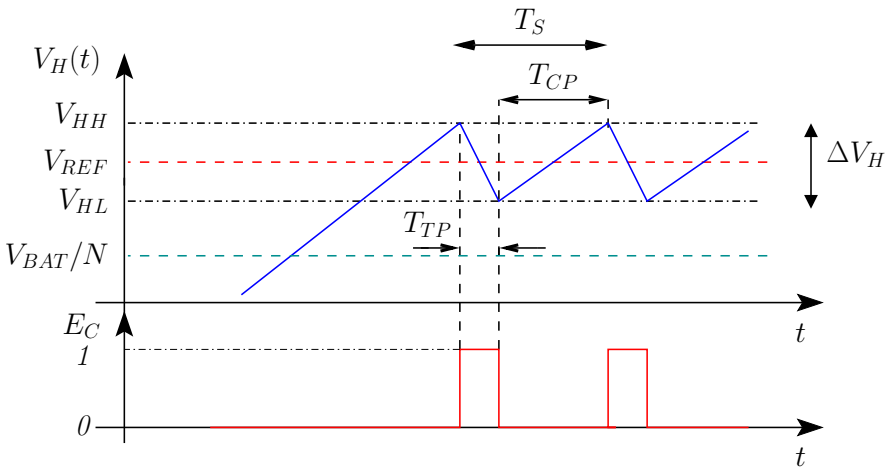

Figure 3.9: Time diagram: V_H, going from V_{HH} to V_{HL}, and control signal E_C.

to model the change of the equivalent load of the rectifier when the converter toggles between ON ($E_C = 1$) and OFF/High-Impedance ($E_C = 0$) states.
From the equation of the power efficiency η_C of the converter, the following relationship is obtained:

$$I_{IN-C} = \frac{I_{OUT} \cdot N}{\eta_C} \tag{3.5}$$

where N is the output-to-input voltage ratio with open-load and I_{OUT} the output current of the DC-DC converter.
Assuming the logic signal E_C at the high level (i.e. the DC-DC converter enabled), some conditions must be imposed on the (short-circuit equivalent) output current of the rectifier I_{Hs}. A positive energy transfer from the RF rectifier to the charge reservoir occurs if $I_{IN-C} \geq 0$. From (3.5) and considering the large value of C_S, the voltage at the input of the enabled converter can be assumed constant and equal to V_{BAT}/N. Therefore, the open-load output voltage of the rectifier must be higher than V_{BAT}/N:

$$V_{H0} \equiv I_{Hs} \cdot R_{Hs} \geq \frac{V_{BAT}}{N} \tag{3.6}$$

A more stringent condition is found if the overall efficiency is considered. Indeed, the energy provided by the converter and accumulated in the charge reservoir (C_S)

must be higher then the energy required for the control of the DC-DC converter itself. Therefore:

$$P_H > \frac{V_{BAT} \cdot I_{RL}}{\eta_C} \tag{3.7}$$

where I_{RL} is the current consumption of the control circuits.
The latter condition might not be satisfied in case of low input power. Finally, the harvester must be able to provide the input current of the DC-DC converter I_{IN-C}, which from (3.5) depends on the output current. Since I_{OUT} is limited by the small series resistance of C_S (not shown in Fig. 3.8) and of the DC-DC converter, the input current is expected to exceed the maximum I_{Hs} that the rectifier can source.
In order to overcome these limitations, a strobed DC-DC converter has been adopted for the harvester implementation. The converter enable signal E_C is provided by a comparator with hysteresis which monitors the output voltage of the rectifier. Furthermore, an on-chip capacitor at the rectifier output C_H, used as charge reservoir, is charged when E_C is low (DC-DC converter disabled) and discharged by I_{IN-C} when E_C is high. A reference voltage V_{REF} is provided at the negative input of the comparator and used as the control set-point. The following condition must be fulfilled:

$$V_{HL} \equiv V_{REF} - \frac{\Delta V_H}{2} > \frac{V_{BAT}}{N} \tag{3.8}$$

where ΔV_H is the hysteresis width. This condition is mandatory to avoid that the DC-DC converter reaches the stable operating condition with $V_H = V_{BAT}/N$, leading to a reverse energy transfer from the storage capacitor C_S towards the rectifier. Therefore, if conditions (3.6) and (3.8) are fulfilled, the average value of V_H is set to V_{REF}.
The main waveforms that characterize the circuit are shown in Fig. 3.9. The conversion period T_S is given by the sum of the charge phase period T_{CP} and the transfer phase period T_{TP}. T_{CP} is obtained by equating the variation of the energy stored in C_H to the energy delivered by the harvester in that phase. T_{TP} depends on the equivalent series resistance of the DC-DC converter R_{SS}, which is mainly due to the on-resistance of the switches in the converter itself. If the effect of R_{Hs} is neglected (since $R_{Hs} >> R_{SS}$) and considering a low input power, i.e. a low value of I_H, T_{CP}

and T_{TP} are approximated by the following equations

$$T_{CP} = \frac{C_H \, \Delta V_H \, V_{REF}}{\eta_R \, P_{IN}} \tag{3.9}$$

$$T_{TP} \approx R_{SS} \, C_H \, \ln\left(1 + \frac{\Delta V_H}{V_{HL} - V_{BAT}/N}\right) \tag{3.10}$$

The approximation in (3.9) is valid if $C_H \cdot R_{Hs} >> T_{CP}$, which is usually verified due to the high value of R_{Hs}. With a low input power the length of the transfer phase is negligible with respect to T_{CP}. Under this assumption, the duty cycle ρ_{DC} of the waveform E_C is

$$\rho_{DC} \approx \frac{R_{SS} \, \eta_R \, P_{IN}}{\Delta V_H V_{REF}} \ln\left(1 + \frac{\Delta V_H}{V_{HL} - V_{BAT}/N}\right) \tag{3.11}$$

The average input resistance of the strobed DC-DC converter, over the period T_S, corresponds to the load resistance of the rectifier R_{LH} of section 3.1.1 and it depends only on the average values of the output voltage $\overline{V_H}$ and of the output current $\overline{I_H}$ of the rectifier:

$$R_{LH} \approx \frac{\overline{V_H}}{\overline{I_H}} \approx \frac{V_{REF}^2}{\eta_R \cdot P_{IN}} \tag{3.12}$$

where the equivalence $\overline{I_H} \approx \eta_R \cdot P_{IN}/\overline{V_H}$ has been used and η_R is the rectifier power efficiency. Therefore, a strobed DC-DC converter with hysteretic control provides a self-adaptive input resistance, which indeed varies according to the harvester input power.

Condition (3.7) must be evaluated before the activation of the DC-DC converter, since, if it is not satisfied, the power wasted for converter control would be higher than the harvested power. Hence, a power meter circuit located at the output of the rectifier can be used to periodically check the amount of input current and then disable the DC-DC converter in case (3.7) in not fulfilled.

It is worth to be noticed that in [24] a DC-DC converter with input control is proposed for RF harvesting. However, in that reported implementation the control is based on the monitoring of the inductor current. The system proposed in this thesis exhibits a simpler control strategy with benefits in terms of reduced complexity, a lower number of involved circuit blocks, and a lower power consumption. A further advantage

provided by the strobed converter is the possibility to implement a Maximum Power Point searching and Tracking for the RF harvester. Indeed, with a low input power P_{IN} the rectifier exhibits the highest efficiency with a low value of V_H. In case of higher available power at the antenna, better power efficiency is achieved if the rectifier is forced to work with higher V_H, as shown in Fig. 3.6. Therefore, the value of V_{REF} and of the voltage ratio N can be adapted to harvest the maximum available power from the antenna at any value of input power, provided that conditions (3.6), (3.7), and $V_{HL} \geq V_{BAT}/N$ are fulfilled.
Finally, since the rectifier input resistance R_{IN} depends on its equivalent load resistance, the value of V_{REF} can be tuned to achieve the resistive power matching between the antenna and the rectifier, i.e. $R_{IN}(R_{LH}) = R_{ANT}$.

3.1.3 Strobed DC-DC converter with input control

In the proposed design, a boost DC-DC converter with off-chip inductor was preferred for the implementation of the strobed converter described in the previous section. The circuit schematic is shown in Fig. 3.10.
Despite a higher switching frequency (f_{SW}), compared with Discontinuous Conduction Mode and Boundary Mode [29], in the proposed implementation the Continuous Conduction Mode (CCM) has been chosen. Benefits of this technique are the reduced complexity and the lower power consumption of the converter control circuit. From (3.7) it results that this power saving allows an effective harvesting of power from the antenna at lower values of available input power.
The converter control circuit is divided into a Monitor section, including the hysteretic comparator and the bias circuit, and a Switching section, including an oscillator, a generator of the non-overlapped clock signals, and drivers for M_{LS} and M_{HS} switches. Both sections are powered by the large, off-chip, storage capacitor C_S. An undervoltage lockout circuit (*UVLO*) is used to monitor the supply voltage V_{BAT} and to power down both Switching and Monitor sections when V_{BAT} is lower than the minimum value. In the proposed implementation this lower bound is set to 1.1 V. The schematic of the *UVLO* block, derived from [32], is shown in Fig. 3.11. Diode D_U is implemented with a MOS transistor biased in weak inversion. The threshold of the

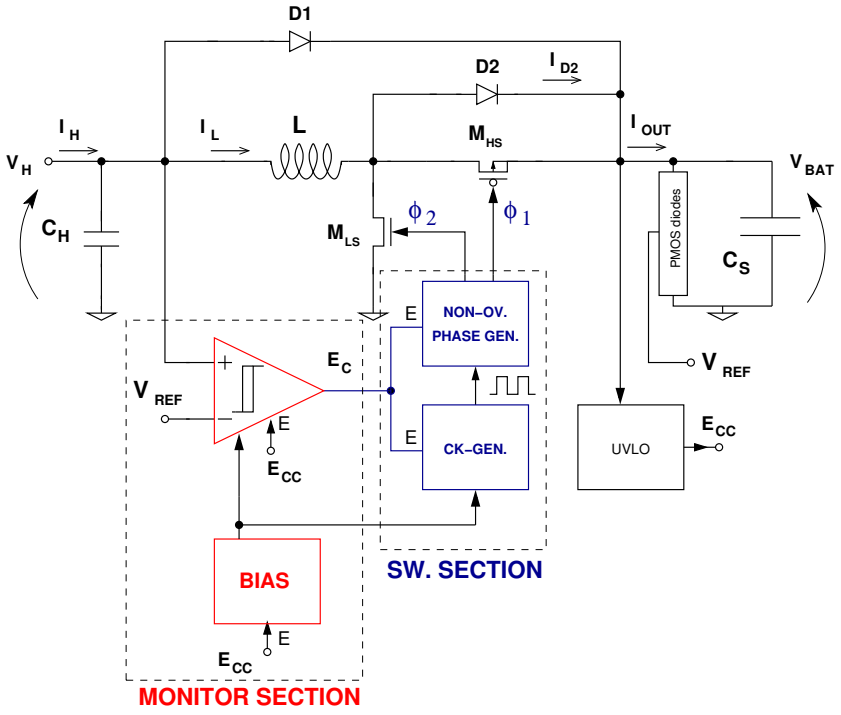

Figure 3.10: Block diagram of the strobed DC-DC converter with input control.

first CMOS inverter is $K_1 \cdot V_{BAT}$, where K_1 is set by design with the aspect ratio of the PMOS and NMOS device within INV_1. Therefore, the voltage threshold of the battery monitor is:

$$V_{T-UVLO} = \frac{V_{DU}}{1 - K_1} \tag{3.13}$$

where V_{DU} is the forward voltage drop across diode D_U. Switch M_1 modulates the bias current of D_U and, therefore, V_{DU}, leading to an hysteresis in the I/O characteristic V_{BAT}-E_{CC}.

The Switching section is disabled with $E_C = 0$, i.e. $V_H \leq V_{REF} + \Delta V_H/2$, where ΔV_H is the hysteresis width of the comparator. In this condition, the DC-DC converter is driven to high-impedance mode and both M_{LS} and M_{HS} switches are forced to the off state.

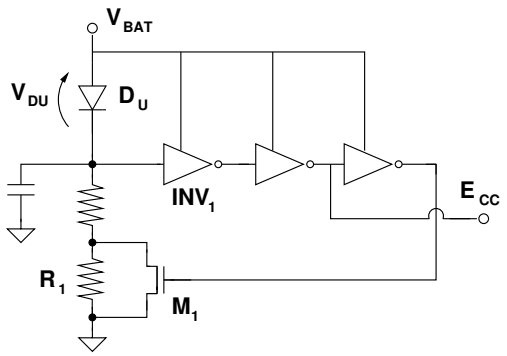

Figure 3.11: Under-Voltage Lockout circuit.

The Bias circuit in the Monitor section is based on a low-power, constant-Gm current reference, with start-up circuit, setting the bias current I_B of a comparator circuit, Figs. 3.12 and 3.13 [33].
The clock generator in the Switching section is a Current-Starved Ring Oscillator featuring a power consumption of few hundreds of nW. Diode *D1* bypasses the DC-DC converter when the voltage across the storage capacitor is too low to enable the Monitor and Switching sections. Therefore, with a low supply voltage the storage capacitor is directly charged by the rectifier through the bypass diode *D1*. Furthermore, such diode provides an effective overvoltage protection for the rectifier inputs. Both *D1* and flyback diode *D2* are implemented with PMOS devices.
The voltage ratio of the DC-DC converter N is set by the duty cycle of the clock signals driving switches M_{LS} and M_{HS}. In our implementation the converter has been optimized for $N = 2$.
Since V_{REF} must track the voltage of the output capacitor to fulfill condition (3.8), this voltage reference is derived with ratiometric approach from V_{BAT} and implemented as a stack of PMOS diodes biased in weak-inversion. Furthermore, the V_{BAT}/V_{REF} ratio has to be changed according to the voltage ratio N of the DC-DC converter. This programmability is easily implemented by changing the tap in the diode stack where the reference voltage is derived from. By means of this approach, the converter can properly work over a large range of the output voltage V_{BAT}, i.e. from 1.1 V to 2.5 V.

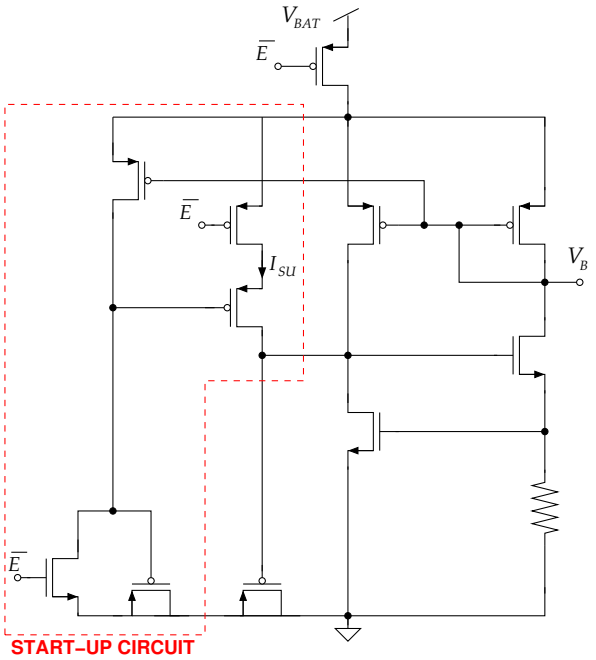

Figure 3.12: Constant-Gm biasing circuit, with start-up circuit, schematic view.

The size of the off-chip inductor and the frequency of the oscillator f_{SW} are optimized for the maximum efficiency, minimum ripple of the inductor current, as well as the inductor availability in a compact package. The latter specification has substantial relevance to minimize the size of the final device embedding the proposed integrated harvester. Finally, the tolerance affecting the switching frequency must be carefully evaluated to avoid the converter being forced to work in discontinuous current mode. The values of C_{HARV} and ΔV_H are chosen on the basis of the maximum frequency $f_S = 1/T_S$ of the enable signal E_C, of the maximum ripple that can be tolerated at the rectifier output, and of the minimum length of the transfer phase, T_{TP} in (3.10). Indeed, f_S must be upper limited in order to minimize the switching power consumption of the comparator.

In the implementation described in this thesis we set $f_S = 20$ kHz. Furthermore, T_{TP} must include at least one period of the DC-DC clock signal.

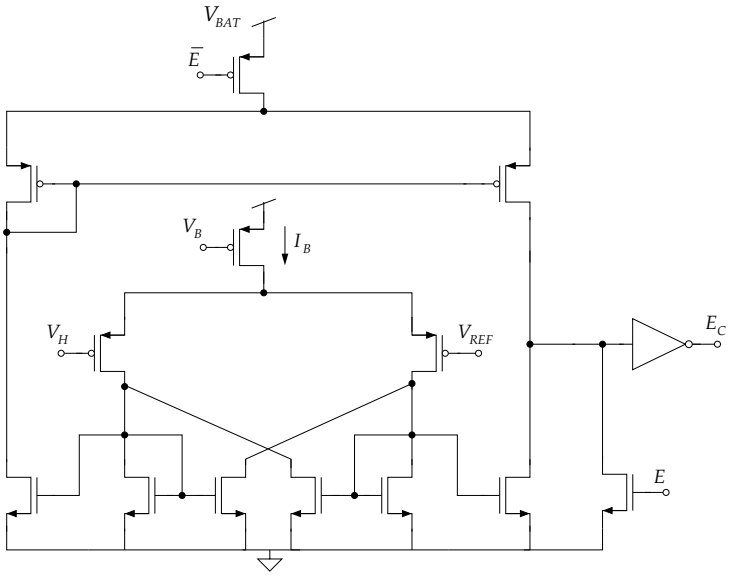

Figure 3.13: Hysteresis Comparator circuit schematic view.

Another design issue is the slew rate of V_H, which must be compatible with the input bandwidth and I/O delay of the comparator. If this condition is not fulfilled, the peak-to-peak variation of V_H largely exceeds the hysteresis width of the comparator, with the risk that condition (3.8) is no longer satisfied. A multi-layer SMD capacitor with ceramic dielectric and a value in the 1-10 μF range was selected as off-chip charge accumulator C_S. The leakage current of these capacitors is limited to few hundreds of nA [34], [35]. Therefore, taking into account that the average current consumption of the analog circuit powered by the harvester (i.e. the temperature sensor) is in the 1-to-10 μA range, a multi-layer capacitor is preferred to a super-capacitor because of the lower leakage current and cost.

The component values and settings for the implementation described within this thesis are reported in Tab. 3.1, where the values of f_{SW}, T_S, and ρ_{DC} are obtained by post layout simulation of a typical corner with $V_{BAT} = 1.4$ V and $I_H = 1\ \mu A$. The chosen inductor has $L = 3.9$ mH and a specified maximum value of equivalent series resistance $R_{LS} = 40\ \Omega$ [36].

Table 3.1: DC-DC converter: settings and component values

	Value	Unit
L	3.9	mH
f_{SW}	750	kHz
C_H	600	pF
ΔV_H	250	mV
V_{REF}/V_{BAT}	0.65	
f_S	20	kHz
ρ_{DC}	50	%
$(W/L)_{LS}$	12/0.4	μm/μm
$(W/L)_{HS}$	12/0.4	μm/μm

3.2 System performance and simulation results

The proposed RF harverster has been implemented and simulated in ST 65 nm CMOS technology with 2.5 V thick-oxide option. Simulations were performed with back-annotated parasitic layout (R-C), SMD inductor model, and across the Process, Voltage, and Temperature space (PVT). The voltage supply of the harvester V_{BAT} can vary from 1.1 V up to 2.5 V and the system can operate over the temperature range $[-40 \sim 85]\ ^{o}$C. Fig. 3.14 shows the main waveforms of the strobed DC-DC converter during the transfer phase whereas in Fig. 3.15 the efficiency of the DC-DC converter at different values of V_{BAT} is plotted versus the rectifier delivered power P_H. The results in Fig. 3.15 shows that an overall positive energy balance between the harvested power and the power consumption of the converter control is achieved starting from a value of P_H as low as 350 nW at V_H = 1.1 V. From the simulated efficiency of the rectifier, Fig. 3.6, this value of P_H corresponds to an input power P_{IN} = −30 dBm at f_0 = 900 MHz and a P_{IN} = -29.7 dBm at f_0 = 950 MHz. The results of Fig. 3.16 show the power efficiency over the process and temperature space. The designed DC-DC converter exhibits a good robustness and performance stability

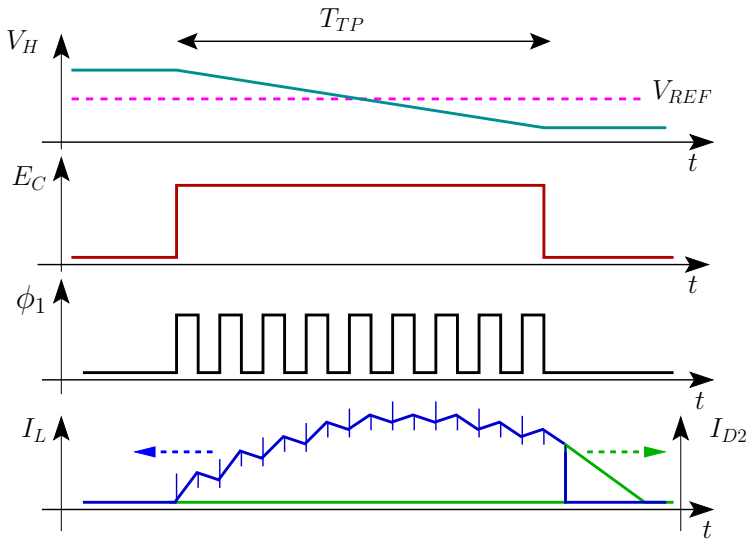

Figure 3.14: DC-DC converter waveforms: detail of the transfer phase when the charge is moved from C_H to C_S through L and $D2$.

Table 3.2: Current consumption at V_{BAT}=1.4 V, process typical

	Charging Phase		Transfer Phase	
Temp	$I_{cc,mon}$	$I_{cc,sw}$	$I_{cc,mon}$	$I_{cc,sw}$
-40^oC	242 nA	1.4 nA	270 nA	369 nA
27^oC	230 nA	2.5 nA	275 nA	346 nA
85^oC	171 nA	4.8 nA	226 nA	335 nA

with a limited spread of the power efficiency over the PVT space.

In Tab. 3.2 the maximum current consumption of the Monitor ($I_{cc,mon}$) and Switching ($I_{cc,sw}$) sections of the DC-DC converter are reported at the minimum, typical, and maximum temperature, for the two operating modes (charging and transfer phase).

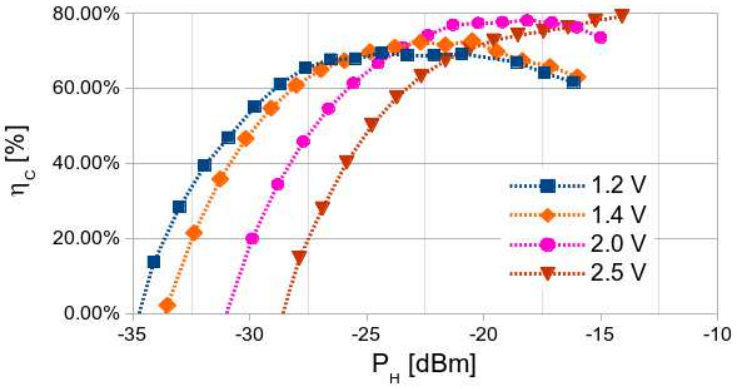

Figure 3.15: Simulated efficiency of the DC-DC converter, η_C, Vs. converter input power P_H at V_{BAT} from 1.2 V up to 2.5 V.

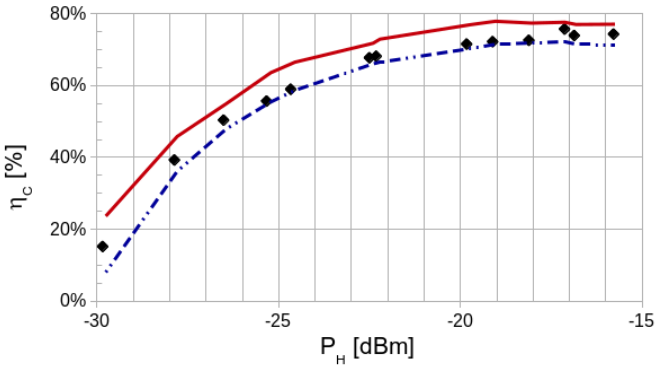

Figure 3.16: Simulated DC-DC converter efficiency η_C vs. input power P_H at V_{BAT} = 2 V, over process and temperature. Black diamonds: typical corner. Solid red line: best-case efficiency. Dashed-dotted blu line: worst case efficiency.

3.2.1 Discussion

As reported in Tab. 3.3, the proposed DC-DC converter shows remarkable performance compared with the state-of-the-art DC-DC boost, buck and buck-boost con-

Table 3.3: Performance comparison: DC-DC converters for power harvesting

	[29]⋆ ISCAS 2016	[37] ISSCC 2011	[31] JSSC 2016	[38] CICC 2018	[30] TPEL 2015	[39] ISSCC 2015	This work⋆ 2018
Process	350 nm⋆⋆	250 nm	180 nm	65 nm	180 nm	250 nm	65 nm
Arch.	Ind. Boost	Ind. Boost	SC Boost	Ind. Buck-Boost	Ind. Boost	Ind. Buck	Ind. Boost
V_{IN}	1.3 V	0.5−2 V	0.35−0.6 V	0.6−1.2 V	>0.6 V	up to 60 V	>0.6 V
V_{OUT}	1.3−3.3 V	0−5 V	0.86−1.8 V	up to 3.5 V	0.9−1.2 V	0−5 V	1.1−2.5 V
Peak η_C	96%@V_{IN}=1.3 V	87%@V_{IN}=1 V	75.8%	91%@V_{IN}=1.5 V	85%@V_{OUT}=0.9 V	85%	80%@V_{OUT}=2.5 V
P_{OUT} @ η_C	123 μW	3 mW	395 μW	200 μW	9 μW	8.5 μW	40 μW
P_H min.	*NA*	5μW@η_C ≈61%	*NA*	5μW@η_C ≈30%	5μW@η_C ≈20%	1μW@η_C ≈50%	350 nW
P_{DC}	*NA*	2.4 μW	320 nW	*NA*	1 μW	500 nW	350 nW
C_H	*NA*	*NA*	4.05 nF	*NA*	*NA*	100 nF	800 pF
Temp. range	-20~80 °C	*NA*	*NA*	*NA*	25~65 °C	*NA*	-40~85 °C
Area [mm^2]	*NA*	2.72	1.65	0.2	0.415	1.85	0.245

⋆Simulated results.

⋆⋆ With Schottky diode option.

verter implementations for power harvesting applications.

The designed system shows good performance in terms of peak efficiency and output voltage range. Remarkable performance, better than the state-of-the-art, has been achieved in terms of power consumption for the converter control, and of minimum input power P_H providing positive energy balance.

The integrated RF harvester based on the cascade of a Full Wave Mirror Stack Rectifier and the strobed DC-DC converter has been simulated over a large range of available input power P_{AV}. Fig. 3.17 shows the typical power conversion efficiency ($\eta_{TOT} \equiv \eta_R \cdot \eta_C$) obtained from post-layout simulations of the whole RF harvester circuit versus the input power P_{IN}, at f_0 = 950 MHz. The worst corner case is also reported (solid red line), corresponding to T = 85 ^{o}C and slow device models. The RF harvester exhibits a start-up time of 3 ms at P_{IN} = -30 dBm and minimum output voltage. The results on typical corner case are reported in Table 3.4 and compared with other RF harvester implementations proposed in literature. The proposed architecture achieves performance comparable in terms of sensitivity and end-to-end power conversion efficiency ($\eta_{TOT} \equiv \eta_R \cdot \eta_C$) with the state-of-the-art RF harvesters, but for

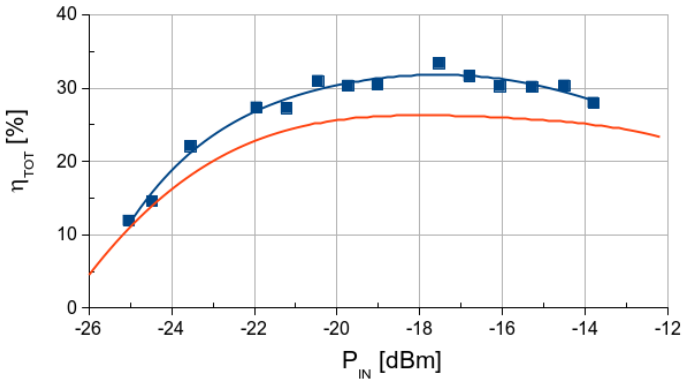

Figure 3.17: Simulated power conversion efficiency η_{TOT} vs. P_{IN} on typical corner (blue) and worst case corner (solid red line) at f_0 = 950 MHz and V_{BAT} = 2 V.

Table 3.4: Performance comparison with state-of-the-art RF Harvesters

	[40]⋆ ISCAS-2018	[23]⋆ NEWCAS-2016	[22] TCAS-2015	[41] Tech. Report 2016	[42] ICRFID-2016	This work⋆ 2018
Technology	180 nm	180 nm	180 nm	*NA*	130 nm	65 nm
Operative Frequency	405.5 MHz	950 MHz	900 MHz	915MHz	900MHz	950MHz
$\eta_R@P_{IN}$ [dBm]	76%@-18 dBm‡	*NA*	53.4%@-15 dBm‡	43%@-10 dBm	5%@-23 dBm	45%@-22 dBm 42%@-25 dBm
Min. P_{IN} [dBm]	*NA*	-24 dBm	-17 dBm‡	-12 dBm	-26 dBm	-30 dBm@V_{BAT}=1.1V -26 dBm@V_{BAT}=2V
$\eta_{TOT}@P_{IN}$ [dBm]	49%@-18 dBm§ 37%@-9 dBm§	16%@-19 dBm 6%@-22 dBm	35.7%@-15 dBm‡ 44.1%@-12 dBm‡	57%@5 dBm	4%@-23 dBm	33%@-18 dBm 27%@-22 dBm
V_{BAT}	>1.1 V	>1 V	2 V	3.3 V reg.	>0.6 V	>1.1 V
Quiescent Power	*NA*	*NA*	3.12 μW	*NA*	10 nW	350 nW
Area [mm^2]	0.2	0.17	0.275	*NA*	0.086	0.3

⋆Simulated results.

‡ P_{AV}.

§ Control circuit power consumption not included.

values of P_{IN} which seem more which seem more likely to be available in the urban and semi-urban RF environments. Moreover, the proposed system shows remarkable performance in terms of minimum input power P_{IN} which allows a positive energy

balance.
It is worth to notice that such values are comparable with those reported in Section 2.1.2 for at least two of the evaluated bands in urban environment and of one band in semi-urban environment.
From the meaurement results reported in Tab. 2.1 (section 2.1) in the GSM-900 band in urban environment, with the average input power $P_{IN} \approx$ -21.5 dBm, the RF harvester can provide an average output power $P_{DC} \approx 2.15$ μW, whereas in semi-urban environment, on the same band $P_{DC} \approx 300$ nW can be scavenged.
Although these values of harvested power could be not sufficient to sustain continuously the power supply of a sensor node, they definitely allow the extension of its life time. Moreover, the information regarding the harvested power availability can be one of the specification for the design of new sensor nodes embedding energy harvesting units.
It is worth noting that wireless sensor nodes operate with low duty cycle. Therefore, although the temperature sensor with A-to-D converter embedded in HarvIC consumes an average power of 15 μW, the power consumption must be averaged on the duty cycle. With a measurement period of ten minutes the average power consumption collapses to hundreds of picowatts [7]. Despite in WSN the power consumption for the data transmission phase has to be considered, the leakage current of the external accumulator still remains the most relevant contribution to the dissipated power [43].

3.3 Maximum Power Point searching and Tracking system

The black box schematic of an RF energy harvester is shown in Fig. 3.18, where the antenna is modeled with a single-tone source with frequency f_S, available power P_{AV}, and series resistance R_{ANT}. As explained in the previous section, the RF harvester is based on an RF rectifier, an intermediate charge reservoir C_H, a DC-DC step up converter, and an off-chip storage element C_{OUT}, with R_L as equivalent load. The inductance L_M models the matching circuit between the source and the rectifier. An R-L-C circuit is obtained at the antenna-to-rectifier interface (i.e. rectenna), with

resonance frequency f_C and quality factor $Q(f_S)$:

$$f_C = \left(2\pi\sqrt{L_M C_{IN}}\right)^{-1} \tag{3.14}$$

$$Q(f_S) = \frac{1}{2\pi f_S C_{IN}\left(R_{IN} + R_{ANT}\right)} \tag{3.15}$$

where C_{IN} and R_{IN} are the input capacitance and resistance of the RF rectifier. The short-circuit output current I_{H0} is modeled as:

$$I_{H0} = \begin{cases} 0 & V_{INp} \leq V_{ID} \\ \dfrac{N_R\left(V_{INp} - V_{ID}\right)}{R_R} & V_{INp} > V_{ID} \end{cases} \tag{3.16}$$

where N_R is the open-load input-to-output voltage ratio, V_{ID} is the internal voltage drop, and V_{INp} is the amplitude of the input sine-wave:

$$V_{INp} = \sqrt{2P_{AV}R_{ANT}}\left[Q(f_S) + 1\right] \tag{3.17}$$

In presence of very low available RF power, the voltage $V_H(t)$ at the output of the rectifier in an input-regulated step-up converter architecture exhibits a saw-tooth shape, with an average value equal to the control set-point V_{H-REF}, Fig. 3.9.
Due to the large value of the charge reservoir C_{OUT}, the converter output voltage can be considered approximately constant over a short time. Furthermore, V_{H-REF} must be higher than V_{OUT}/N_C to avoid any reverse energy flow. Accordingly, the converter is enabled only if the open-load rectifier output voltage, i.e. $I_{H0} \cdot R_R$, is higher than the set-point value.

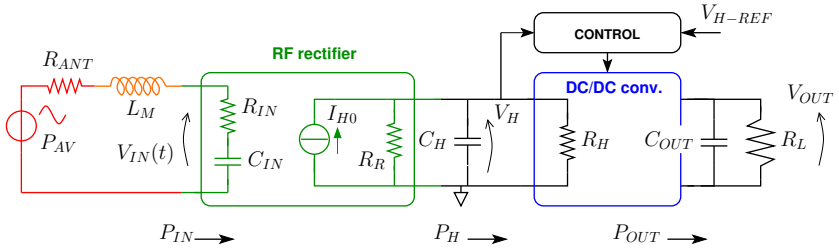

Figure 3.18: Black-box schematic of an RF harvester.

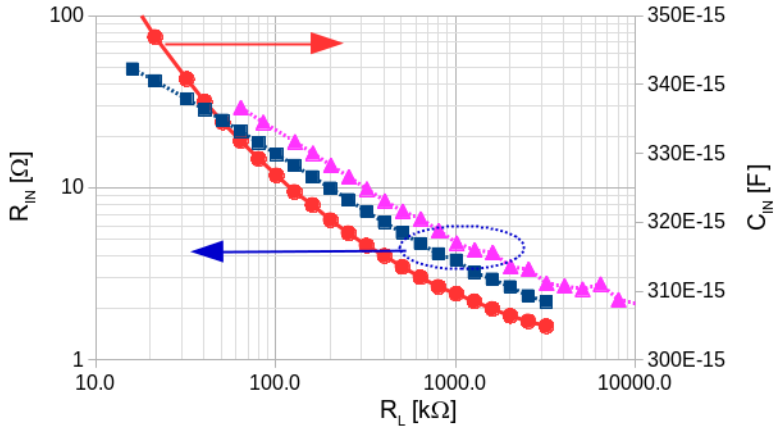

Figure 3.19: Simulated values of the input resistance R_{IN} and input capacitance C_{IN}. Equivalent load R_L is provided by the DC-DC Converter for V_H from 0.8 V to 1.6 V, at f_S = 900 MHz.

Due to the input-control strategy, the converter input resistance R_H depends on I_{H0} and on the average value of V_H, i.e. $R_H \approx \overline{V_H}/I_{H0}$. It can be noticed that R_{IN} is mainly affected by R_H, whereas C_{IN} exhibits a mild dependence on the rectifier's load [44].

3.3.1 Rectifier tuning and power efficiency

From the simulation results in Fig. 3.19, a Q-factor of the rectenna higher than few tens is achieved with a delivered power P_H in the 1-to-10 μW range, if resistive matching $R_{IN} = R_{ANT}$ is assumed. This relatively high Q is mandatory for achieving a suitable value of V_{INp}, i.e. $V_{INp} > \Delta V$, with a low P_{AV}. Taking into account that a high value of Q results in a narrow input bandwidth and that the RF power peaks change with location and time, the tuning frequency f_C must be periodically adapted. This result can be achieved by means of a bank of on-chip binary scaled capacitors [18], [45], as shown in Fig. 3.20.

Driving the control switches, the overall capacitance connected to the input is

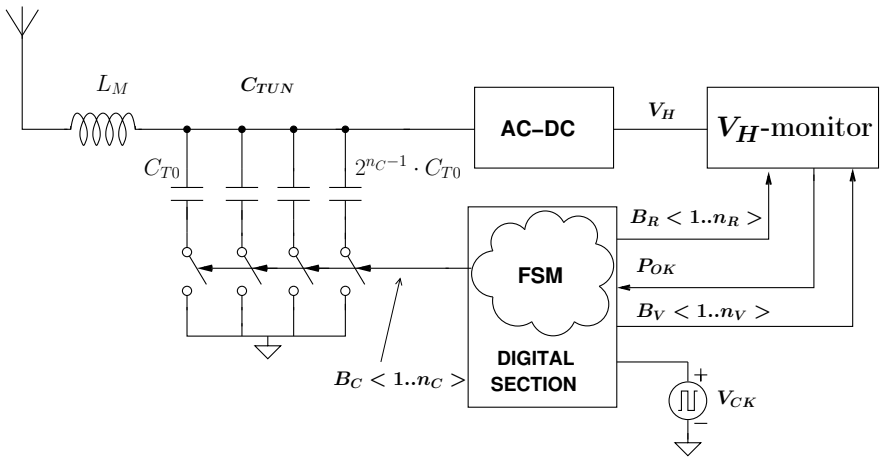

Figure 3.20: Architecture of the proposed MPPT system for RF harvesting.

$C_{TUN} = B_C \cdot C_{T0}$, where B_C is a n_C bits word. Then, with a high-Q value the equivalent input capacitance of the rectifier is increased to $C_{INtot} = C_{IN} + C_{TUN}$. Therefore the tuning frequency f_C is shifted down according to (3.14).
It should be noticed that any resistive mismatch between the antenna (R_{ANT}) and the rectifier (R_{IN}) causes an input power loss (i.e. $\eta_{IN} \equiv P_{IN}/P_{AV} \leq 1$).
Furthermore, the delivered power is strongly affected by the power conversion efficiency of the rectifier, i.e. $\eta_R \equiv P_H/P_{IN}$.
The simulated η_R, with full backannotated layout parasitics, is shown in Fig. 3.21. The bell-shape of $\eta_R(P_{IN})$ is due to the combined effects of the voltage drop ΔV and of the equivalent series resistance R_R. Therefore, the delivered power depends on the input tuning (on the basis of the spectrum of the available RF power, discussed in chapter 2) and on the overall power transmission efficiency, $\eta_T \equiv \eta_{IN} \cdot \eta_R$. From these evaluations and considering the dependence of R_{IN} on V_{H-REF} through R_H, we infer that the RF harvested power is maximized with a concurrent optimization of the tuning frequency and of the overall power efficiency. In our system the overall optimization has been obtained by means of an Maximum Power Point searching and Tracking (MPPT) algorithm, which allows an effective RF harvesting with a very low level of available RF power.

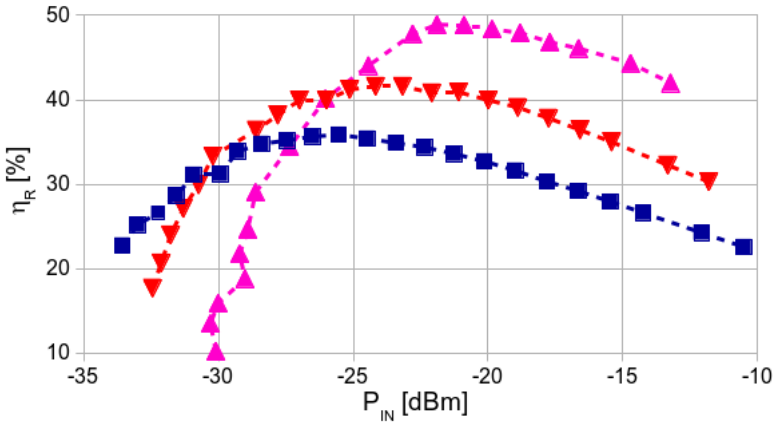

Figure 3.21: Simulated conversion efficiency of the rectifier vs. P_{IN}: Squares: V_{H-REF}=0.8 V, Triangles-down: V_{H-REF}=1.1 V, Triangles-up: V_{H-REF}=1.6 V.

3.3.2 MPPT algorithm

A 3-D MPPT algorithm suitable for the MPPT system developed for the RF harvester is reported in the flow-chart of Fig. 3.22. Differently from other approaches proposed in literature [46], [47], the algorithm acts on three elements during the calibration procedure: the input capacitance, the load current, and the output voltage of the rectifier.

Starting from the minimum value of the array of capacitors connected to the input C_{TUN} (B_C), hence from the upper boundary of the investigated band, the load resistance of the rectifier is progressively decreased by means of the driving bits n_R, until the AC-DC output voltage V_H falls below the detector threshold, V_T (B_V), Fig. 3.23. Here, the tuning frequency is shifted down by means of the bits n_C until V_H rises again up over V_T and the sweep of the load resistance resumes. This routine finishes when the lower boundary of the band is evaluated or when the load resistance reaches the minimum value. When this procedure is completed, the voltage threshold V_T (B_V) is increased and the nested B_C-B_R loops are repeated. The power delivered from the rectifier is calculated by means of the function $PW(B_V, B_R)$, implemented in a lookup

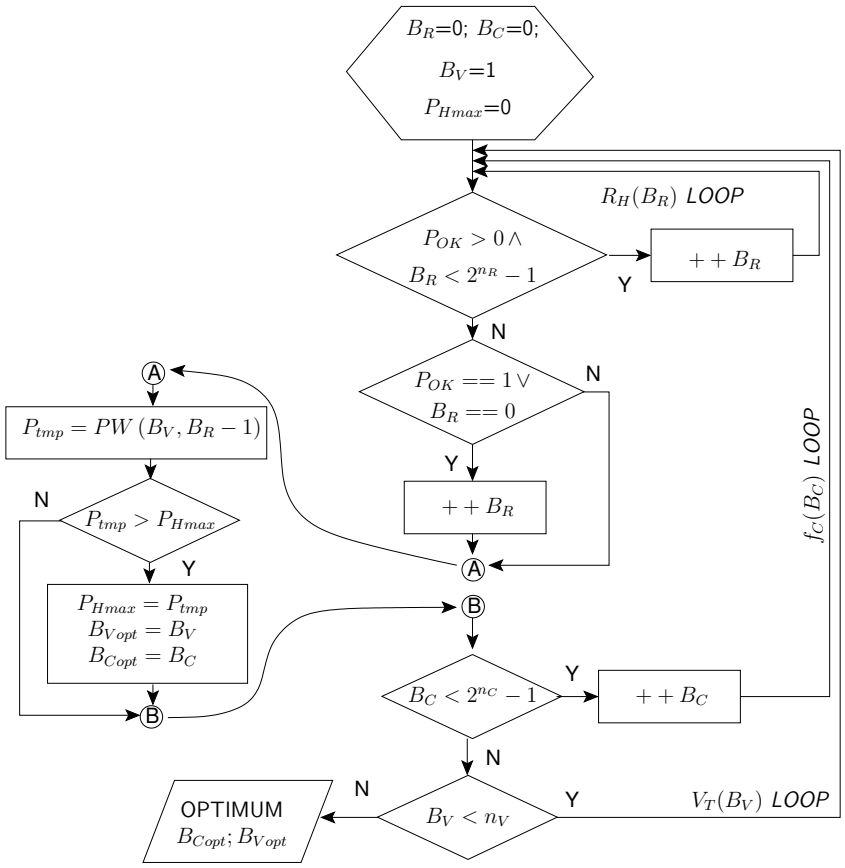

Figure 3.22: Flow-chart of the proposed 3-D MPPT algorithm.

table to reduce power consumption.

The quantization error affecting the obtained value of $PW(B_V, B_R)$ can be reduced by increasing the number of bits n_R, at the cost of a slower search algorithm and hence higher power consumption.

Taking into account that this procedure returns the absolute value of the delivered power P_H, it is mandatory to relate the so-obtained optimum V_T $\left(B_{Vopt}\right)$, and hence of V_H, to the battery voltage V_{BAT}. Therefore, at the end of the 3-loop algorithm the optimum V_{H-REF}, which is derived from V_{BAT}, can be obtained driving V_H-Monitor

with the last calibration code B_R, and connecting V_{H-REF} instead of V_H. The tapping point generating V_{H-REF} must be sweeped until P_{OK} rises up. Finally, the DC-DC converter can be enabled setting R_H to the value B_R, returned by the MPPT flow.
In the current implementation the MPPT algorithm only nests the R_B and f_C loops. The 3-D algorithm can be easily realized with minimum variations of the control finite state machine and of the V_H-Monitor circuit, presented in the next section, and with the addition of the lookup table.
It is worth to be noticed that, differently from other solutions reported in literature [38, 48] which evaluate only the rectifier output current or voltage, the 3-D MPPT algorithm takes also into account the variation of the rectifier power conversion efficiency, for different value of V_H, as shown in Fig 3.21. Moreover, the V_H scan procedure operates on R_{IN} through the load resistance, potentially achieving the resistance matching. By scanning the tuning frequency together with both the output current and voltage, the proposed approach achieves the actual maximum harvested power at the given quantization level. Indeed, at the end of the calibration, the MPPT system tunes the harvester on the B_C, B_R, and B_V configuration where the maximum power is transferred to the load.

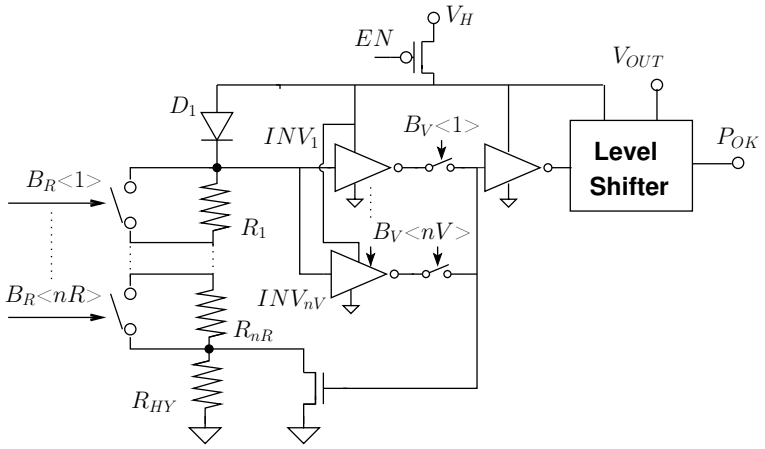

Figure 3.23: Rectified voltage meter for the 3-D MPPT algorithm, with variable load and voltage threshold.

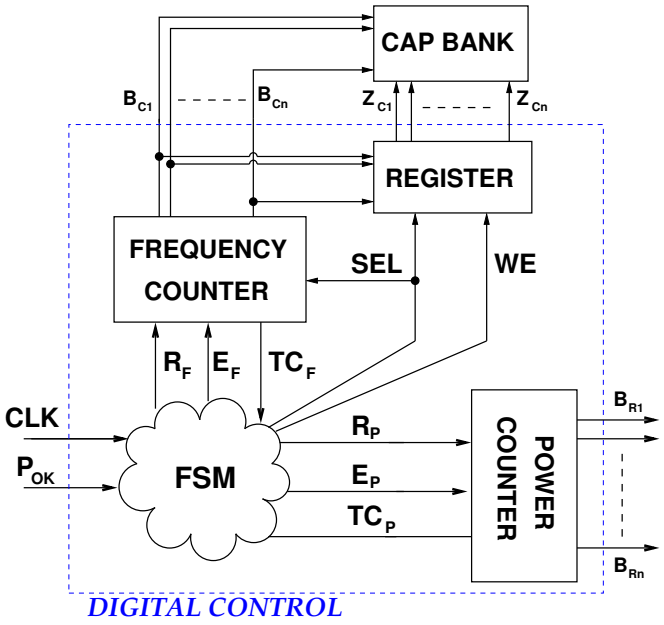

Figure 3.24: Architecture of the MPPT digital control.

3.3.3 MPPT circuit implementation

The proposed MPPT system is based on a rectified voltage meter with a variable load and on a low-power finite state machine (FSM), as shown in Fig. 3.20. When the MPPT circuit is activated the DC/DC converter is disabled (high-impedance) and the voltage meter, shown in Fig. 3.23, is connected to the rectifier output, i.e. EN=0.

3.3.3.1 Bank of capacitors

The bank of capacitors (Fig. 3.20) allows the impedance matching for different values of input frequency f_S, increasing the input frequency range and the matching efficiency. This circuit is used to vary the reactive part of the input impedance, connecting in parallel with the input terminals of the AC-DC converter a sequence of

binary scaled capacitors, generating the equivalent capacitance:

$$C_{TUN} = \sum_{i=0}^{n_c} C_{T0} \cdot (2^i - 1) \tag{3.18}$$

The series switches are driven by the counters of the digital control. This circuit acts as an LC voltage amplifier, with a controlled resonance frequency f_{LC}:

$$f_{LC} = \left(2\pi\sqrt{L_M \cdot (C_{IN} + C_{TUN})}\right)^{-1} \tag{3.19}$$

where C_{IN} is the input capacitance of the RF rectifier and L_M the matching inductance.

Layout accuracies In our implementation, based on the RF power survey reported in chapter 2, the system is designed to improve the matching over the band [770−960] MHz, with $C_{T0} \approx 10$ fF and $n_c = 5$, Fig. 3.25.
A drawback of this approach is the slight, but progessive, decreasing of the quality factor Q_{LC} (3.15), shifting down f_{LC}, due to the increasing input capacitance. On the other hand, the reduction of Q_{LC} enlarges the amplified band, partially mitigating this effect.
The geometry of the layout and the sizes of the metal tracks have huge impact on the performance of the circuit. Indeed, the sweep of the bits $B_C < 1 \ldots n_C >$ can provide non-constant capacitance steps in case of asymmetric layout of the bank of capacitors. Furthermore, the width of the switches of the bank of capacitors has been optimized to provide low series resistance if the switches are closed and low leakage current if they are open.
A trade-off on the sizes of the tracks is necessary. Reduction of the track area means lower parasitic capacitance, but also higher track resistance. In any case the lenght of the track must be minimized. Hence, the sixth and seventh low-resistance layers of metal have been used for the routing and the distances between the devices kept at minimum.
Fig. 3.25 reports the result of post-layout simulations of the whole MPPT system, embedding the RF pads, with RC parasitic extraction.

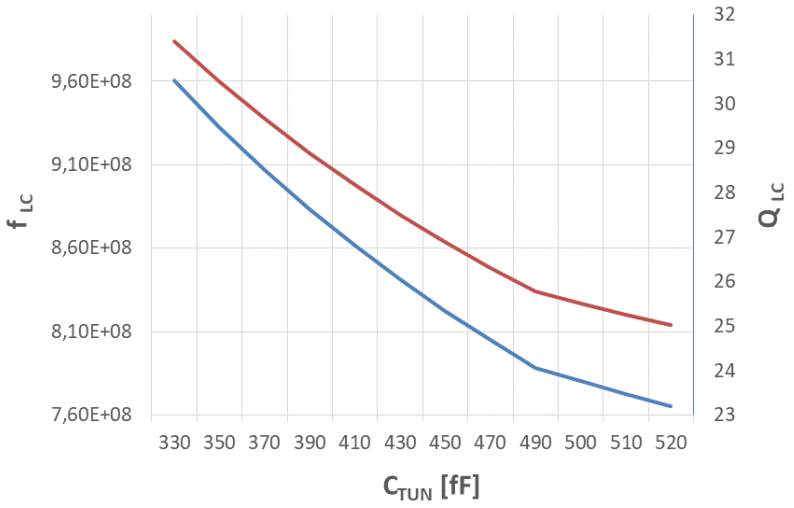

Figure 3.25: Simulated resonance frequency f_{LC} (blue) and quality factor Q_{LC} (red) Vs. equivalent input capacitance C_{TUN}.

3.3.3.2 Finite State Machine

Fig. 3.24 shows the block diagram of the digital control system realizing the MPPT algorithm. The architecture, implemented in the analog domain to minimize the number of states, of gates and hence of area and power consumption, is based on a synchronous finite state machine (FSM) with one-hot state encoding, plus two counters and a register.

The register is used to store the configuration driving the capacitor bank, and thereby select the tuning frequency for RF harvesting. During the scan, the power counter is used to modify the AC-DC load, whereas the frequency counter drives the bank of capacitors. The clock signal is provided by the low frequency oscillator of section 3.1.3.

The state diagram of the FSM is given in Fig. 3.26. The machine is triggered from a reset signal *RST* provided by a high-level FSM, implemented on a FPGA. The *WAIT* state allows the first settling of the output voltage of the AC-DC converter. A preset number of clock cycles is waited before starting the scan operation.

States $SCAN\ FREQ$, $SCAN\ POWER$, and $SCAN\ FREQ\ 2$, driven by the P_{OK} signal generated by the V_H-Monitor, control the progress of the counters and the capacitor bank configuration storage by means of the enable signals E_P, E_C of the counters, and the write enable WE for the register. The FSM enters the possible output states $NO\ POWER$, $LAST\ FREQ$, $MAX\ POWER$, and $LAST\ FREQ\ 2$ based on the signals of terminal count TC_P and TC_F and P_{OK}. The variation of the P_{OK} signal relaunches the MPPT FSM.
It should be noted that it is not necessary the repetition of the whole power-check for every frequency. If the $B_C < 1 \ldots n_C >$ configuration generates $P_{OK} = 1$ for the specific $B_P < 1 \ldots n_P >$ configuration, the next bank of capacitor configuration will have to generate $P_{OK} = 1$ only for the next B_P configuration, to be selected.
On the other hand, it is not necessary to evaluate every other B_C configuration in case one configuration has already generated $P_{OK} = 1$ with the maximum load ($MAX\ POWER$ output state).
The ouput states $LAST\ FREQ$ and $LAST\ FREQ\ 2$ are entered in case the frequency counter reaches the end ($TC_F = 1$), whereas $NO\ POWER$ state represents the situation in which V_H-Monitor is not able to give $P_{OK} = 1$ for the minimum current load.
The FSM has been designed with a small number of states and clock cycles for the digital control, limiting the power consumption, and providing a fast selection of the most promising frequency.

3.3.3.3 V_H-Monitor

The voltage meter V_H-Monitor of Fig. 3.20 embeds a programmable load resistance, replacing R_H of Fig. 3.18 during the MPPT search. Such rectifier load is generated by the binary scaled resistance $R_1..R_{nR}$ and the by-pass switches driven by the n_R-bit word B_R, Fig. 3.23. The rectified voltage V_H, shifted down by a diode voltage drop V_{D1}, is compared with the voltage threshold of a CMOS inverter INV_1. The voltage threshold is set by means of the aspect ratios of the inverter pull-up and pull-down MOS devices.
Considering the effect of V_{D1}, the rectified voltage is compared with V_T, being the

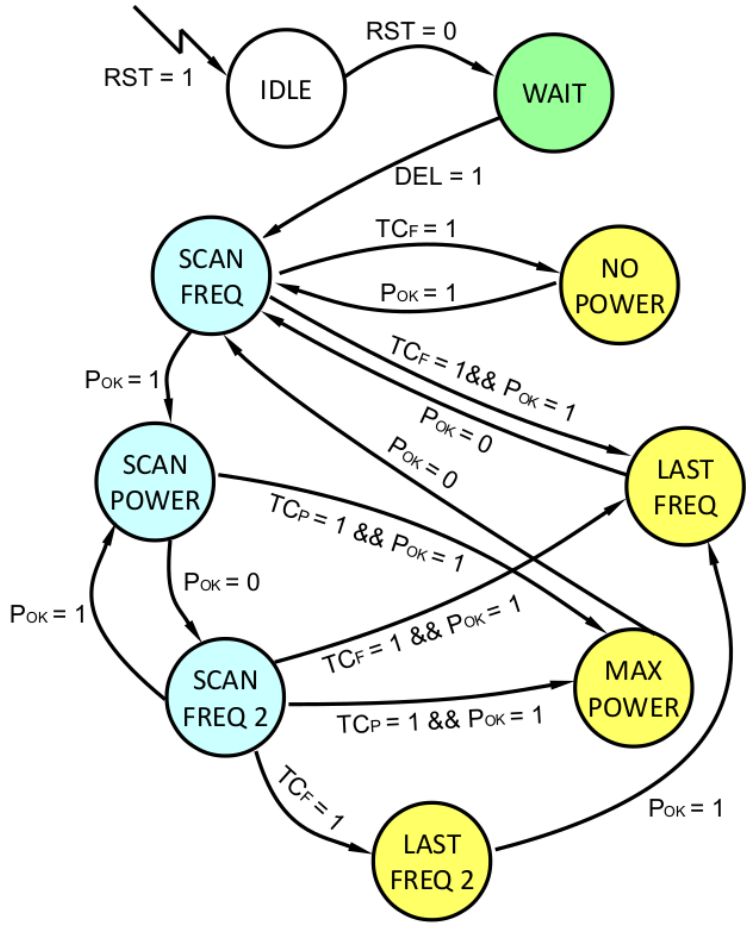

Figure 3.26: State diagram of the FSM controlling the MPPT algorithm. In blue the states controlling the counters, in yellow the output states.

threshold of the voltage meter:

$$V_T = \frac{V_{D1}}{1-K} \tag{3.20}$$

where $K \cdot V_H$ is the voltage threshold of the inverter. Here D_1 is implemented with a diode-connected PMOS transistor in weak-inversion. A hysteresis is introduced in the P_{OK} vs. V_H characteristic by means of the feedback through R_{HY}.

In the circuit shown in Fig. 3.23 many inverters are connected in parallel. This upgraded circuit can be used for the implementation of the 3-D MPPT algorithm. Only one inverter at the time is selected through a series transmission gate, by means of the n_V-bit word in 1-to-n configuration. When INV_j is activated, B_V=j in Fig. 3.23, considering the effect of V_{D1}, the rectified voltage is compared with V_T (j).

3.3.4 MPPT performance and simulation results

Referring to the circuit in Fig. 3.20, the simulated signals obtained nesting B_C and B_R loops at V_T = 0.7 V are shown in Fig. 3.27. Here, two sinewaves were considered at 950 MHz and 860 MHz, with P_{AV}= -26 dBm and P_{AV}= -20 dBm respectively.
At the very beginning of the routine, the MPPT system finds the first suitable fre-

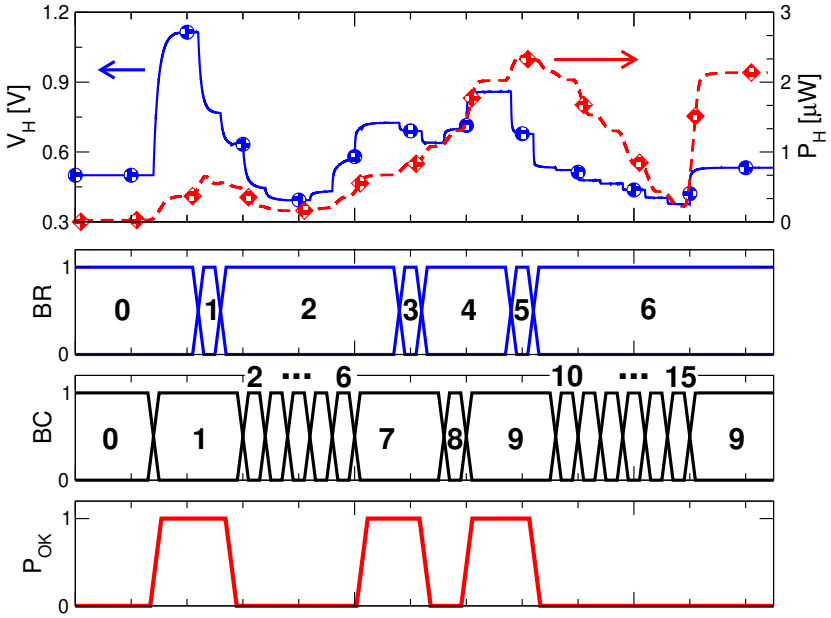

Figure 3.27: Simulated waveforms and digital signals at V_T=0.7 V - Top graph, solid line, circles, left y-axis: rectified voltage - Top graph, dashed line, diamonds, right y-axis: delivered power

Table 3.5: Performance comparison with state-of-the-art RF MPPT systems

	[49]⋆ ISCAS-2010	[46] JSSC-2014	[47]⋆ ISCAS-2015	[40]⋆ ISCAS-2018	[38] CICC-2018	This work⋆ 2018
Technology	130 nm	65 nm	65 nm	180 nm	65 nm	65 nm
Monitor Param.	V_H	V_H	V_H	V_H	V_H	V_H, I_{LOAD}
Sweep Element	X_{IN}	X_{IN}	X_{IN}	R_{LOAD}	R_{LOAD}	X_{IN} , R_{LOAD}
Frequency Range	860-960 MHz	NA	NA	403 MHz‡	NA‡	760-960 MHz
Minimum P_{IN}	-20 dBm	-20 dBm	-20 dBm	-27 dBm	-23 dBm	-30 dBm
Quiescent Current	1.6−2.7 μA	<1μA	NA	<20nA	NA	<50nA
Area [mm^2]	NA	0.3	0.17	0.18	0.06	0.085

⋆Simulated results.

‡ Fixed frequency

quency. Then, after the drop of P_{OK}, the resonance frequency is correclty shifted down, covering with the amplification band of the $R-L-C$ matching the second tone and increasing the harvested power P_H. At the end of the nested B_C-B_R loop the FSM properly selects the tuning frequency corresponding to the maximum harvested power, with $V_H \approx 0.55$ V.

The performance of the designed MPPT system is reported in Tab. 3.5 and compared with the existing state-of-the-art MPPT implementation for RF harvesters.

The systems proposed in [40] and [38] sweep the output resistance R_{LOAD} to operate on the input resistance, as shown in Fig. 3.19, maximizing the rectifier efficiency for a large range of input power P_{IN}. However, these approach designed for RFID systems or other implementations with large amount of available power on a specific carrier frequency are totaly non-flexible and cannot be used for true RF energy harvesting.

The tracking time for the MPPT routine is a misleading parameter due to the strong dependency of this metric on the incoming power and hence it is not taken in consideration in Tab. 3.5. In this work a maximum settling time of 200 μs per MPPT step is considered.

It is worth to notice that solely the proposed 3-D algorithm allows control of both the

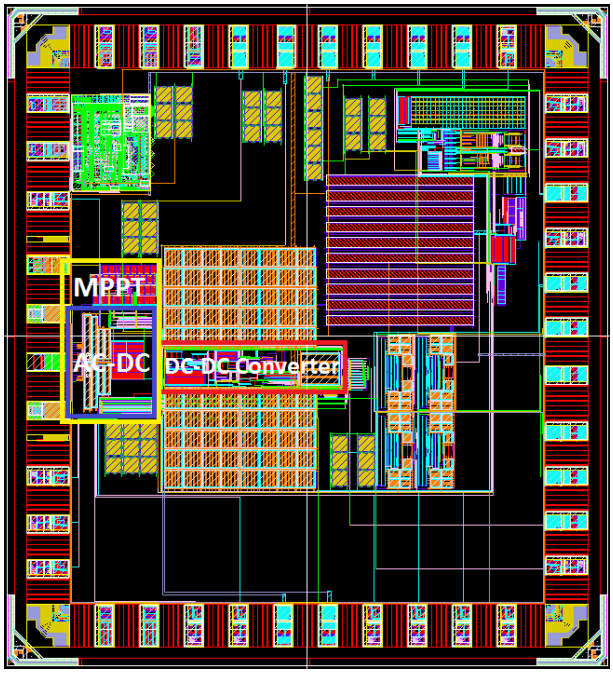

Figure 3.28: Layout of the HarvIC integrated circuit. Highlights: in blue the AC-DC converter, in red the DC-DC converter, in yellow the MPPT system that integrates also the AC-DC converter.

rectified voltage V_H and the output current I_{LOAD}, providing a real tracking of the maximum tranferred power. Furthermore, the combination of this MPPT system with a boost converter capable to adapt the average drawn current and input voltage permits the havester to operate at the maximum transferred power point to the accumulator. This feature can be achieved controlling both the reference voltage and the switching frequency of the DC-DC converter proposed in section 3.1.3. In the presented harvester this feature can be implemented with an external control logic by means of an FPGA, but it could be easily integrated in the digital control in a revised design.
The designed MPPT shows minimum power consumption, which is essentially leakage current of the control section, since, differently from other implementations reported in literature [50], no other circuits are under the general power supply.

3.4 Summary

In this chapter, the design and implementation of an integrated RF Energy Harvester for sensor node applications in CMOS 65 nm technology has been presented.
Fig. 3.28 shows the layout of the HarvIC chip embedding the RF harvester, the temperature sensor with A-to-D converter and the transmitter section [7]. The RF harvester with the MPPT system requires a silicon area of 0.36 mm^2, whereas the whole test chip has an area of 2.7 mm^2.
The RF harvester architecture is composed by the power management section, used for the power transfer from the antenna to the accumulator, and the digital control section, for maximum power point searching and tracking, which operate alternately. Central in the harvester architecture is a strobed DC-DC converter with input control, whose design is based upon an innovative analysis of the energy harvesting from discontinuous ultra low-power RF sources. The proposed architecture can provide auto-adaptive capability to the available antenna power level and to the voltage of the accumulator and it exhibits positive energy balance at extremely low levels of RF power. Results of post-layout simulation, in terms of sensitivity and end-to-end power conversion efficiency (Tab. 3.4), show that the proposed harvester architecture can be effectively used in the urban and semi-urban environments investigated in chapter 2.
To further expand the applicability of the RF harvester, the strobed DC-DC converter has been equipped with a novel MPPT system [8]. A finite state machine combined with a bank of capacitors tunes the input impedance to maximize the output power delivered by the AC-DC converter, whereas a power meter circuit is used for the control feedback.
From simulation results, the implemented MPPT system allows the RF harvester to adapt to mutable environments, drastically expanding its application space, with a negligible impact on the overall power consumption.

3.4.1 Physical implementation

The design of the HarvIC chip has included the padring with fourteen digital pads, twenty five analog pads, and two RF pads for power supplies, digital commands and

testing outputs.
The tiling procedure, used to fill the empty areas with dead devices and bypass the DRC rules, has been the last step before the generation of the GDSII file for the foundry. As mentioned in section 3.3.3.1, particular attention must be paid to the parasitic capacitance and resistance in the RF section. Therefore, the tiling has been avoided under the whole RF section of the chip. Moreover, the RF pads have been custom re-layouted to minimize their parasitic capacitance contribution.
At the time of this writing, the HarvIC integrated circuit, embedding the RF harvester described in this thesis, is being manufactured in Crolles STMicroelectronics foundry (ST 65 nm CMOS technology node with thick-oxide option). The printed circuit board for the testing of HarvIC has been designed and realized.

Chapter 4

PVREF: Ultra Low-Power Programmable Voltage Reference

Systems on chip are becoming more and more complex and are key components in countless portable electronics applications. To display the full potential of SoC in these power-constrained applications, there is a pressing need to equip them with accurate yet low-power voltage references (i.e. bandgap circuits), insensitive to process, voltage supply, and temperature variations (PVT space). Moreover, recently large emphasis has been given to low-power systems including sensor nodes [7] [51], energy harvesters [52], and implantable devices for biomedical applications [53], [54], where the low-power consumption is one of the most relevant design constraints. For these applications, bandgap circuits with average current consumptions in the microampere range, like [55] and [56], cannot be used despite their good performance in terms of temperature coefficient and accuracy.

Voltage references with current consumptions in sub-microampere or nanoampere ranges have been reported in literature [57], [58]. Picoampere voltage references made by few transistors have also been proposed, but normally these circuits show very poor accuracy without an external calibration routine [59].

It is worth noting that the increasing of the complexity in analog and mixed-signal systems, where different voltage supply domains coexist, also requires the capability to

provide simultaneously multiple voltage references [60]. The previously mentioned bandgap architectures do not provide reference programmability. Furthermore, to guarantee the programmability of the voltage reference, external calibrations should be avoided, since they are costly in terms of resources and time [55].
The approach based on digital calibration proposed in [61] does not solve the programmability issue, since it requires the storage of data obtained from external calibrations in an integrated memory. Digital self-calibration procedure is therefore the most suitable solution, since it minimizes the external interaction and allows large flexibility. This approach was already proposed in [62] and [63], but these implementations suffer the drawback of a resistors-ladder architecture. Basing the self-calibration procedure on the resistance cannot provide large programmability range, with nominal current consumption of some nanoamperes, unless very large resistors, with large silicon area, are used. This is due to the limited value of the ratio $resistance/\mu m^2$.
This chapter describes the design, implementation and simulation of an ultra low-power, multiple outputs programmable voltage reference, with digital self-calibration capability. The circuit, named PVREF, is embedded in the NampIC integrated circuit designed at IMEC-NL. PVREF realizes the calibration and the periodic recalibration of four voltage references with an output range from 0.4 to 2.5 V. The self-calibration, based on MOS diodes and resistors, can achieve a large calibration range, with bias currents in the order of few nanoamperes and limited silicon area.
The PVREF mixed architecture, composed by the analog section and the digital control, has been implemented in TSMC 55 nm CMOS technology node, with thick-oxide option, to be integrated in the power managements of energy harvesters, sensor nodes, and biomedical devices. In post-layout simulations with back-annotated parasitic extraction, the circuit has shown remarkable performance in terms of temperature coefficient (TC) and power consumption, compared with the state-of-the-art ultra low-power bandgap circuits and low-power programmable voltage references.

4.1 PVREF architecture

The programmable voltage reference (PVREF) circuit has been designed to provide four programmable voltage references V_{REF}s, with a nominal current consumption per reference I_{DC} in the order of few nanoamperes, over the temperature range [-40−120] °C.

Fig. 4.1 shows the block diagram of the architecture used for the generation of one voltage reference. In the diagram, the accurate voltage reference V_{BG}, generated by means of the bandgap circuit, drives the programmable gain amplifier PGA, used to scale the bandgap reference at a selected value V_{ACC}, in the [0.4 − 2.5] V range. V_{ACC} is compared to the low-power voltage reference $V_{ref-calib}$ by means of a comparator circuit $COMP$. $V_{ref-calib}$ is obtained from a 1nA-current source, biasing a programmable impedance composed by diode-connected MOS transistors and resistors (Z_{CALIB}).

The calibration of the low power reference at the preset value is implemented with a digital control circuit. The digital system periodically verifies the value $V_{ref-calib}$ to compensate any variation of the voltage reference due to temperature changes. In case the temperature changes, the control recalibrates the reference, acting on the programming code of the matrix and modifying the impedance. At the end of the recalibration, $V_{ref-calib}$ is restored at the same voltage, but with different Z_{CALIB} configuration. The duration of the recalibration routine is related to the temperature drift and it is assumed to be much shorter and less power consuming than the first calibration.

At the end of the calibration and recalibration routines $V_{ref-calib}$ is shorted to V_{REF} and connected to a large capacitor, where the calibrated reference is memorized. The capacitor is disconnected during both the calibration and recalibration phases. The output signal of the comparator C_{OUT} is the feedback signal used to close the loop and achieve the calibration of V_{REF}.

When the calibration is completed the digital control enters the stand-by mode, where the circuits generating V_{ACC} and the clock generator for the timing of the FSM are powered down (Sleep phase). This section is highlighted in blue in Fig 4.1. The wake-

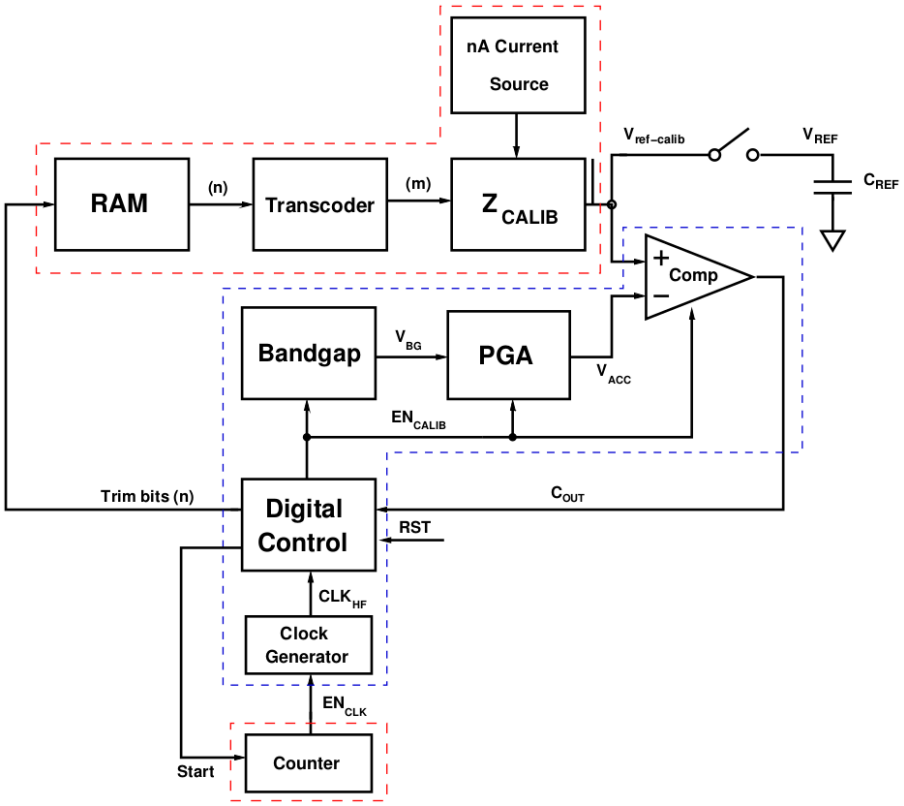

Figure 4.1: Programmable voltage reference architecture. Highlighted in blue: the subsection alternating on and off states. Highlighted in red: the subsection always in on state generating the low power voltage reference.

up signal used to exit the Sleep phase, starting the Recalibration routine, is provided by a low frequency oscillator circuit combined with a binary counter.

A low leakage RAM memory, implemented in the analog domain, is used to store Z_{CALIB} programming configuration and all the other static control bits during the Sleep phase. These bits are used as starting point for the recalibration procedure of V_{REF}, shortening the recalibration time and hence limiting the power consumption.

A transcoder circuit is used to implement in the analog domain the binary-to-

thermometer code conversion used to drive the programmable impedance. This design choice allows a simplification of the digital control, the best logic implementation and a reduction of the leakage current.
In the technology node used for the design of this circuit, the analog and the digital sections belong to different voltage supply domains, hence level shifters are required for the communication between the digital control and the programmable impedance. Thanks to the implementation of the RAM memory in the analog domain, also the level shifter interface can be powered down during the Sleep phase, further reducing the power consumption.
The first calibration after the reset of the PVREF circuit can be divided in three phases. In the first one, diode-connected MOS transistors are connected in series to increase $V_{ref-calib}$, realizing a large-steps voltage ladder. During the second phase, $V_{ref-calib}$ is reduced, with smaller voltage steps, connecting diode-configurated MOS transistors in parallel with the series. In the end, the fine tuning is realized trimming a binary-scaled series resistance. The last part of the calibration routine can be realized both with a successive approximation algorithm (SAR) [64] and a linear sequence of voltage steps.
The recalibration of the reference is based only on the modification of the series resistance to compensate V_{REF} variation, with shorter recalibration time.
The four references share the bandgap circuit, the PGA, the timing circuits and the digital control, whereas the Z_{CALIB}, the RAM, the transcoder, and the comparator are replicated four times.

4.2 Voltage references generators

4.2.1 V_{ACC}: accurate voltage reference

The subsection composed by the bandgap, the Programmable Gain Amplifier (PGA) and the voltage Comparator is periodically turned on, to generate the accurate and programmable voltage reference V_{ACC}, calibrating or recalibrating the low power voltage reference $V_{ref-calib}$.
The bandgap circuit provides an accurate and temperature-stable voltage reference, in

	Min	Typ	Max
V_{DD}	2.8 V	3.3 V	4.2 V
Temperature	-40°C	27°C	120°C
V_{BG}	1.118 V	1.205 V	1.22 V
I_{CC}	235 nA	440 nA	965 nA
Temp. Coefficient	14 ppm/°C	23 ppm/°C	40 ppm/°C
PSRR	-51 dB	-60 dB	-75 dB
Thermal Noise avg.	-	6μV	-
Noise @ 1Hz	-	50 μV	-

Table 4.1: Post layout performance of the bandgap circuit, over the PVT space.

this implementation V_{BG} ≈1.2 V, whereas the PGA guarantees the programmabilty of the reference by means of a selectable voltage gain G, ranging from 0.33 to 2.1. The so-obtained voltage reference is:

$$V_{ACC} = V_{BG} \cdot G \tag{4.1}$$

and it ranges from 0.4 to 2.5 V.
The calibration loop, from the digital control to the analog system, is closed comparing the voltage output of the low power voltage refererence $V_{ref-calib}$ with V_{ACC}, by means of a high resolution voltage comparator.
In the design of this subsection particular attention has been paid to the accuracy and the settling time of the generated reference, and on the power consumption of the circuitry that has to be in the range of few μA during the operative phase.

4.2.1.1 Bandgap circuit

The bandgap circuit generates the accurate and temperature-stable voltage reference V_{BG}. It has been designed to provide V_{BG} = 1.205 V, at room temperature.
The architecture of this circuit is presented in Fig. 4.2. Here, two native transistors

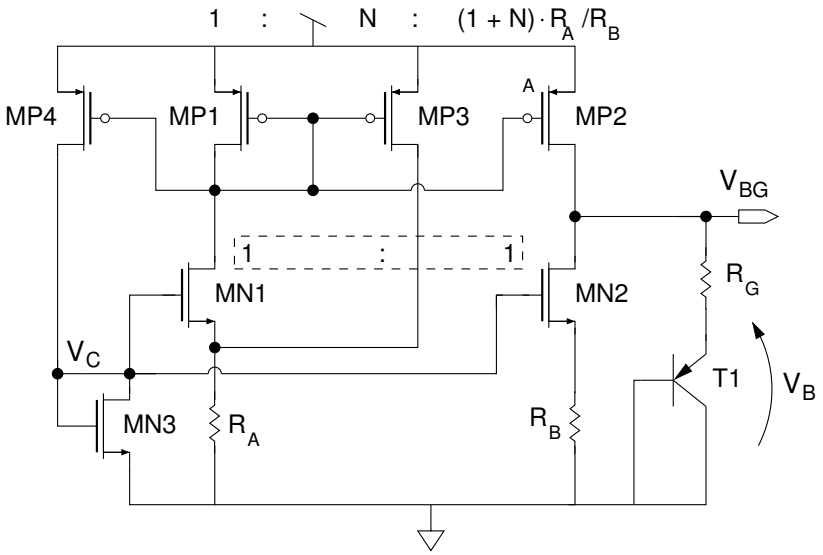

Figure 4.2: Bandgap schematic view.

$MN1$ and $MN2$ have their source terminals coupled to ground trough the resistor R_A and R_B, respectively. The current mirror, made by $MP1$ and $MP2$ with aspect ratio $1 : R_A/R_B$, forces into $MN2$ and the parallel load, consisting of R_G and a diode-connected PNP bipolar transistor, a current R_A/R_B times the current of $MN1$.
The bias current current of $MN2$ is approximately R_A/R_B times larger than the $MN1$ one, if their source voltages V_{S1} and V_{S2} are much larger than their difference.
If $MN1$ and $MN2$ are in weak inversion the difference of their voltage source is:

$$V_D = V_{TH} \cdot ln\left(\frac{R_A}{R_B}\right) \tag{4.2}$$

The diode $MN3$ is used to increase V_{S1} and V_{S2} as well as to keep $MN1$ and $MN2$ in subthreshold region. In the additional branch of $MP3$, the current mirror provides a current N-times larger than the $MP1$ one, allowing the reduction of R_A, with large area saving.
The current provided by $MP2$ is R_A/R_B times the current of $MP1$, hence the current

difference between $MP2$ and $MN2$ is:

$$I_{T1} = \frac{V_{TH} \cdot ln\left(\frac{(N+1) \cdot R_A}{R_B}\right)}{R_B} \tag{4.3}$$

This current difference flows into the branch of R_G and T1, generating the reference voltage:

$$V_{BG} = \frac{R_G}{R_B} \cdot V_{TH} \cdot ln\left(\frac{(N+1) \cdot R_A}{R_B}\right) + V_B \tag{4.4}$$

where V_B is the voltage drop provided by the diode-connected bipolar transistor T1.
This bandgap can operate without any start-up circuit, thanks to the native-based architecture, and it can guarantee high precision, since few transistor structures with critical matching are required.
The values of V_{BG} in post layout simulations, over the process-voltage-temperature (PVT) space, are shown in Fig. 4.3, whereas the other performance parameters of the

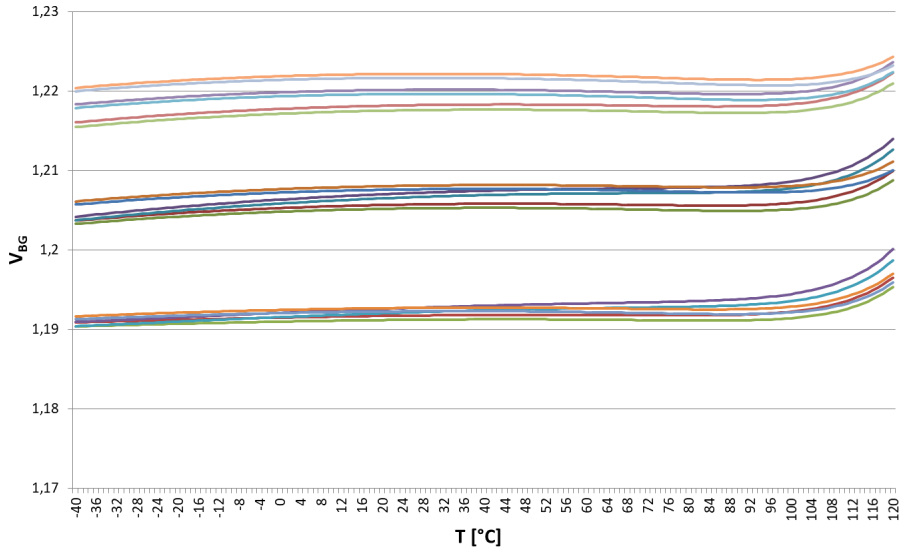

Figure 4.3: V_{BG} variation in post layout simulation, over the process-voltage-temperature (PVT) space.

circuit are reported in Tab. 4.1.
Fig. 4.4 shows the spread of the bandgap reference V_{BG} and of the PGA output with unitary gain $V_{PGA-1V2}$ on process-mismatch Monte Carlo simulation with 400 runs. The average reference value μ, the standard deviation σ, and the percentage normalized reference accuracy σ/μ are also provided.

4.2.1.2 Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) is used to scale the bandgap voltage reference V_{BG} in the range 0.4 V to 2.5 V, Fig. 4.5. The circuit architecture is based on 2-stage Miller operational amplifier with feedback resistor, Fig. 4.6 [65].
The system allows selection of V_{ACC} by means of a digital multiplexer circuit with 5 bits of programmability, among twenty-eight tapping points in the resistor series R_1-R_2, with a resolution of 75 mV.

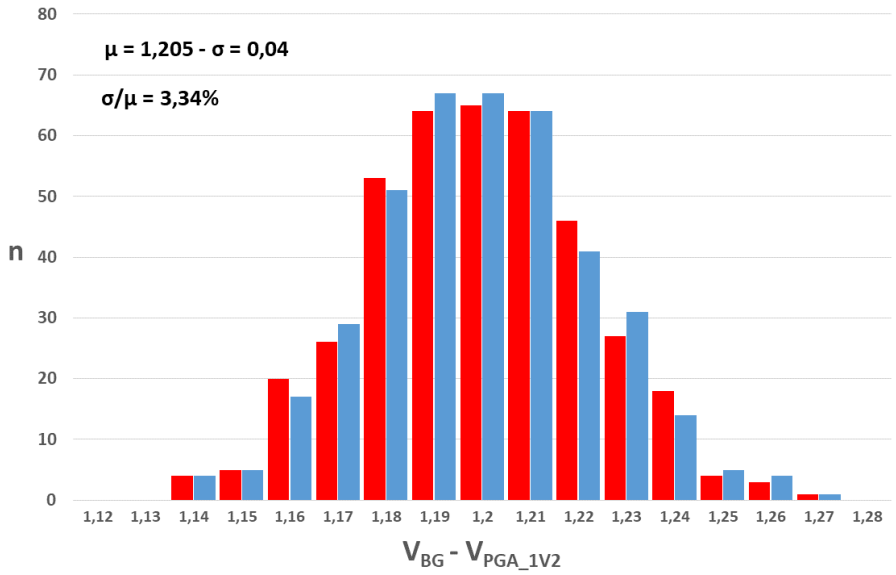

Figure 4.4: V_{BG} (red) and $V_{PGA-1V2}$ (blue), Monte Carlo process and mismatch simulations, 400 runs.

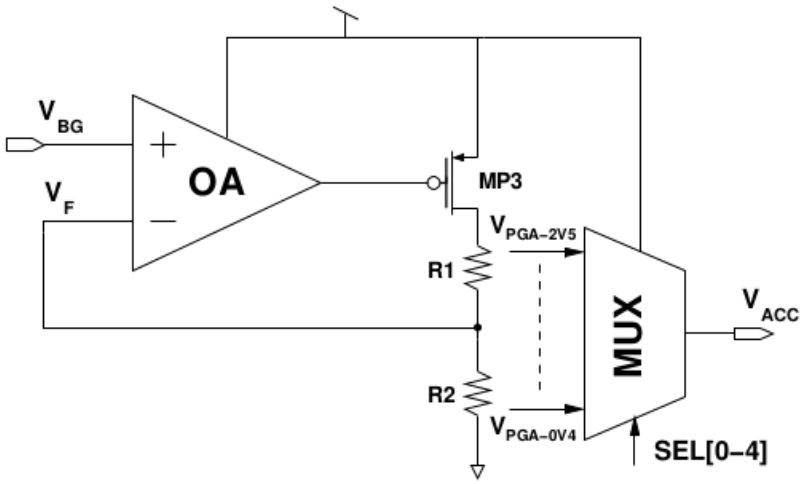

Figure 4.5: PGA architecture with output multiplexer.

Short settling time and low current dissipation were the main targets for the PGA design, whose performance results over the PVT space are provided in Tab. 4.2.
Figs. 4.7 and 4.8 show the spreads of the minimum and the maximum selectable outputs of the PGA ($V_{PGA-0V4}$, $V_{PGA-2V5}$), on process-mismatch Monte Carlo simulation with 400 runs.

4.2.1.3 High resolution comparators

The comparator circuit is used as single-bit quantizer to close the calibration loop. The comparator output C_{OUT} is provided as feedback signal to the digital control subsystem to carry on the calibration algorithm.
Taking into account the large programmability of V_{ACC}, two comparators with different input pairs are used to cover the whole common-mode input range. The comparators operate alternatively depending on the value of V_{ACC}. The bias currents are provided by the bandgap circuit.
The target resolution is $V_{LSB} = 50\ \mu$V, hence high voltage gain is required. Moreover, to guarantee such a small detection threshold no latching or hysteresis are allowed

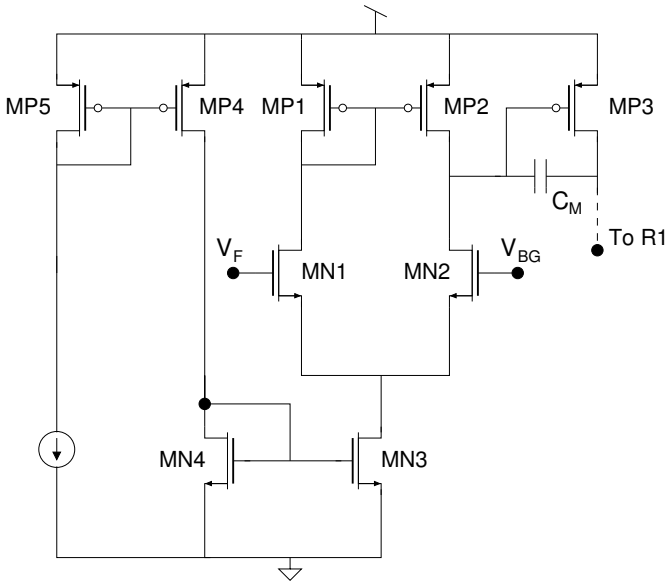

Figure 4.6: Main amplifier of the PGA schematic view.

in these circuits. An architecture made by the cascade of two operational amplifiers, in open-loop configuration, has been chosen, leading to four overall gain-stages, Fig. 4.9.

In this system, the kickback effect in the comparator, combined with the high output impedance of the PGA, could lead to the oscillation of C_{OUT}, for small differential input voltages. In order to prevent this detrimental effect, the full swing of V_{OUT} signal is provided by an inverter chain, pushing the signal commutations far away from the input pair and decoupling the output from the input.

Post-layout simulated performance results of the comparators are given in Tabs. 4.3 and 4.4. In these results, the transition output delay at 50 μV of differential input voltage defines the maximum sampling rate of C_{OUT} that can be used by the digital control. Moreover, it is worth to notice the value of the offset voltage of the preamplifier V_{OSS}, since this undesired effect directly impacts on the voltage reference accuracy.

	Min	Max
V_{DD}	2.8 V	3.6 V
Temperature	-40°C	120°C
I_{CC}	195 nA	310 nA
Settling Time	1.2 ms	3.1 ms
Phase Margin	87°	88°
Gain Margin	31 dB	36 dB
Noise @ 50Hz	0.88 μV	1.3 μV
V_{OSS}	90 μV	560 μV

Table 4.2: Performance of the PGA in post layout simulation.

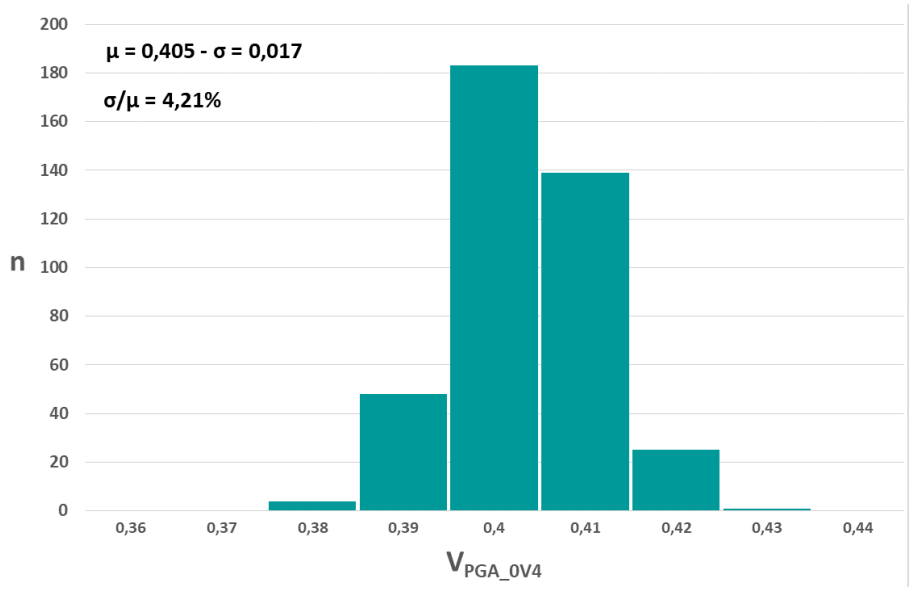

Figure 4.7: Spread of the minimum selectable voltage reference 0.4 V ($V_{PGA-0V4}$), Monte Carlo process and mismatch simulation, with 400 runs.

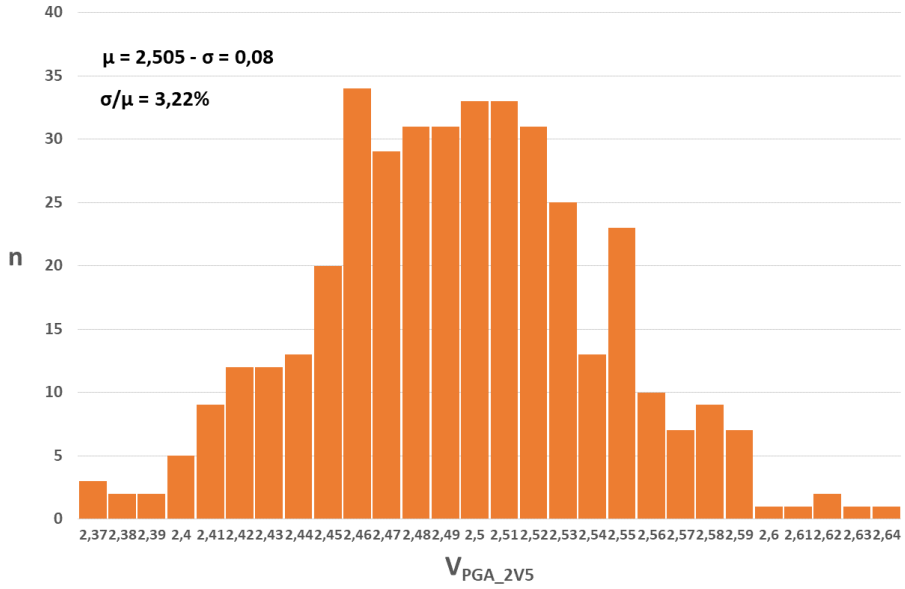

Figure 4.8: Spread of the maximum selectable voltage reference 2.5 V ($V_{PGA-2V5}$), Monte Carlo process and mismatch simulation, with 400 runs.

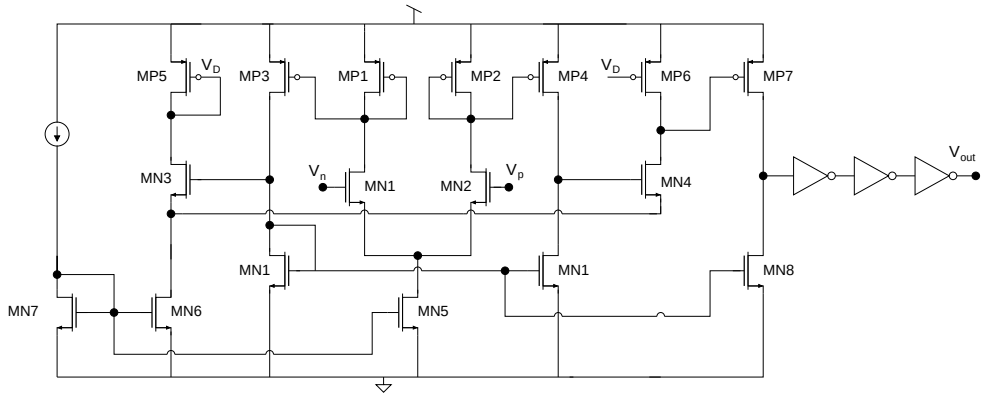

Figure 4.9: Comparator schematic view for V_{ACC} ranging from 0.4 to 1.5 V. For higher values the complementary architecture with pMOS differential pair is used.

	Min	Max
V_{DD}	2.8 V	3.6 V
V_{CM}	0.4 V	1.5 V
Temperature	-40°C	120°C
I_{CC}	-	240 nA
Start-up time	-	500 μs
Tran. delay	50 μs	70 μs
Preamp. stage gain	56.1 dB	67.6 dB
Preamp. stage GBW	1.3M	2.5M
V_{OSS}	80 μV	2.3 mV

Table 4.3: Performance of the comparator for low voltage reference in post layout simulation, over the PVT.

	Min	Max
V_{DD}	2.8 V	3.6 V
V_{CM}	1.5 V	2.5 V
Temperature	-40°C	120°C
I_{CC}	-	250 nA
Start-up time	-	500 μs
Tran. delay	60 μs	80 μs
Preamp. stage gain	54.5 dB	62.3 dB
Preamp. stage GBW	915k	2.1M
V_{OSS}	10 μV	2.1 mV

Table 4.4: Performance of the comparator for high voltage reference in post layout simulation, over the PVT.

4.2.2 V_{REF}: low-power voltage reference

The calibrated reference V_{REF} is generated using the nanoampere current generator (I_{GEN}) (Fig. 4.10) to bias the programmable impedance matrix Z_{CALIB}, Fig. 4.11. In the matrix structure, the MOS diodes were chosen as fundamental devices for their relatively low impedance and therefore low noise, for a given current.
The PVREF system contains four Z_{CALIB} matrices, biased by the I_{GEN} circuit, generating four V_{REF} voltage references. The matrices can be driven simultaneously by the digital control during the calibration and recalibration phases.
To allow fast calibration, the large capacitor storing the value of V_{REF} is disconnected from the output of the Z_{CALIB} during this procedure. Instead, the $V_{ref-calib}$ signal is calibrated and at the end of the calibration V_{REF} and $V_{ref-calib}$ are shorted.
In order to reduce the static power consumption of the digital section of the chip, the calibration codes are stored and transcoded in the analog domain. Indeed, every configuration obtained from the calibration procedure is memorized in a RAM memory during the Sleep phase and converted by means of a binary-to-thermometer digital transcoder. This design choice allows the switching off of the level-shifter interface during the Sleep phase. The circuits generating V_{REF} are always enabled and connected to the power supply.

4.2.2.1 Nanoampere current generator

The nanopower current generator I_{GEN} is used to provide the bias current to the impedance matrix. In this thesis an architecture derived from [66] was chosen, Fig. 4.10. Here, the resistor used in [67] is replaced with the active resistance provided by the nMOS transistor MN5, in triode region. This substitution allows the generation of currents in the nanoampere range using the architecture proposed in [67], with massive silicon area saving.
Altough the circuit proposed in [66] was intended for temperature-compensated current sources, here it is used as proportional-to-absolute-temperature (PTAT) current source. Indeed, the PTAT behavior is exploited to partially compensate the complementary-to-absolute-temperature (CTAT) variation of the voltage threshold of

	Min	Typ.	Max
V_{DD}	2.8 V	3V	3.6 V
Temperature	-40°C	27°C	120°C
I_{REF}	0.7 nA	1 nA	1.3 nA
TC [ppm/°C]	–	3750	–

Table 4.5: Performance of the current source in post-layout simulation, over the PVT.

the diodes composing the matrix. In particular, despite the negligible increase in the generated current with the temperature, the PTAT behavior permits a drastic reduction of the number of the series diodes, required to achieved the maximum value of the reference, and of the parallel diodes, used to overlap the voltage drop provided by a series diode. Therefore, a PTAT current source allows a simplified design of the digital control, in addition to area saving. The performance of the current generator is given in Tab. 4.5.

4.2.2.2 Z_{CALIB} programmable impedance matrix design

To guarantee the programmability of the voltage reference, a digital self-calibration procedure has been considered the most suitable solution, since it minimizes the external interaction and provides broad flexibility. In [62] and [63] the impedance matrix is based on a resistors-ladder architecture that cannot provide large programmability range with ultra low-power consumption unless very large resistors, with large silicon area, are used. Therefore, a different approach for the generation of programmable references is necessary. The implementations proposed in [62] and [63] are able to provide good resolution and the PVREF circuit aims at similar performance. The whole programmability range must be achievable and amenable to calibration with fine resolution (V_{LSB}).
The programmable impedance Z_{CALIB} proposed in this thesis (Fig. 4.11) is based on both diode-connected nMOS transistors and resistors. The programmable impedance matrix is divided in three main subsections:

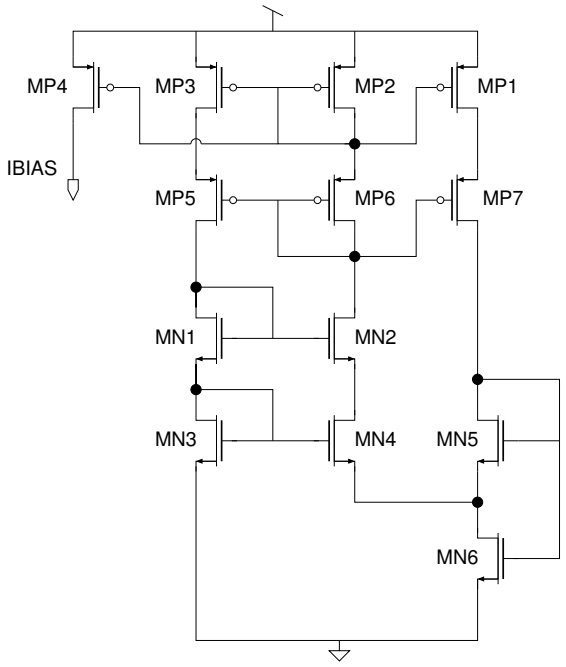

Figure 4.10: Nanoampere current reference schematic view.

- **Series diodes ladder** used to overlap the voltage reference programmability range [0.4 − 2.5] V.
- **Parallel diodes section** used to overlap the voltage drop V_S provided by one MOS diode connected in series.
- **Resistors ladder** used to overlap the voltage drop V_p provided by one MOS diode connected in parallel, and to achieve the required resolution $V_{LSB} \approx 50\mu$V.

The voltage contributions to the calibrated voltage reference $V_{ref-calib}$ of the devices composing the matrix are regulated by means of electronic switches. MOS transmission gates are used for the series diodes and the resistors, whereas nMOS switches are used for the parallel diodes (respectively S_S and S_P in Fig. 4.11).

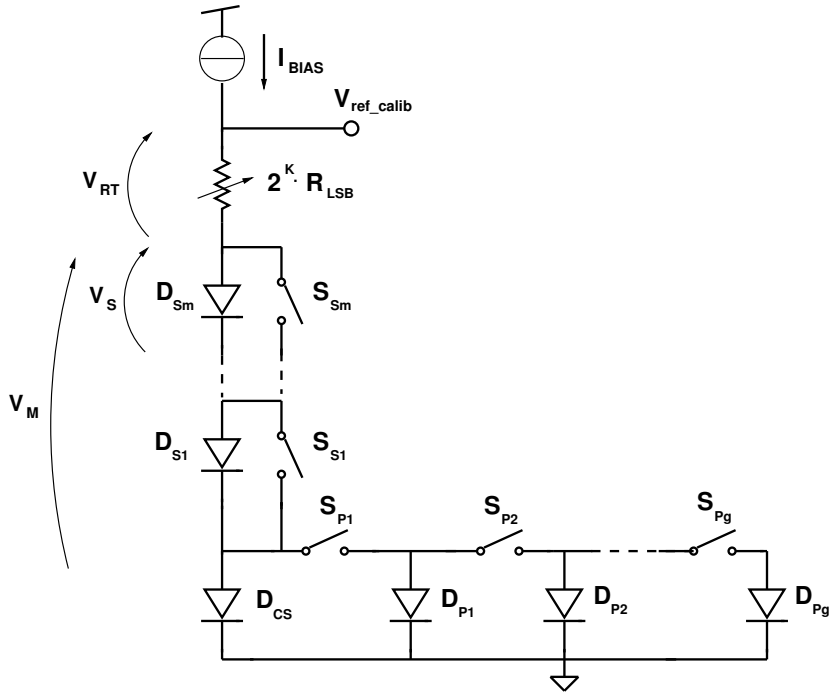

Figure 4.11: Impedance matrix simplified schematic view.

4.2.2.3 Z_{CALIB} devices sizing

The sizing of the devices of the matrix begins with a premilinary consideration regarding the matrix bias current I_{BIAS}. With $I_{BIAS} \approx 1$ nA the MOS diodes are biased in weak inversion region, therefore, the equation that describes the drain current is not anymore quadratic, but exponential:

$$I_{WI} = \mu \cdot C_D \cdot V_{TH}^2 \cdot \frac{W}{L} \cdot e^{\frac{V_{GS} - V_{T0}}{n \cdot V_{TH}}} \tag{4.5}$$

where $V_{DS} > 3V_{TH}$ has been assumed (i.e. the dependence of the current on the V_{DS} has been neglected), μ is the electron mobility, C_D the depletion capacitance, V_{TH}=kT/q the thermal voltage, W/L the aspect ratio of the transistor, and n the parameter that relates C_D to the oxide capacitance C_{OX} ($n \approx 1.45$).

The equation 4.5 can be approximated as:

$$I_{WI} \approx I_0 \cdot \frac{W}{L} \cdot e^{\frac{V_{GS}}{(n \cdot V_{TH})}} \quad @ \quad V_{DS} \geq 3 \cdot V_{TH} \tag{4.6}$$

where I_0 is the sub-threshold diode saturation current, normalized at the aspect ratio. From 4.6, for a MOS transitor in weak inversion, in diode-connected configuration $V_{GS} = V_{DS} = V_{DROP}$:

$$V_{DROP} = n \cdot V_{TH} \cdot \left(ln\left(\frac{I_{BIAS}}{I_0}\right) + ln\left(\frac{L}{W}\right)\right) \tag{4.7}$$

where I_{BIAS} is the current provided by the current source I_{GEN}.
From 4.7, the voltage drop provided by the cornerstone diode (D_{CS} in Fig. 4.11), with m diode-connected MOS transistors of the same sizes in series, is:

$$V_m = n \cdot V_{TH} \cdot \left[(m+1) \cdot ln\left(\frac{I_{BIAS}}{I_0}\right) + ln\left(\frac{L_{CS}}{W_{CS}}\right) + ln\left(\frac{L_S}{W_S}\right)\right] \tag{4.8}$$

The voltage drop provided by the cornerstone diode with g diode-connected MOS transistors in parallel is:

$$V_g = n \cdot V_{TH} \cdot \left(ln\left(\frac{I_{BIAS}}{I_0}\right) - ln\left(\frac{W_{CS}}{L_{CS}} + \sum_{i=1}^{g} \frac{W_i}{L_i}\right)\right) \tag{4.9}$$

The voltage drop provided by the binary scaled, series connected, resistors of Fig. 4.11 is:

$$V_{RT} = 2^K \cdot R_{LSB} \cdot I_{BIAS} = 2^K \cdot V_{LSB} \tag{4.10}$$

with K the number of resistors in series and R_{LSB} the value of the smallest resistor.
Finally, the calibrated voltage reference is given by the sum of V_{RT}, V_m , V_g:

$$\begin{aligned} V_{ref-calib} = \quad & 2^K \cdot R_{LSB} \cdot I_{BIAS} + n \cdot V_{TH} \cdot \left[(m+1) \cdot ln\left(\frac{I_{BIAS}}{I_0}\right) + ln\left(\frac{L_S}{W_S}\right) \right. \\ & \left. - \; ln\left(\frac{W_{CS}}{L_{CS}} + \sum_{i=1}^{g} \frac{W_i}{L_i}\right)\right] \end{aligned} \tag{4.11}$$

Here, the aspect ratios L_S/W_S and L_i/W_i, respectively of the series diodes and of the parallel diodes, are constants.
The sizing of the diodes added in parallel requires a deeper analysis. The dimensions L_i and W_i, and the number g of the parallel-connected diodes must be sized to overlap the voltage step V_S provided by a series diode.
The equation 4.9 can be rewritten as:

$$V_p = (V_g)_i - (V_g)_{(i+1)} \tag{4.12}$$

Therefore, the overall voltage drop V_g can be redefined as:

$$V_g = V_{CS} - \sum_{i=1}^{g} (V_P)_i \tag{4.13}$$

where V_{CS} is the voltage drop provided by the cornerstone device D_{CS} in Fig. 4.11.
Increasing the number of diodes in parallel i generates an exponential reduction of the voltage step V_p per diode, if the devices have the same aspect ratio (Fig. 4.12). Smaller voltage steps with i cause the saturation with $ln(g)$ of the achievable voltage

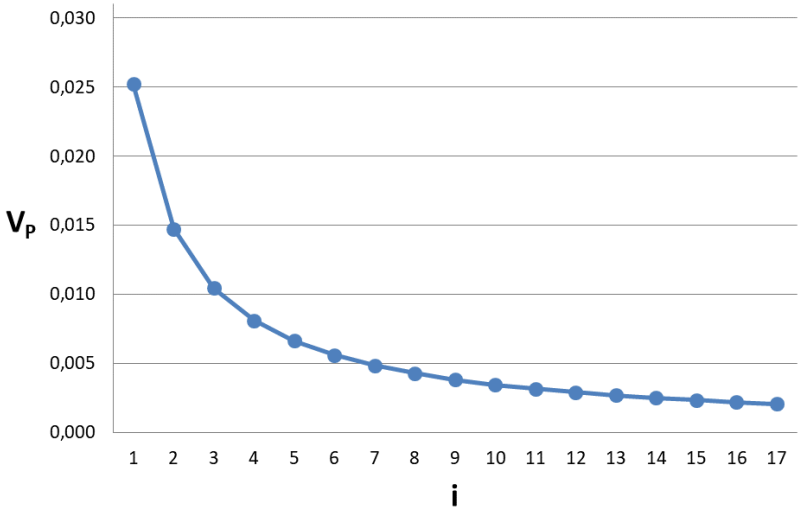

Figure 4.12: V_p provided by the i-th diode in parallel: constant aspect ratios sequence.

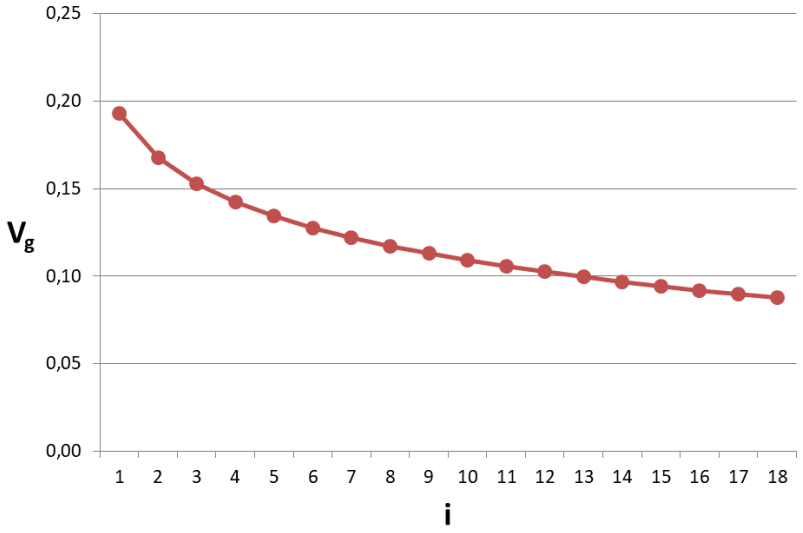

Figure 4.13: V_g provided by i diodes in parallel: constant aspect ratios sequence.

drop V_g, shown in Fig. 4.13. This detrimental behavior can lead to $V_g < V_S$, with missing values in the voltage reference programmability range. To overcome this issue, the diodes in parallel must be sized with an exponential aspect ratio sequence (Fig. 4.14), providing an almost constant voltage step per diode. $V_p \approx 10$ mV in this implementation (Fig. 4.15). The almost constant V_p generates a linear variation of V_g (Fig. 4.16) and it is also used to properly size the overall resistance R_T for the fine tuning.

In conclusion, an exponential sequence of aspect ratios permits the overlapping of V_S with a limited number of devices, thereby simplifying the digital control of the matrix. Moreover, the almost constant V_p leads to the optimum value of R_T.

Fig. 4.17 graphically shows the strategy developed to ensure the coverage of the reference range with the desired resolution. In orange, the D_S blocks represents the series diodes, each one providing the voltage drop V_S. In red, the D_P blocks are the parallel diodes providing the voltage drop V_p. In green are depicted the resistors, each one providing the voltage drop V_R. The sum of the voltage drops provided by

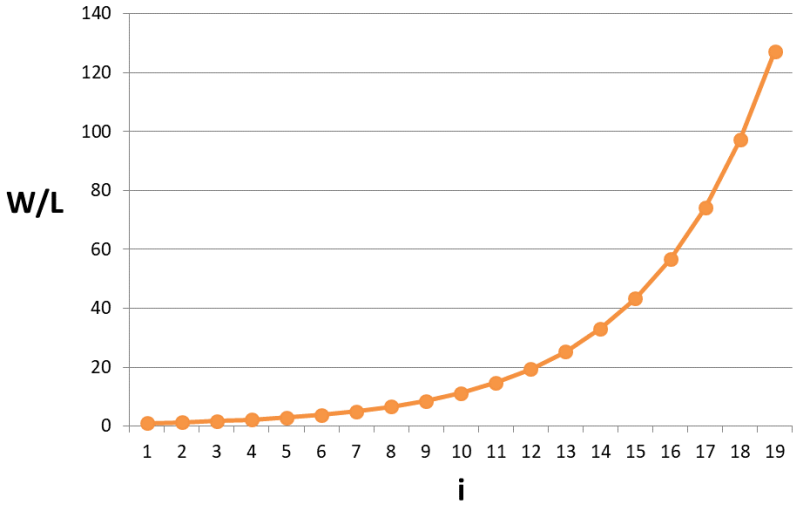

Figure 4.14: Exponential sequence of aspect ratios.

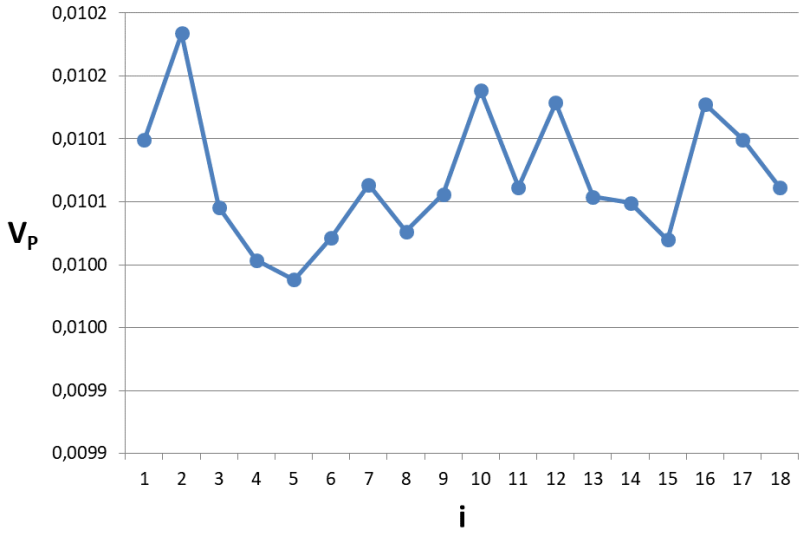

Figure 4.15: V_p given by the i-th diode in parallel: exponential aspect ratios sequence.

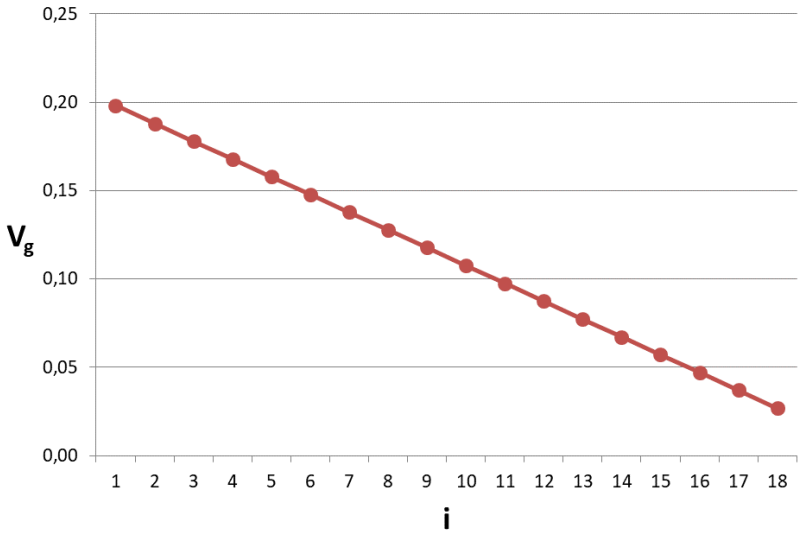

Figure 4.16: V_g given by i diodes in parallel: exponential aspect ratios sequence.

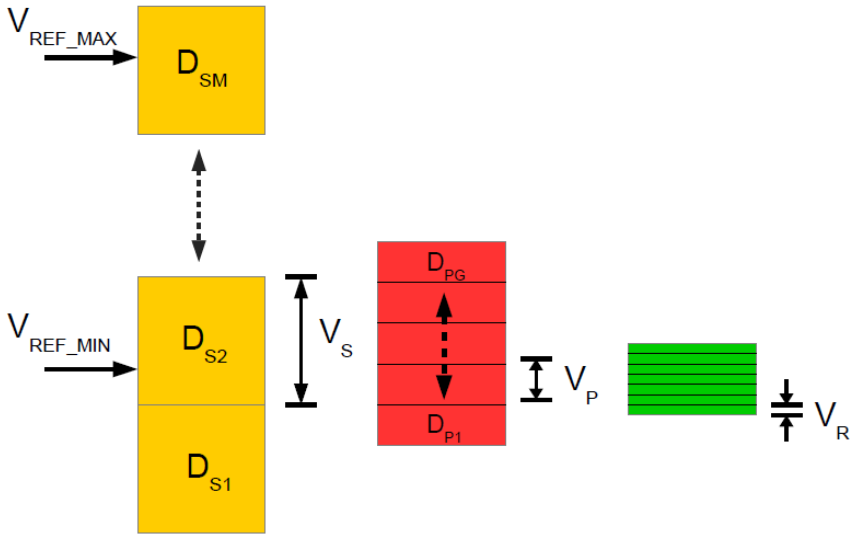

Figure 4.17: Graphical sketch of the matrix voltage sub-sets.

the elements of these stacks are V_m, V_g and V_{RT} of the equations 4.8, 4.9, and 4.10, respectively.
In order to overlap completely the selected voltage reference range, the following constraint must be fulfilled:

$$(V_{m-MIN} - V_{g-MAX}) < V_{ref-MIN} \quad \wedge \quad V_{m-MAX} > V_{ref-MAX} \quad \forall \ T \tag{4.14}$$

where V_{m-MIN} and V_{m-MAX} are the minimum and the maximum of the V_m series, from equation 4.9, V_{g-MAX} is the maximum of V_g, from equation 4.13, $V_{ref-MIN}$ and $V_{ref-MAX}$ are the boundaries of the voltage reference range, and T is the temperature range.
In order to overlap V_S, the following equation must be fulfilled:

$$V_{g-MAX} > V_S \quad \forall \ T \tag{4.15}$$

where V_S is the voltage drop provided by the addition of one diode in series.
Choosing the same device for the two sections of Z_{CALIB} is definitely helpful, since only one temperature coefficient must be taken into account in the matrix design. Moreover, a PTAT current source for the biasing of the matrix partially compensates the temperature drift of V_S, as mentioned in section 4.2.2.1. This design choice reduces the number of diodes both in series and in parallel, simplifying the digital control.
Finally, the voltage step given by the resistance R_T must overlap the almost constant V_p over the whole temperature range. Therefore:

$$V_{RT-MAX} > V_p \quad \forall \ T \tag{4.16}$$

where V_{RT-MAX} is the maximum of V_{RT} given by the resistance R_T. As previously mentioned, a constant V_p allows the optimization of the resistance size.

4.2.2.4 Z_{CALIB} implementation

From the design procedure previously discussed, the impedance matrix Z_{CALIB} has been implemented in TSMC 55 nm CMOS technology. This node provides MOS devices with different voltage thresholds. To satisfy the inequation 4.14 an extreme

low voltage threshold device ($elvt$) was chosen for the MOS diodes and as cornerstone diode D_{CS} in the matrix. The low voltage threshold of this transistor allows $V_{ref-calib}$ < 0.4 V, over the PVT space.
As previously mentioned, the PTAT current source I_{GEN} is used to partially mitigate the CTAT variation of the devices threshold voltages and the resulting variation of V_S and V_p. However, an oversizing with respect to the nominal case, with T = 27 °C and typical process, is necessary.
The variation of V_S for an $elvt$ device over the PVT gives the number of D_S to achieve the upper boundary of the V_{ref} range and it has been computed as $m = 41$. In this work, V_m must satisfy constraint 4.14 with $V_{ref-MAX}$ = 2.5 V, T up to 120 °C and low threshold voltage devices.
The value $g = 54$ has been chosen to fulfill the inequality 4.15 with T down to -40 °C, and high threshold voltage devices. To limit g the D_S diodes have larger aspect ratio compared with D_{CS} and hence they generate smaller V_S.
In this technology the resistance has smaller absolute temperature coefficient with respect to MOS devices. Therefore the compensation derived from the PTAT current source is more effective.
In the Z_{CALIB} implementation, from an almost constant $V_p \approx 10$ mV and a nominal current I_{BIAS} = 1 nA, R_T = 25.6 MΩ was chosen for the fine tuning of the reference. The target resolution $V_{LSB} \approx 50$ μV is obtained with binary-scaled resistors, R_{LSB} = 50 kΩ, and $K = 9$. The resistance was implemented with high density poly-silicon resistors to limit the occupied area.
In conclusion, the proposed approach allows $V_{ref-calib} \in [0.4-2.5]$ V, with a voltage step $V_{LSB} \approx 50$ μV, over the PVT space. A calibration range in the order of Volts can be completely covered with a resolution in the order of μVolts, with a tremendous silicon area saving compared with resistor-based solutions, such as [62] and [63], at the same current consumption.

4.2.2.5 RAM memory and digital transcoder

The pass-gates and the switches controlling the matrix of Fig. 4.11 are driven with a well-defined command sequence from the digital control. The calibration code is sent

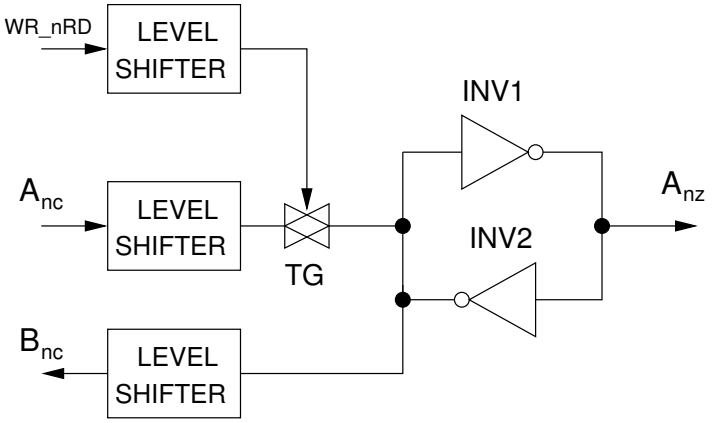

Figure 4.18: Single bit RAM cell schematic view.

to the matrix passing through a level shifter interface (A_{nc} inputs), a RAM memory and a digital transcoder. The 21-bits code is divided in three parts, one per matrix section, generated by three binary counters. The RAM implemented in the analog domain is used to store the code during the Sleep phase (Fig. 4.18).

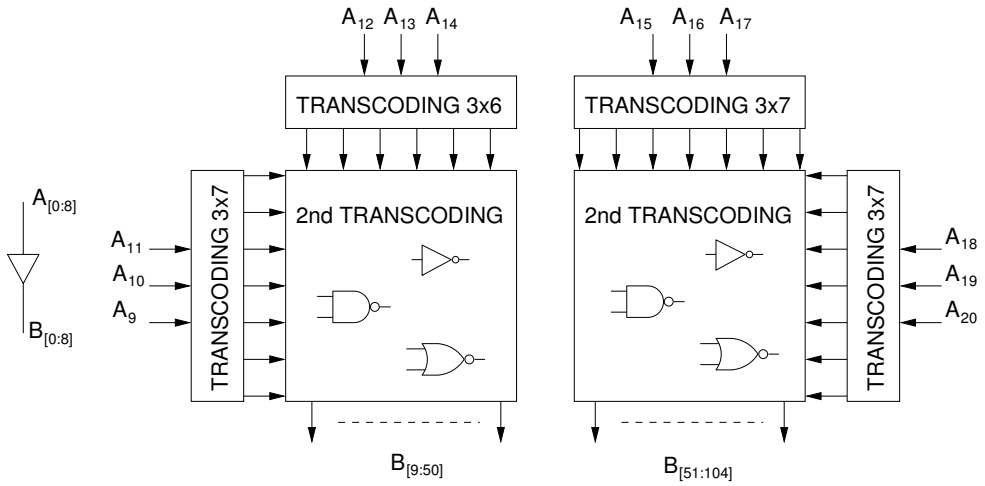

Figure 4.19: Transcoder architecture.

The digital transcoder, also designed in the analog domain, implements binary-to-thermometer code conversion of two of the binary codes generated by the digital control (Fig. 4.19).
The $A[9-15]$ bits from the digital control encodes the control of the diodes in series, whereas the $A[16-21]$ bits drive the the parallel diodes section. The $A[0-8]$ bits for the binary scaled resistors section are only buffered, since with binary counters in the digital control no conversion is required. The memory drives the transcoder with the calibration code by means of the output signals A_{nz} and during the Sleep phase of the digital control it also memorizes the other static bits.
The RAM memory is composed by single bit RAM cells, each one being a latch made by the cascade of two not gates in feedback (Fig. 4.18). The RAM is accessible with the write-not-read command $WR-nRD$. The digital control receives the starting code for the recalibration from the RAM with the B_{nc} feedback bits.
The thick-oxide technology option guarantees null leakage current through the gate terminal of the logic gates in the transcoder, allowing the data retention. Indeed, in addition to increased static power consumption, large leakage currents through the logic gates could cause the loss of the logic value 1.
The digital control and the memory belong to different voltage supply domains, therefore a level shifter interface is located between them. In the Sleep phase, the interface is powered down to limit the static power consumption and every memory cell is disconnected from the digital bus to maintain the stored data with the transmission gate TG.
One binary-to-thermometer transcoder per matrix explodes the 21-bit digital code in the 102-bit code, driving the switches of the matrix. In the binary-to-thermometer code conversion N inputs generates $2^N - 1$ outputs. From the previous section $m = 41$ and $g = 54$. Therefore, $N = 6$ is required in the binary counters, although not every code must be generated.
Shifting the code conversion in the analog domain allows better control of the leakage current of the transcoder with the sizing of the transistors.

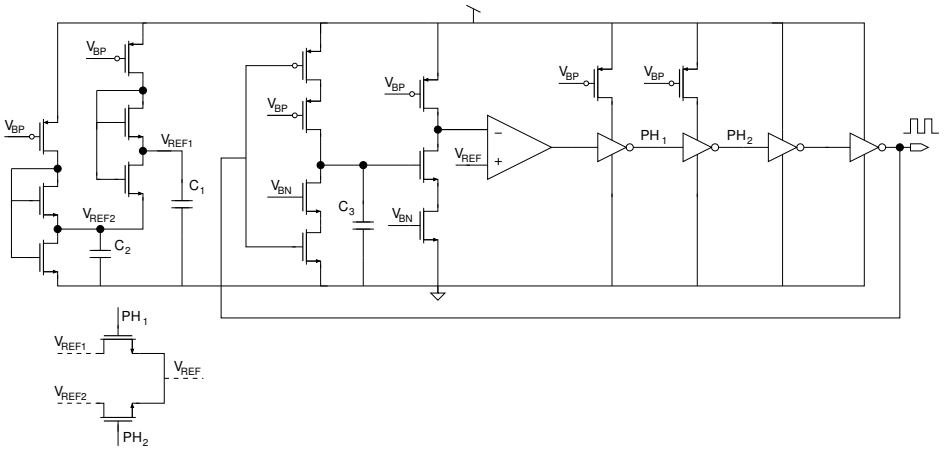

Figure 4.20: Low frequency oscillator schematic view.

4.3 Timing circuits

Two oscillator circuits are used for the synchronization of the system. In particular, a low frequency oscillator (Fig. 4.20) combined with a programmable binary counter separates the Calibration phase from the Sleep phase. The counter provides the wake-up signal for the digital control after the Sleep phase. This circuit can be externally trimmed and the PVREF system has been designed for a sleep time t_{sleep} ranging from 25 ms to 6.4 s.

The oscillation frequency of the slow oscillator is related to the size of the capacitor C_3 and to the voltage thresholds V_{REF1} and V_{REF2}, between which it is forced to rebound the negative input of the operational transconductance amplifier. The voltage references V_{REF1} and V_{REF2} are obtained from two branches biased with I_{bias} = 250 pA.

The chain of inverters (starved and non-starved) provides a clock signals with full CMOS swing, with a limited current consumption.

A current-starved ring oscillator is used to provide the clock signal to the digital control and it is the time base for every digital function (e.g. counting, sampling, averaging), Fig. 4.21.

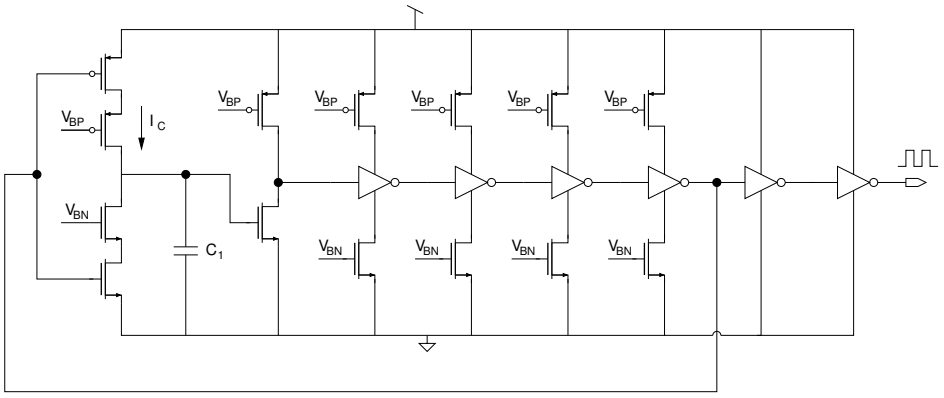

Figure 4.21: High frequency oscillator schematic view.

The operative frequency of this oscillator f_{HF} has been sized to fit the settling time of the smallest voltage step in the matrix (V_{LSB}).
The low frequency oscillator and the counter are always active, whereas the high frequency oscillator is powered down during the Sleep phase. The main performance of the oscillators are reported in Tab. 4.6.

	Min	Max
V_{DD}	2.8 V	3.6 V
Temperature	-40°C	120°C
I_{CC-LF}	1.3 nA	4 nA
f_{LF}	23 Hz	40 Hz
I_{CC-HF}	20 nA	50 nA
f_{HF}	23 kHz	50 kHz

Table 4.6: Post layout performance over the PVT of the low and high frequency oscillators, respectively.

4.4 PVREF digital control

The block diagram of the digital control is shown in Fig. 4.22. The architecture is divided in multiple finite state machines, at different hierarchical levels. The clock signal for the digital section CLK_{HF} is provided by the high frequency oscillator (Fig. 4.21).
The top-level finite state machine is shown on the left of the diagram. This section interacts with the oscillators and the counter and it communicates with a FPGA by means of a serial peripheral interface (SPI). This interface transmits to the digital control system the settings for the calibration the PVREF in terms of timing, calibration mode, and number and values of the references to be calibrated.
At the top-right, the $Calibration\ control$ FSM, managing one voltage reference, is shown. This section is responsable for the calibration and the recalibration of $V_{ref-calib}$, as well as for the all the other correlated functions such as the enabling of the power supplies of the analog circuitry and the writing of the RAM memory. This sub-part is replicated three times for the control of the other references.
The digital control generates the $REF\ ctrl\ code$ and it receives the output of the comparator CMP_{OUT} as feedback signal to implement the calibration procedure. $A_{OUT} < 0 : 20 >$ output pins are used to communicate with the analog domain.
$REF\ ctrl\ code$ made by the $A_{OUT} < 0 : 20 >$ pin is organized as follow:

- $A_{OUT} < 0 : 8 >$ for the control of the resistors in Z_{CALIB} (fine tuning). The digital control can actuate a successive approximation algorithm (SAR) from the (MSB - 1)-th bit or a standard binary count. The default output configuration is in the middle of the count.

- $A_{OUT} < 9 : 14 >$ for the control of the series diodes in Z_{CALIB} (coarse tuning). The digital control can run up-down count till 41. The code conversion is realized by the transcoder circuit of section 4.2.2.5. The default output configuration is 41.

- $A_{OUT} < 15 : 20 >$ for the control of the parallel diodes in Z_{CALIB} (medium tuning). The digital control can run up-down count till 54. The code conver-

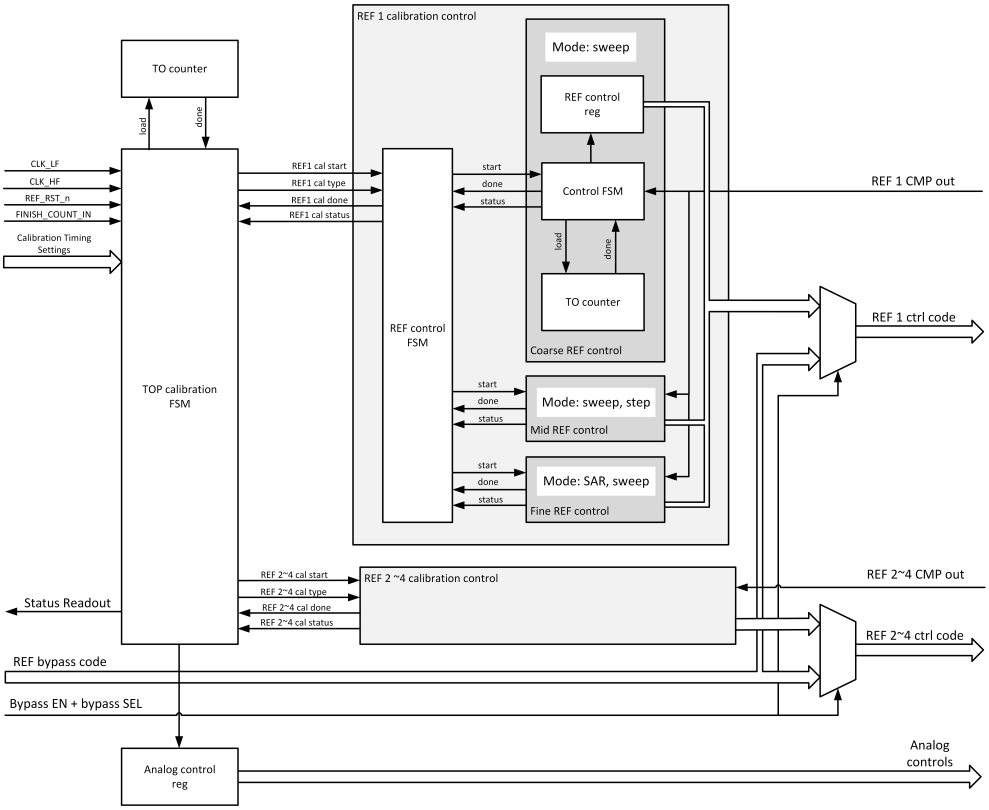

Figure 4.22: Block diagram of the PVREF digital control.

sion is realized by the transcoder circuit of section 4.2.2.5. The default output configuration is 0.

The RAM memory is used to store the $A_{OUT} < 0 : 20 >$ bits and the other static bits during the Sleep phase. In particular, in case the first calibration is successfully accomplished the C_{VAL} bit is set high. The $REF\ ctrl\ code$ and the C_{VAL} bits are used as starting point for the recalibration procedure after the Sleep phase, shortening the time required for this routine, with large power saving.
The algorithm for the calibration of the voltage reference $V_{ref-calib}$ has been developed starting from the matrix architecture of Fig. 4.11. After the reset of the system,

the digital control carries out the first calibration. At the beginning of the routine, the diode-connected MOS transistors are added in series until $V_{ref-calib}$ rises above the accurate voltage reference V_{ACC}. Then, the sweeping of these diodes is stopped. In the second phase, MOS diodes are added in parallel, providing smaller steps in the opposite direction, until $V_{ref-calib}$ drops below V_{ACC}. Finally, after the end of the diodes sweeping phases, the control implements the fine tuning acting on the binary scaled resistance R_T.

When the calibration is completed, the digital control enters the Sleep phase, powering down the circuits and enabling the counter $COUNT_{CLK}$. When the count is over, the counter generates the wake-up signal to enable again the clock signal, restarting the digital control.

After the restart, the digital control actuates the recalibration routine, that operating on the resistance restores V_{REF} in case of temperature variations. The fine tuning can be implemented driving the resistor switches with the SAR algorithm or with the binary count. The SAR algorithm requires an average number of steps lower than the binary sequence, although it also requires longer and not-constant settling times for different bits.

The addition of different devices in the Z_{CALIB} matrix configuration causes voltage steps with different settling times, therefore the binary counters for the calibration have different periods, depending on the controlled matrix section, derived from the primary clock signal.

Both calibration and recalibration routines can implement the averaging of the less significant digit, sampling the comparator output for a preset number of clock cycles.

The digital control has been descripted in Verilog and synthetised in TSMC 55 nm CMOS technology, with voltage supply of 1.2 V and a post-synthesis gate count of 6005.

The post-synthesis power estimation, with typical process at 25°C, returns a stand-by current consumption $I_{SB} \approx 3.75$ nA and a dynamic current consumption $I_{DYN} \approx 1.5$ μA per reference.

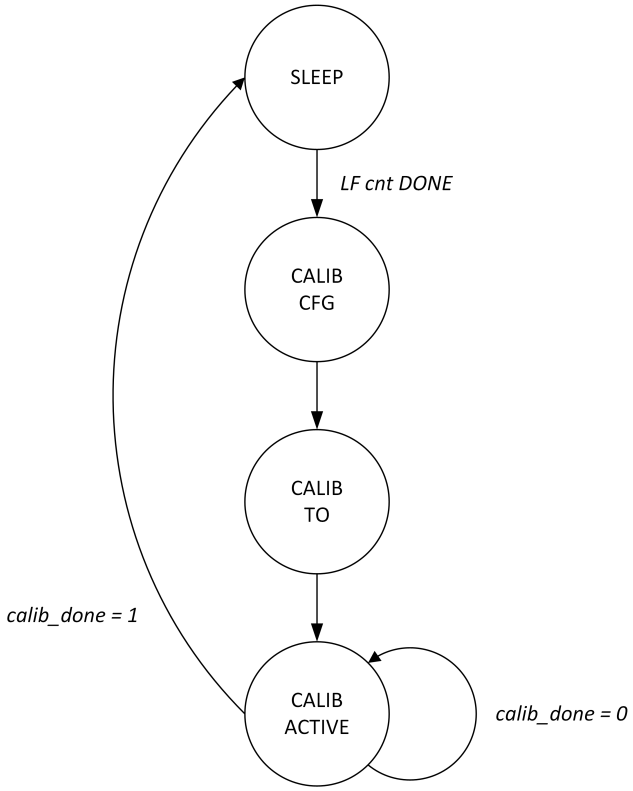

Figure 4.23: *Calibration control* finite state machine.

4.4.1 Finite state machines

The calibration procedure is controlled by hierarchical finite state machines. The top-level finite state machine is shown in Fig. 4.23. When the digital counter $COUNT_{CLK}$ ends the count the FSM exits the $SLEEP$ state. The digital control passes through the verification of the calibration configurations and the $CALIB\ ACTIVE$ state actuates the calibration or recalibration routine.

Fig. 4.24 shows the state diagram of the finite state machine controlling the calibration of one voltage reference. The states $COARSE\ CAL$, $MEDIUM\ CAL$, and $FINE\ CAL$ realize the calibration routine with the series diodes, the parallel diodes

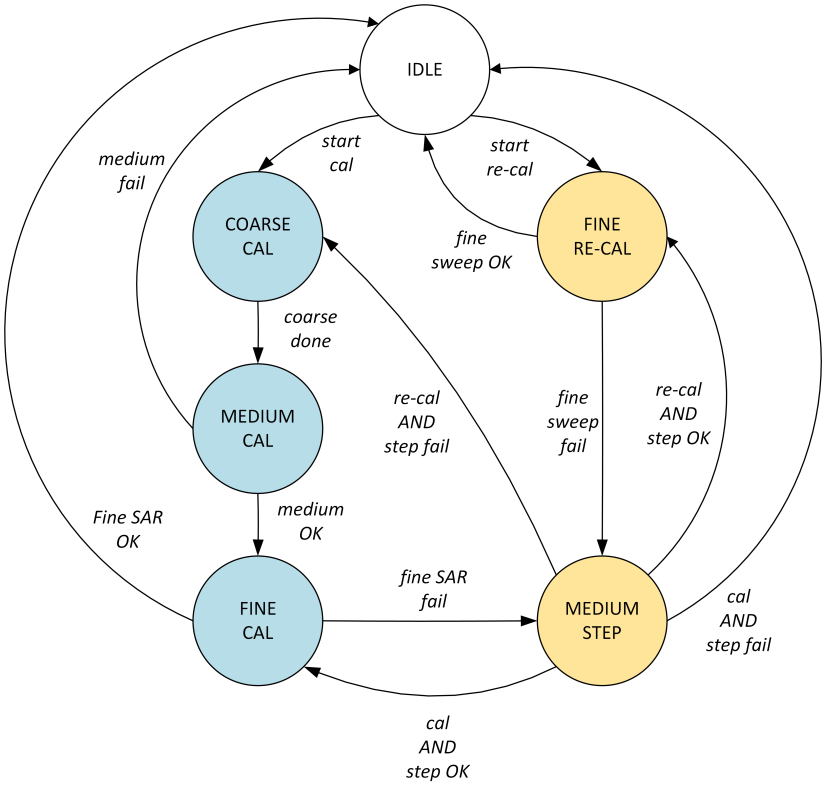

Figure 4.24: State diagram of the FSM for the calibration of one reference. In blue, the states referring to the first calibration. In orange, the states for the recalibrations.

and the resistors, respectively. The states $FINE\ RECAL$ and $MEDIUM\ STEP$ refer instead to the recalibration procedure with resistors and parallel diodes. The $MEDIUM\ STEP$ state has been added to cope with the case where the fine recalibration with resistors fails. Indeed, if the temperature drift during the $SLEEP$ state exceeds the maximum drift that can be compensated with the resistance sweeping in the recalibration routine, the state machine would be locked in an undefined state. To avoid this problematic situation, the $MEDIUM\ STEP$ state has been added, to sweep again the parallel diodes, extending the recalibration range. In case the voltage drift due to temperature variation still exceeds the recalibration range, the finite state

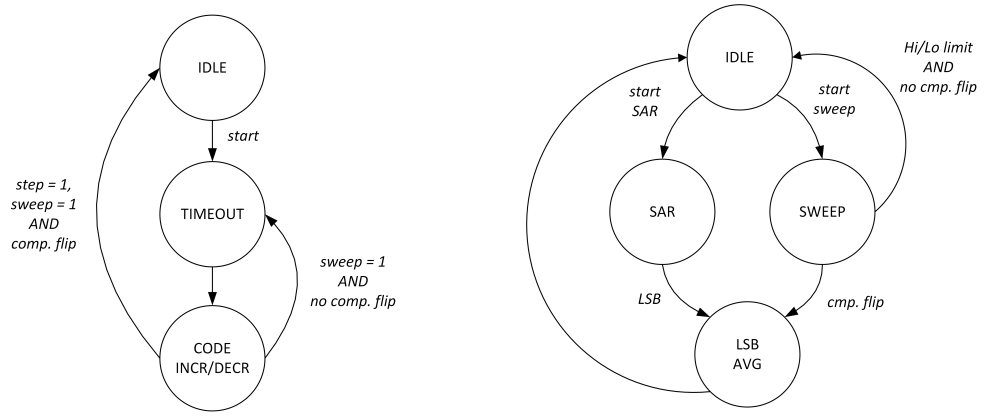

Figure 4.25: State diagram of the FSMs for the fine tuning. On the left, the resistance sweeping. On the right, the high level FSM.

machine relaunches a complete calibration.
The state diagrams of Fig. 4.25 show the sequence of states for the calibration and recalibration routines in the fine tuning phase. On the right it is depicted the high-level FSM, with both the SAR algorithm and the linear sweeping of the resistance. The state diagram of the machine regulating the linear sequence of resistors is shown on the left.

4.5 System performance and mixed-signal simulation results

The programmable voltage reference has been designed, implemented and simulated in TSMC 55 nm CMOS technology, with thick-oxide option. The PVREF circuit is embedded into the NampIC integrated circuit, which includes also an ultra low-power charge pump. The layout of the NampIC chip is shown in Fig. 4.26.
The PVREF circuit has been designed to provide accurate and programmable voltage references, with minimum power consumption compared with the state-of-the-art voltage references. The power consumption, expressed in terms of drawn DC current

I_{CC}, is one of the fundamental metrics.

Taking into accout that PVREF has been designed to alternate operative and stand-by phases and that the average current is given by the weighted sum of the I_{CC} in these phases, to reduce the power consumption at system level it is necessary to shorten the active time as much as possible. To keep short the active phases, with small settling error, the settling time of every voltage step during the calibration must be minimized. Therefore, the layout of Z_{CALIB} was made as compact as possible, with short and large tracks to limit the parasitic capacitance and resistance.

Mixed-signal transient simulations were performed, with back-annotated parasitic layout (R-C), to verify the performance at system level and to evaluate the impact of the layout on the settling times during the calibrations.

Fig. 4.27 shows transient response of the system when four voltage references are

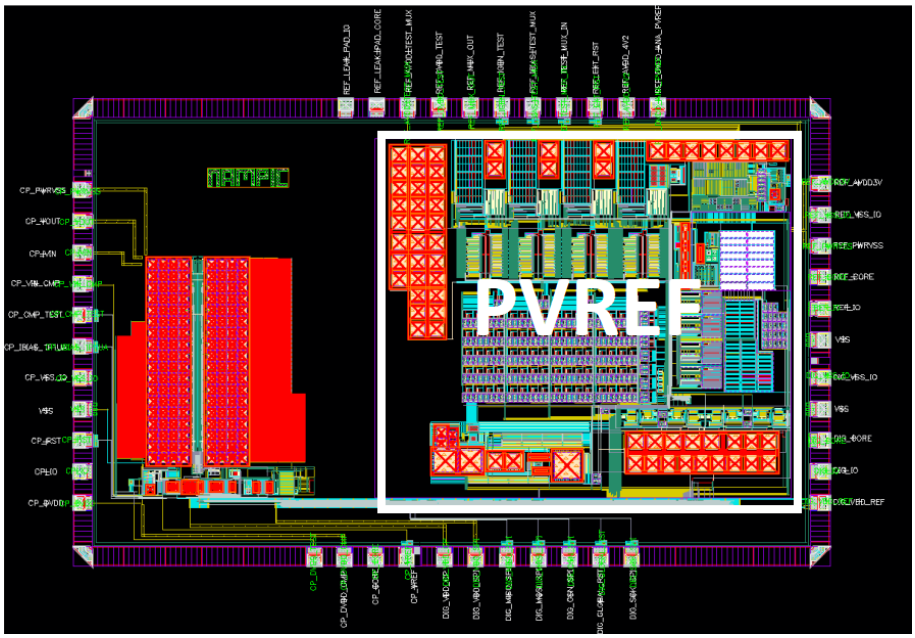

Figure 4.26: Layout of the NampIC integrated circuit. Highlighted in the white box is the programmable voltage reference PVREF.

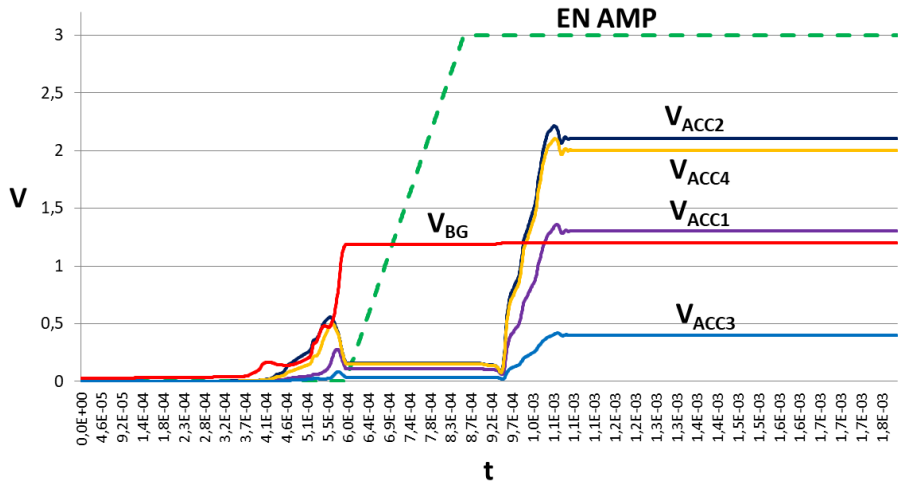

Figure 4.27: Transient post layout simulation. Generation of the accurate voltage references.

required. After the enabling of the system, the bandgap reference output V_{BG} rises up, then the PGA is activated by means of the signal $EN\ AMP$ and the four accurate references are generated for the calibration. In the example shown in Fig. 4.27 the references are V_{ACC1}= 1.3 V, V_{ACC2}= 2.1 V, V_{ACC3}= 0.4 V, and V_{ACC4}= 2 V.

Fig. 4.28 shows the transient response of PVREF in operative condition. In particular, the reference V_{REF1} on the output capacitor and of the internal calibrated voltage $V_{ref-calib1}$ are shown. V_{REF1} is shorted to $V_{ref-calib1}$ after the first calibration and during the Sleep phases. After the first calibration, recalibration routines are periodically repeated, with t_{recal} = 200 ms. The first two phases of the calibration routine, the series diodes ladder and the addition of diodes in parallel, are clearly recognizable in Fig. 4.27.

Fig. 4.29 zooms in the previous figure. Here, the temperature was instantaneously increased of 1 °C during the Sleep phase. The temperature variation affects immediately both V_{REF1} and $V_{ref-calib1}$. During the following Recalibration phase, $V_{ref-calib1}$ is restored to V_{ACC1} and in the end, entering the new Sleep phase, also the drop of V_{REF1} is compensated. The voltage drops prove the overall CTAT behavior of the

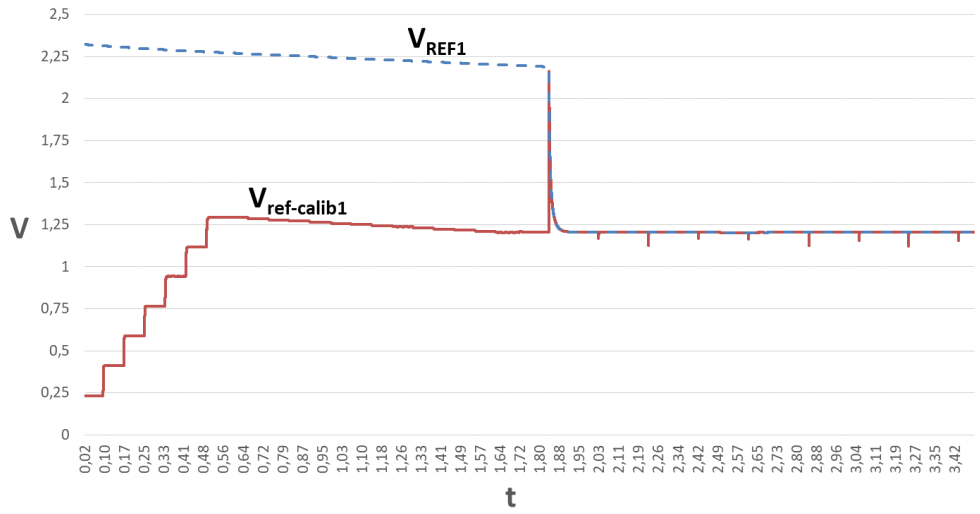

Figure 4.28: Transient post layout simulation of PVREF. The internal calibrated voltage $V_{ref-calib1}$ (red line) and the output reference on the capacitor V_{REF1} (dashed blue line).

voltage references.

To evaluate the performance of the system and compare it with the state-of-the-art voltage references, besides the overall current consumption I_{CC}, other metrics must be taken in consideration. In particular, the maximum acceptable ripple of the output reference V_{PP}, the number of calibrations per second C and the equivalent temperature drift $D = \frac{\delta T}{dt}$ that the system can tolerate.
Taking into account the target of ultra low-power applications, V_{PP} =500 μV is considered acceptable, whereas I_{CC} must be minimized. C and D are obtained from these definitions. We can conclude that a trade-off among these metrics clearly arises.

Fig 4.30 shows the current consumption of PVREF as ultra low-power reference (ULP) per number of recalibration per second. The same figure also depicts the sustainable temperature variation per second for V_{PP} = 500 μV. In these simulation results, that include also the digital control, one reference is considered. The current consumption $I_{CC} \approx 20$ nA can be achieved with $C < 1$ and the current consumption

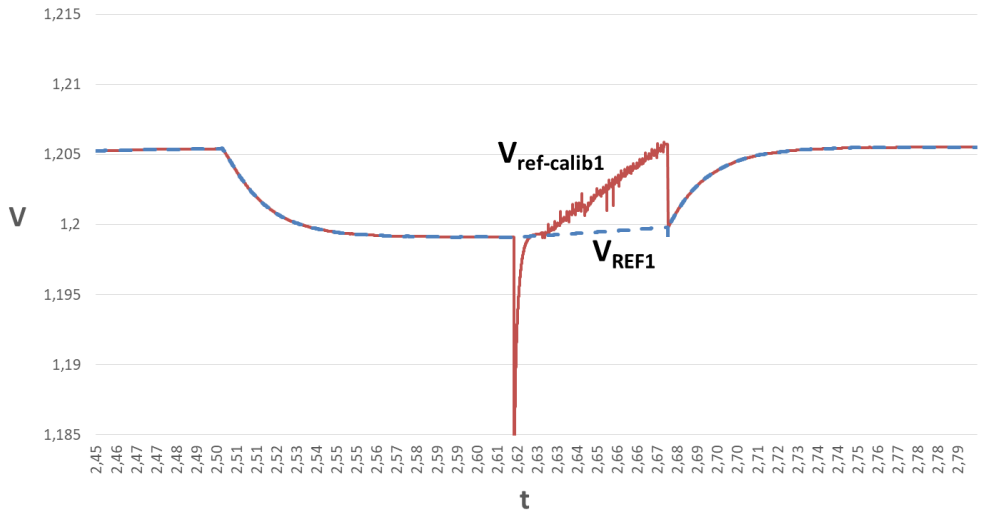

Figure 4.29: Transient post layout simulation of PVREF. The temperature variation causes the drop of $V_{ref-calib1}$ (red line) and V_{REF1} (dashed blue line); the recalibration procedure restores the correct value of V_{REF1}.

can be pushed down to $I_{CC} \approx 10$ nA with $C = 0{,}0625$. The calibration rate $C = 5$ can compensate temperature drifts up to $D = 0.5\ ^{\circ}C/s$, with current consumption of only 60 nA.

The exact correspondence between the two graphs in Fig. 4.30 means that increasing the power consumption allows the compensation of larger temperature variations.

It is worth to notice that the power consumption performance is limited by the leakage current during the Sleep phase of the system. It is expected an improvement of the performance in the chip testing, since it is well-known the large overestimation of the leakage current in the transistor models provided for the simulation.

Fig. 4.31 shows the ratio between I_{CC} of the ULP PVREF and the current consumption I_{BG} of the bandgap described in section 4.2.1.1. It can be noticed a drastic reduction of the power consumption even for $C = 20$. This performance allows the generalization of the proposed approach for other bandgap architectures with current consumptions higher than hundreds of nanoamperes.

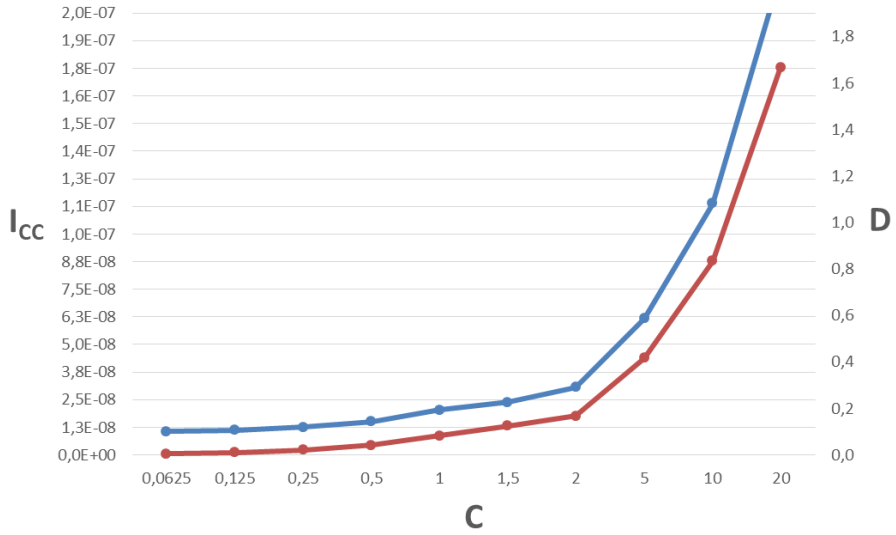

Figure 4.30: Current consumption of the ULP voltage reference I_{CC} (blue) and sustainable temperature variation per second D (red) vs. number of calibration per second C @ V_{PP} = 500 μV.

The performance of the PVREF circuit is compared with the state-of-the-art ultra low-power (ULP) bandgap circuits in Tab. 4.7. The power consumption of the circuitry for the other references have been subtracted to allow a fair comparison. The designed system achieves remarkable performance in terms of temperature coefficient over a large temperature range. Moreover, the current consumption, here given for C =1, is limited by the leakage during the Sleep phase and comparable with the state-of-the-art ultra low-power bandgap circuits.

Compared with others duty cycle based voltage references, the designed system achieves better performance in terms of voltage ripple and temperature range, but lower accuracy. This negative result derives from the bandgap reference signal V_{BG} and it could be further improved with more accurate bandgap architectures.

The circuit proposed in [68] achieves astonishing performance in term of power consumption, but with a sleep period of approximately ten minutes. The circuit in [69]

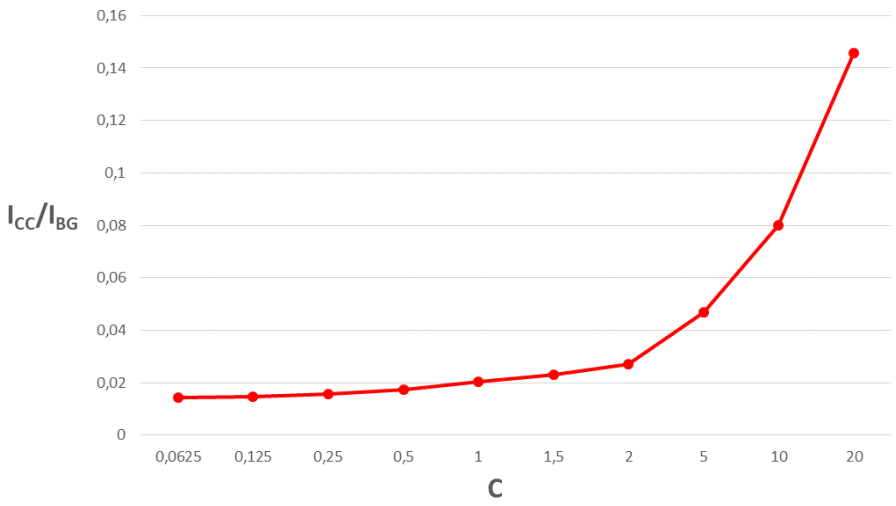

Figure 4.31: Ratio between I_{CC} and I_{BG} vs. number of calibration per second C - ULP voltage reference.

Table 4.7: Performance comparison with state-of-the-art ULP voltage reference

	[68] VLSI-2012	[69] JSSC-2012	[58] JSSC-2013	[70] ISSCC-2015	[71] ISSCC-2015	[72] VLSI-2018	[57] VLSI-2018	This work⋆ 2018
Tech.	180 nm	130 nm	180 nm	130 nm	350 nm	180 nm	180 nm	55 nm
Type	Duty Cycle	Duty Cycle	BG	Switched Cap.	Leak. Based	Leak. Based	Sub-BGR	Duty Cycle
Ripple	100 μV	20 mV	NA	50 μV	NA	NA	NA	500 μV
V_{REF}	1.198 V	255 mV	1.09 V	498 mV	1.175 V	1.232 V	412 mV	1.205 V
σ/μ	0.144%	0.65%	0.74%	3.86%	0.2%	0.54%	0.39%	1.67%
Ext. Calib.	Yes	Yes	No	No	NA	No	Yes	No
TC [ppm/°C]	24.7	40	147	75	12.75	143	33.7	40
T. Range [°C]	-20–100	-20–85	-40–120	0–80	-10–110	-20–100	-40–125	-40–120
I_{CC}	2 nA@R	200 nA@NA	65 nA@R	140 nA@R	24 nA@R	13.6 nA@R	95 nA@R	20 nA@R
Area [mm^2]	0.01	0.07	0.03	0.026	0.48	0.056	0.11	0.4

⋆Simulated results.

has larger power consumption, and requires ten calibrations per second.
Even though at the cost of a slightly higher current consumption compared with [72],

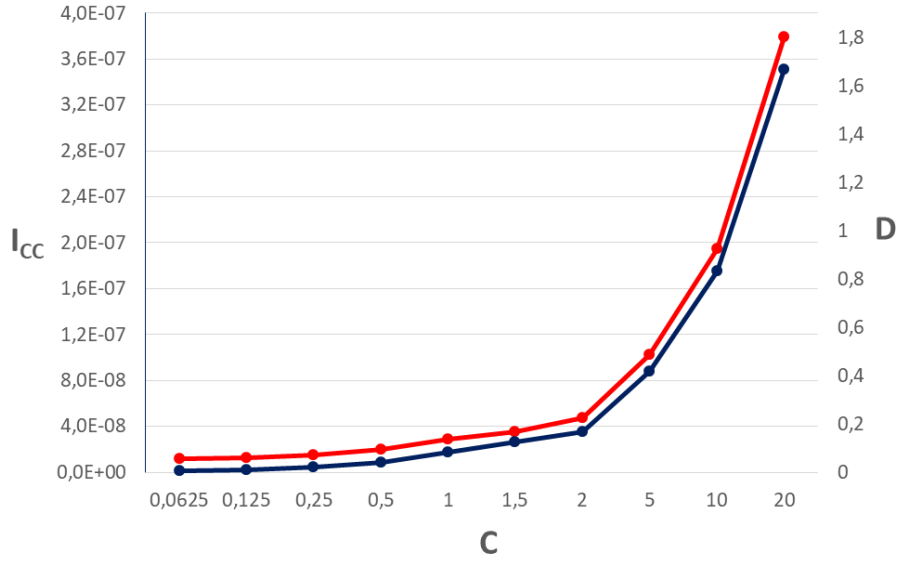

Figure 4.32: Current consumption I_{CC} of a programmable voltage reference (red) and sustainable temperature variation per second D (blue) vs. number of calibration per second C @ V_{PP} = 500 μV.

the system reported in this thesis achieves better temperature coefficient and lower accuracy.

Capacitorless solutions, like the sampling based architecture proposed in [73], despite the duty cycle based behavior, cannot achieve comparable current consumption performance, since they require high refresh rates.

It is worth to note that none of the alternative ULP voltage reference architectures of Tab. 4.7 has any programmability feature. To summarize the overall performance of the multi-reference PVREF circuit, Fig 4.32 shows the current consumption of one voltage reference of PVREF, including also the programmability feature, per number of recalibration per second. The same figure also depicts the sustainable temperature variation per second for a voltage ripple on the reference V_{PP} = 500 μV. Fig. 4.33 shows the current consumption of four programmable voltage reference of PVREF per number of recalibration per second. Fig. 4.34 shows the ratio between I_{CC} of the

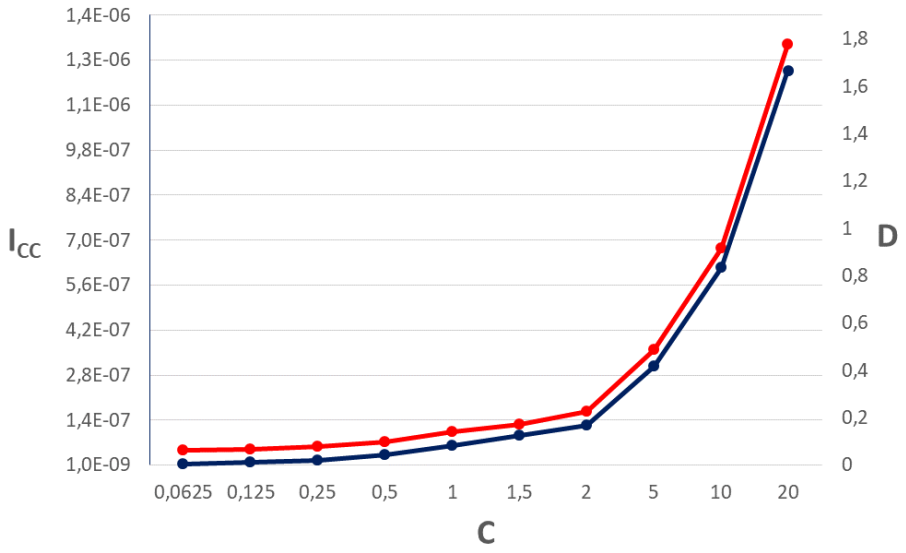

Figure 4.33: Current consumption for the four programmable voltage references (red) and sustainable temperature variation per second D (blue) vs. number of calibration per second C @ V_{PP} = 500 μV.

programmable PVREF and the current consumption I_{BG} of the bandgap described in section 4.2.1.1. The power consumption of the programmable PVREF approaches the bandgap one for $C = 20$.

The performance of the programmable PVREF circuit, considering one voltage reference, are compared with the state-of-the-art low-power programmable voltage references in Tab. 4.8.

The circuit proposed in [75], based on the variation of transistor sizes in a current generator circuit, achieves an I_{CC} in the order of tens of nanoamperes, but over a limited temperature range, suitable for biomedical applications. [77] and [79] attain good temperature coefficients over a large temperature range using switched capacitor feedback array architectures, but with current consumptions orders of magnitude higher than the circuit described in this thesis.

Compared with programmable voltage reference circuits in literature, the PVREF

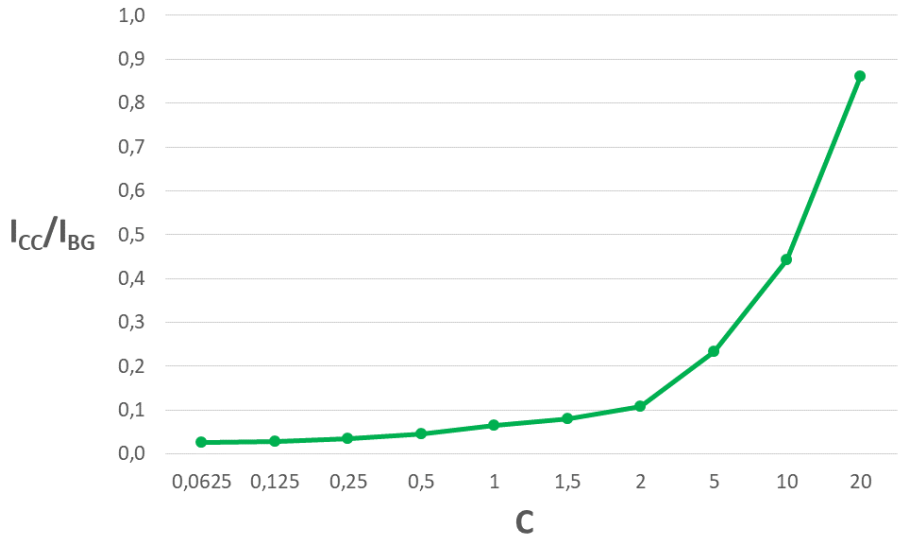

Figure 4.34: Ratio between I_{CC} and I_{BG} vs. number of calibration per second C - Programmable reference.

Table 4.8: Performance comparison with the state-of-the-art programmable voltage references

Year	[74] TCAS-2008	[75] EMBS-2011	[76] ICASIC-2007	[77]⋆ MWSCAS-2012	[78] TCAS-2015	[79] ESSCIRC-2017	This work⋆ 2018
Technology	350 nm	250 nm	350 nm	65 nm	40 nm	180 nm	55 nm
Type	Floating Gate	Size Control	Current DAC	SC FB	Res. FB	SC FB	DC Res. FB
V_{REF} range	50–600 mV	0.67–1.04 V	0.75–1.85 V	< 1.2 V	< 0.8 V	1.25–2.88 V	0.4–2.5 V
TC [ppm/°C]	100–185	627	35	23-43	45	28–38	40
σ/μ	NA	0.64%	NA	NA	5%	0.4%	1.67%
Ext. Calib.	No	NA	No	NA	No	No	No
T. Range [°C]	-60–140	20–50	0–100	-40–100	-40–85	5–85	-40–120
I_{CC}	10 μA	80 nA	840 μA	60 μA	40 μA	50 μA	29 nA
Area [mm^2]	0.002	0.011	0.11	0.04	0.01	0.09	0.5

⋆Simulated results.

system exibits excellent performance in terms of current consumption and temperature coefficient (TC), but with larger occupied area. Clearly, the trade-off between the power consumption and the silicon area arises again.

4.6 PVREF: summary

The design and implementation of an integrated ULP self-calibrated programmable voltage reference for sensor nodes and biomedical applications in CMOS 55 nm technology has been presented. The PVREF circuit for the generation of four voltage references, embedded in the NampIC chip, occupies a silicon area of 1.32x1.54 mm^2. The digital control occupies an area of 488x25 μm^2.
The system is based on the periodic recalibration of the low power voltage reference, composed by the nanoampere current source and the programmable impedance. Mixed signal post-layout simulations show that thanks to the fast recalibration routine an average current consumption $I_{CC} \approx 20$ nA can be obtained, with one calibration per second. With these values a temperature variation of 1 °C per twelve seconds can be compensated, with a refererence voltage ripple of 500 μV.
Summarizing, from the comparisons of Tabs. 4.7 and 4.8 some additional remarks on the PVREF circuit can be formulated.
The PVREF circuit can provide the best performance integrated into applications with slow or limited temperature variations, such as sensor nodes or biomedical applications, and has the ability to cope with a large temperature range.
The system demonstrates remarkable performance in both comparisons and it can be considered an excellent cross-over between the ultra low-power voltage references and the programmable voltage references. It seems therefore suitable for a large range of applications from biomedical systems, to wireless sensor networks and consumer electronics.

4.6.1 Physical implementation

At the time of this writing, the NampIC integrated circuit, embedding the PVREF circuit described in this thesis, has been manufactured in TSMC 55 nm CMOS tech-

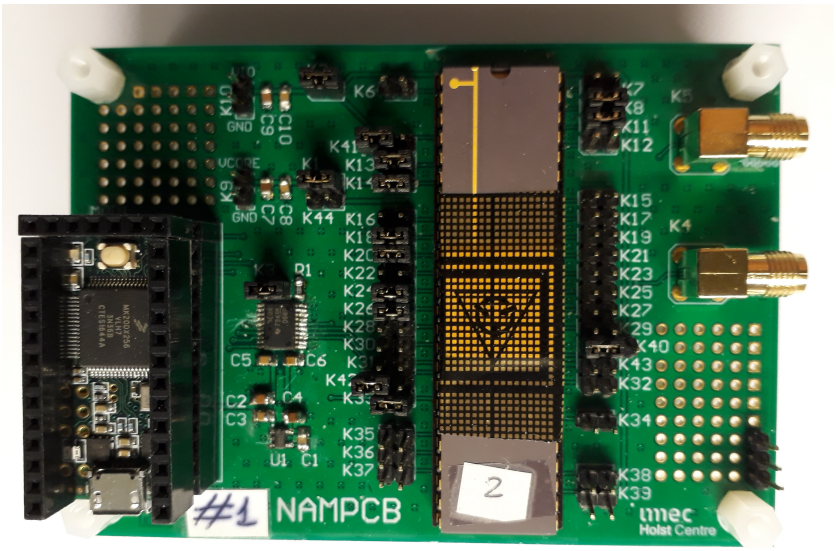

Figure 4.35: Test PCB for the NampIC integrated circuit.

nology. The printed circuit board for testing of PVREF has been designed and realized (Fig. 4.35). The testing setup is currently being prepared.

In the testing phase particular attention will be paid to the current consumption measurements. Taking into account that an average current consumption close to the leakage current is expected, the leakage current of the pads will be measured over the temperature separately, to subtract this contribution from the overall performance. Moreover, the decoupling capacitors for the power supplies on the PCB will be disconnected during the power consumption measurements to eliminate the contribution of their leakage current to I_{CC}.

Chapter 5

Conclusions

The demand for portable electronic equipments is rising in day-to-day life and it spans over an endless number of applications, from consumer electronics, to biomedical electronics systems, including implantable devices, up to sensor network. These systems, which are inherently mixed-signal systems, demand minimum power dissipation to extend the device life-time and reduce the size and weight of the battery. Therefore, lowering the power consumption of the analog circuitries without affecting the performance has become a major research topic. The reduction of power consumption permits the extension of portable devices life-time, but cannot guarantee their complete independency. Energy Harvesting techniques, which aim to collect energy from the surrounding environment, have emerged as valuable alternative for charging or power supplying low-power and ultra low-power circuits.
The work in this thesis has focused on the design and implementation of power management circuits for low-power and ultra low-power systems.

5.1 Contribution of this work

5.1.1 RF survey and RF harvester

A survey of the radio frequency electromagnetic field power availability in different environments has been carried out to assess whether this source can recharge or

directly supply an ultra low-power integrated sensor node.
Measurements show that it is possible to achieve an average value of available RF power of about -25 dBm over the GSM-900 band, in a typical urban environment. Power values adequate for energy harvesting have been recorded also in semi-urban environments on the same band, which seems to be the most suitable for RF harvesting.
A mathematical model of the interface between the RF rectifier and the DC-DC converter has also been provided. The analysis demonstrates that the energy can be efficiently transferred to the external accumulator even for extremely low values of available RF power at the antenna terminals, coupling an RF rectifier with a DC-DC converter with a strobed input control. Indeed, the equivalent load resistance of the AC-DC is only defined by the input power and the rectifier efficiency, hence the approach can be generalized to any AC-DC topology. Therefore, taking into account the ultra low-power condition of generic RF environments, the design of an ultra low-power harvester operating over the GSM-900 band, with a strobed DC-DC converter, has been proposed. The control strategy of the converter allows to continuously adapt the harvester behavior to the available RF power with a limited power consumption.
An RF harvester circuit, embedded in the HarvIC integrated circuit, has been designed and implemented in ST 65 nm CMOS technology for power management of an integrated temperature sensor with analog-to-digital converter. HarvIC integrates a novel Maximum Power Point searching and Tracking system to adapt the system to mutable environments and exploit the most promising RF source.
The results of the post-layout simulation, in terms of sensitivity and end-to-end power conversion efficiency, show that the proposed RF harvester architecture can be effectively used in real life environments, including two of the environments surveyed in this thesis. The MPPT system allows the RF harvester adaptation to mutable environments, expanding its application space with a negligible impact on the overall power consumption.

5.1.2 Programmable voltage reference: PVREF

ULP applications, such as sensor nodes or implantable devices require ULP Bandgap circuits with good performance in terms of temperature coefficient, reference accu-

racy, and power consumption of few nanowatts. In this thesis, the design of a novel ULP bandgap circuit, PVREF, has been reported. PVREF has been fully designed and implemented in TSMC 55 nm CMOS technology, with thick-oxide option. The circuit has been developed to be integrated in the power management sections of energy harvesters, sensor nodes, and biomedical applications.

The increasing of the complexity in analog and mixed-signal systems, where different voltage supply domains coexist, also requires the capability to simultaneously provide multiple voltage references. The ULP bandgap circuits reported in literature cannot provide reference programmability without a large increase of their power consumption.

PVREF provides four voltage references and improves with respect to the state-of-the-art ULP bandgap circuits, since it realizes the calibration and the periodic recalibration of the voltage references with an output reference range from 0.4 to 2.5 V, bias currents in the order of few nanoamperes, and limited required silicon area.

In post-layout simulations with back-annotated parasitic extraction, the circuit shows remarkable performance in terms of temperature coefficient and power consumption, compared with the state-of-the-art ultra low-power bandgap circuits and low-power programmable voltage references. The PVREF system can be considerated a cross-over between the ultra low-power voltage references and the programmable voltage references, with competitive performance compared with the state-of-the-art of both classes of circuits.

SoC	Main block	Sub-Block	Literature/Revised	Fully new	Ref.
HarvIC	AC-DC		**X**		[28]
	DC-DC			**X**	
		Uvlo battery	**X**		[32]
		Constant-Gm	**X**		
		Hysteresis Comp.	**X**		[33]
		Ring Oscillator	**X**		
	MPPT	V_H monitor		**X**	
		FSM		**X**	
PVREF	Z_{CALIB}			**X**	
	I_{GEN}		**X**		[66]
		Transcoder		**X**	
		RAM	**X**		
		Bandgap	**X**		
		PGA	**X**		[65]
		Comparator	**X**		
		LF-Oscillator	**X**		
		HF-Oscillator	**X**		
		FSM		**X**	

5.1.3 Circuit domain contribution

Table 5.1.3 lists the main circuits developed in the thesis and summarizes the contribution of this work to the circuital domain. Where possible, references to literature have been added in the table.
Other circuits have been adapted for the specific application, without claim of originality. For sake of brevity, this dissertation does not provide the complete transistor analysis of some of the circuits composing the PVREF SOC.

5.1.4 Open issues and further developments

Despite the contribution proposed by this work of thesis, still some issues remain open. As mentioned in the previous chapters both circuits (HarvIC and PVREF) have not been tested yet. Hence, the simulation results must be confirmed by measurements on actual silicon. Indeed the future developments of both systems on chip will be strongly affected by their silicon performance.

For the HarvIC circuit, future developments should lead to a further lowering of the power consumption, for istance by substituting the PVREF voltage reference to the bandgap used for the RFID communication. The PVREF system instead can be further developed to be integrated into duty cycled sensors. During the sleep phase of these circuits, when the power supply and references are still required, PVREF could be used to minimize the power consumption. Moreover, during the same phase, the memory retention voltages can be varied to lower the leakage, exploiting the PVREF programmability.

Appendix A

HarvIC Testing

The HarvIC circuit has been implemented in ST 65 nm CMOS technology and it can be divided in three subsections: the RF harvester, the temperature sensor with A-to-D converter, and the section for the RFID communication.
The DC-DC converter and the MPPT system, composing the RF harvester, have been designed to operate alternatively, allowing the periodic scan of the RF band. This feature permits the cyclic tuning of the system on the most promising carrier frequency.
A finite state machine, implemented on FPGA for testability reasons, regulates the alternative enabling of the two subsections. In next releases this digital supervisor can be directly integrated on chip. Moreover, the FPGA programs the digital serial programmable interface of Fig. A.1 used for the testing of the blocks composing HarvIC.
By means of the signal CLK, the setting bits are transmitted through the serial chain of flip-flops. The LOAD command is used to send simultaneously the bits to the second row of flip-flops. At the next rising edge of CLK, the configuration is transmitted to the pass-gates in the chip. The digital outputs of HarvIC are transmitted to the FPGA via digital pads, that also provide the buffering.
For the testability of analog signals four analog interfaces are used, as shown in Fig. A.2. The configuration of the IO analog interface is provided by the FPGA, by means

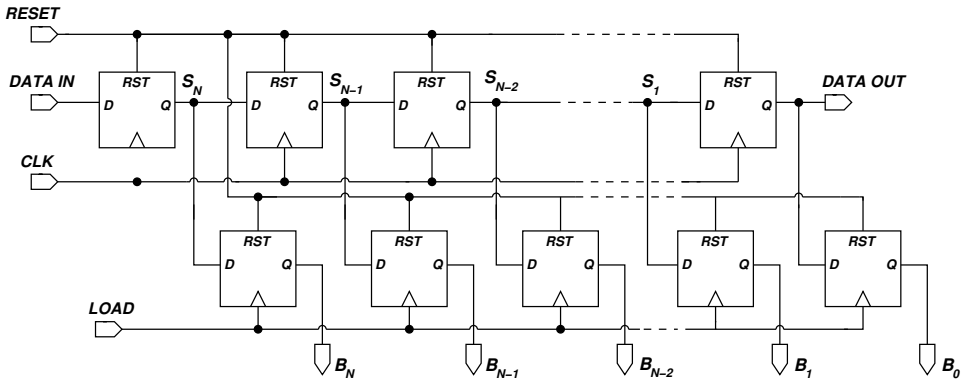

Figure A.1: Schematic of the serial programmable interface.

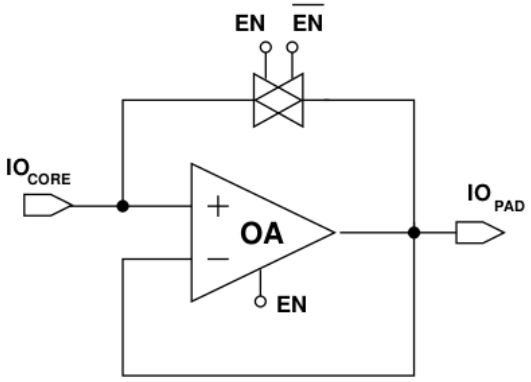

Figure A.2: Architecture of the input-output interface.

of the serial programmable interface.

Analog voltage references can be externally provided through these interfaces, when configured as inputs.

During the test of analog outputs, the analog buffers provide signal buffering to avoid undesired effects due to the parasitic capacitance of the probes.

The four buffers are implemented as operational amplifiers in unity gain feedback, with folded cascode architecture, Fig. A.3.

Complementary nMOS and pMOS differential pairs are used for large input common

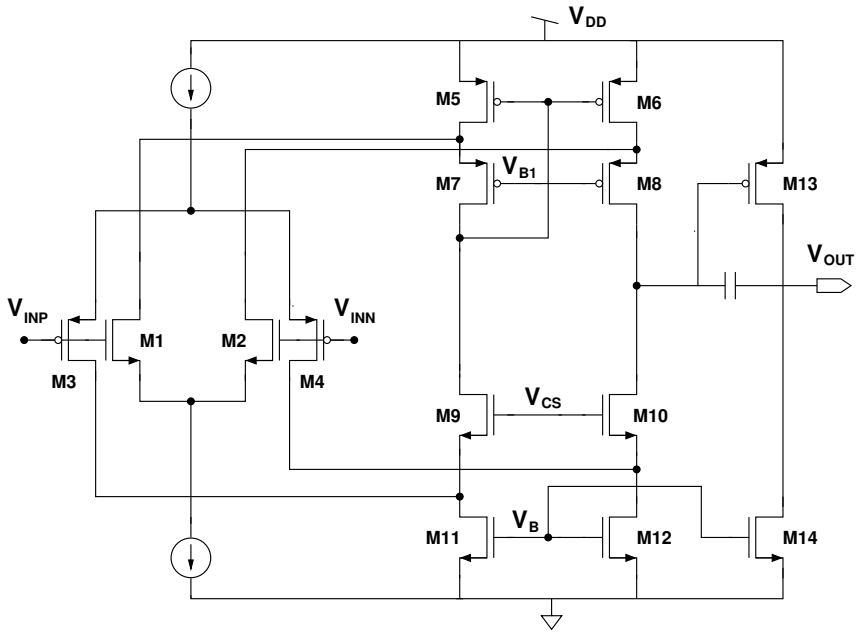

Figure A.3: Schematic view of the buffer circuit.

mode range. Standard Miller compensation guarantees the buffer stability.

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