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Exploitation of an Industrial Low-Bandwidth Communication Line for Modulation-Level Synchronization of Voltage Source Converters

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Abstract: Parallelization of power electronic converter units is a way to meet the high current requirements of modern electrification applications. In case of voltage source converters, parallel operation can be attained only if the voltages of all the units are equal. In the current state of the art, this voltage synchronization can be achieved at the fundamental frequency, but not at modulation frequency, hence requiring bulky filters to limit circulating currents; this lowers the system performance in terms of cost, volume, weight and sustainability. In this paper, the authors propose a novel approach to synchronization, acting directly at the modulation frequency level, thus removing the need for any filter. This technique relies on the natural parasitic inductance and resistance of the wiring among parallel units. Specifically, this paper presents the first of two synchronization stages required to reach the sub-nanosecond synchronization necessary to completely remove the filters. At start-up, a low-bandwidth industrial communication line, based on the CAN protocol, is exploited to guarantee that the error in the synchronization of PWM signals among all the parallel units is lower than 0.1%. This limits the initial circulating current, supporting the subsequent control stage that achieves sub-nanosecond synchronization. The proposed concept is validated by experiments using a commercial MCU unit with an unadorned CAN peripheral.

Keywords: circulating current; initial synchronization; parallel operation of power converters; switched mode DC/AC power converter

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1. Introduction

Parallelization of voltage source converters is becoming a widely used practice [1–5]. With the constantly increasing power systems size [6], parallelization becomes a landmark for feeding power systems because like the multi-levels structures, it enables the use of smaller power devices with smaller power losses, reduces the total harmonic distortion [2], and achieves higher overall efficiency because the switching frequency can be increased [7]. Other advantages are the reliability of arbitrary redundancy [1,4,8–10] and the standardization of power devices, because the power systems specifications are met by the number of parallel units and not by the devices themselves.

In the literature, a lot of papers propose studies about parallelization of power converters. Parallel operation is used in the renewable energy conversion field, in particular [1] proposes a way to connect wind turbines to the grid by using AC-DC-AC topology with parallel operation of both rectifiers and inverters. In [11], the authors present a parallel DC-AC switched mode power converter that connects a small power generator (<1 MW) to the grid, using two smaller units connected in parallel through master–slave logic. In the automotive field, ref. [3] proposes an electric vehicle fast charger based on two parallel three-level DC-DC converters, where the parallelization is achieved through an integrated inductor at each converter output in order to minimize the circulating current and reduce the output current ripple.

In case of voltage source converters (VSCs), there are different ways to deploy parallel operation in order to avoid circulating current among units, which causes undesired voltage drops, power losses and stress on the common DC link (in case of parallel input topology). This reduction can be achieved using particular modulations: the authors in [8,12] use SVPWM (Space Vector PWM). Other researchers in [7] propose a cascade null vector control system together with a three-phase Harmonic Elimination PWM (HEPWM) modulator in order to reduce the zero sequence circulating current.

Other techniques [13–19] perform synchronization at a fundamental frequency by using two different approaches: galvanic isolation using multiple winding line frequency transformers or including an impedance at the output of each VSC. This can be achieved either by using a single phase harmonic filter inductor or using magnetic coupled inductors between corresponding phases of each parallel VSC.

Authors in [14] propose criteria to evaluate frequency line inductors at VSCs output in three study cases: single unit connected to the bus, two units with different DC link and two units that share the same DC link. The latter case results in significant circulating currents between units, that can be mitigated by inserting a high impedance path with common mode coils placed between corresponding phases of different VSCs. In [19], a total flux minimization control method based on Discontinuous PWM (DPWM) is presented in order to reduce the coupled inductors size.

All of the works reviewed above use some filters, usually inductors, to keep any recirculating currents under control. In [20], the authors propose a novel parallelizing method acting directly at the modulation frequency level, relying only on the natural parasitic inductance and resistance of the wiring among parallel units. This would allow the complete removal of any filter, so that a complete parallel converter would be truly modular, composed only of the sum of the parallelized converters.

The proposed synchronization method is based on a sequence of two stages: an initial coarse synchronization supported by a slow communication interface like CAN bus, followed by a high speed closed-loop control on each converter that compensates for slightly different clock frequencies and residual delay errors left by the initial synchronization.

The main contribution of this paper is the design and test of a practical technique for the initial (coarse) synchronization of parallel converters referred to in [20], using identical microcontroller units (MCUs) connected through a CAN bus interface to a master unit managing the entire system. Although the authors estimated that the initial (coarse) synchronization is required to yield a <1% synchronization error in order for the secondary (fine) synchronization to do its job, experiments show that the proposed solution guarantees a <0.1% error on the starting times of the modulating signals of three parallel units.

2. Materials and Methods

Unless additional impedance elements are used to connect the outputs of power converters in parallel, limiting the recirculating currents has to be achieved using only the natural resistance and inductance of the connections among the units. In particular, given the intrinsically transient operation of high frequency switch mode converters, the arising of recirculating currents is delayed only by the stray inductance, that for typical cable lengths of tens of centimeters can be estimated as a few hundred nanohenries [21]. Such a small inductance requires the PWM outputs of parallel converters to be synchronized at the picosecond level, which justifies the proposed two-stage approach. This is true even considering the damping effect of the stray resistance, mostly related to the on-state resistance of the power switches rather than to the one of copper traces and wires [22].

The initial synchronization has to minimize the delay error between parallel units in order to reduce the circulating currents after startup. Experimental validation has been done on identical MCU evaluation boards connected through CAN bus interface to a higher level control unit (master) managing the system. The hardware used for the units and the master is the ST NUCLEO-F446RE evaluation board with the STM32F446RE MCU. This hardware provides CAN peripherals and advanced controls timers embedded in the

MCU for PWM generation with complementary outputs and dead time insertion, suitable for inverter control. The MCU is an ARM® Cortex® M4 with embedded FLASH, SRAM and 32 bit FPU that, combined with 12-bit ADCs, can also support the secondary fine synchronization control stage; this is not discussed in this paper.

Figure 1 is a diagram of the test bench used for this work. As can be seen, CAN tranceivers are not used to adapt the voltage levels to those required by the CAN protocol because the tests are done with short connections to avoid any disturbance problems. The diodes are used for monitoring purposes during tests, since they allow us to discriminate which unit is transmitting a dominant bit on the bus. The physical experimental setup is shown in Figure 2.

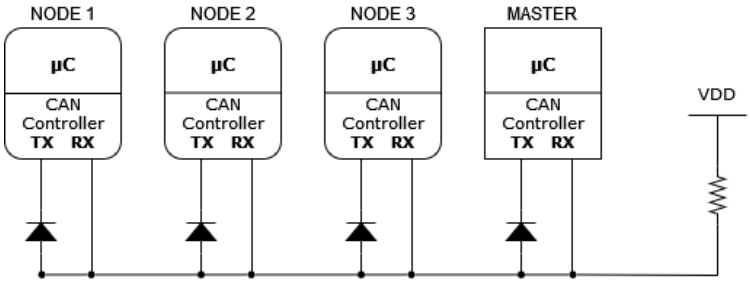

Figure 1. Principle diagram of the test bench. The master triggers three slave nodes, which synchronize themselves following the technique proposed in this paper. The CAN line is configured for wired and operation.

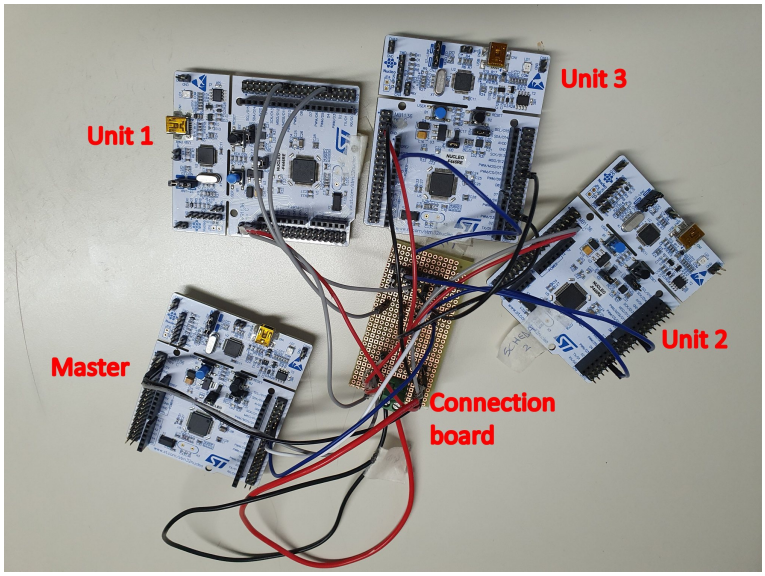

Figure 2. Photo of the test setup.

2.1. CAN Peripheral Synchronization Method

The CAN bus protocol is widely used in automotive and industrial embedded applications because of its robustness towards electromagnetic interference (EMI), which makes it suitable for communications between voltage source converters. To understand how the strategy works, it is necessary to introduce the bit timing properties of CAN bus. As will be clear in the following, the bit rate of the CAN network affects the precision achievable through the proposed technique (the faster the better). A bit rate is usually chosen based on the interference level and maximum distance between nodes in the final application; in this work a comparatively slow speed communication (100 kbit/s) was chosen in order to assess the level of synchronization obtainable in slow communications scenarios. The peripherals connected to CAN bus use a particular synchronization method based on division of total

bit time into fixed-length time units called time quanta. There are different segments in a bit time:

- Synchronization segment: where an edge is expected to be.
- Propagation segment: used to compensate line and drivers delay.
- Phase segments 1 and 2: dynamic length segments used to perform synchronization.

Two processes are involved in synchronization: hard synchronization, which is done at the beginning of each message to align segment slots between all nodes and soft synchronization, and soft synchronization, which is done by each node, lengthening phase segment 1 or shortening phase segment 2 by an integer number of time quanta, in order to compensate lagging or leading edges.

2.2. Oscillators Tolerance

The boards used in tests mount an external 8 MHz crystal oscillator. Due to temperature, voltage, capacitor tolerance and long term state of wear, frequency drift between units is unavoidable. As a consequence, CAN controllers on different units show frequency drift as well, which brings different peripherals to sample the same bit at different times. One of the goals of this work is to prove that synchronizing units on a common bus event leads to a residual PWM starting delay that depends on system frequency drift and not on the CAN bus resynchronization process.

Oscillator tolerance is obtained by an indirect measurement of alignment time of PWM signals, nominally identical, generated by the nodes. Due to different periods (clock frequency drift), a progressive time shift is found between corresponding rising/falling edges, so, by measuring the interval between two consecutive alignments of the rising edge (T_{SY}), the frequency drift can be derived as follows. Considering two PWM signals generated by different oscillators with periods T_1 and T_2, respectively, during an interval T_{SY}, a number of N_1 periods are counted for the first PWM generator and N_2 are counted for the second, with $T_{SY} = N_1 T_1 = N_2 T_2$. Considering $T_1 > T_2$ leads to:

$$N_1 = N, N_2 = N_1 + 1 = N + 1 \tag{1}$$

$$T_1 = \frac{T_{SY}}{N}, T_2 = \frac{T_{SY}}{N+1} \tag{2}$$

Normalizing periods difference to nominal switching period T_{sw} and using Equations (1) and (2):

$$\Delta T_{norm} = \frac{T_1 - T_2}{T_{sw}} = \frac{1}{N(N+1)} \frac{T_{SY}}{T_{sw}} \tag{3}$$

Considering that T_{sw} is approximately equal to the average of the periods of the two units ($T_{sw} \approx \frac{T_1 + T_2}{2}$) and using (2):

$$\Delta T_{norm} \approx \frac{1}{N(N+1)} \frac{T_{SY}}{\frac{T_1 + T_2}{2}} = \frac{2}{2N+1} \tag{4}$$

Since $T_{SY} \gg T_{sw}$:

$$N \approx \frac{T_{SY}}{T_{sw}} \tag{5}$$

A PWM frequency of 10 kHz nominal was generated for the experimental measurement of realignment times. As an example, the realignment of converter 2 and converter 1 took an average of 20.61 s over 303 measurements (Table 1). This value of T_{SY} translates into a number of cycles N before realignment of about 206,100.

Table 1. Alignment test results.

Units under Test	N (Number of Tests)	Average [s]	Std. Dev. [ms]	Minimum [s]	Maximum [s]
2 ⟶ 1	303	20.61	395.3	19.28	21.15
3 ⟶ 1	338	7.79	161.5	7.49	8.24
3 ⟶ 2	314	5.59	79.91	5.39	5.78

2.3. CAN Peripheral Interrupt Synchronization

Two different converter synchronization techniques have been tried in this work. The first one relies on the response of the CAN communication peripheral to a specific converter start-up message issued by the master controller. Robustness and versatility of the CAN protocol coexist with a big limitation in applications with very strong real time constraints, like in parallelization of VSCs without filters, where precise initial synchronization is needed to ensure the system integrity. CAN ensures a synchronization process at level 1 of the ISO/OSI stack that is used to compensate for the natural drift of local oscillators. This resynchronization process can lengthen or shorten the bit time at fixed steps determined by peripheral clock frequency, that in most cases is much lower than the system clock frequency. The CAN controller used in these tests, for example, can work at 45 MHz maximum frequency so that, with the limitation of phase segments length, bit time can be shortened or lengthened by 22 ns. In many cases due to noisy environment, the peripheral cannot work at this maximum speed so, the sampling process of bits in the CAN packet, improves uncertainty at lower speed like as demonstrated in this test.

The on board CAN peripheral (bxCAN) offers an hardware HLP (Higher Layer Protocol) at the data link level of the ISO/OSI stack managing:

- Transmission and reception of incoming messages;
- Construction of bit time (Time Quanta, Sync and Phase segments);
- Interrupt management registers;
- Diagnostic information.

The reception can be done using an input filter to store particular message IDs (in this case the converter start-up message) in particular FIFO stacks of the CAN peripheral. The presence of a message in a FIFO can cause a message pending (MP) interrupt, signaling the MCU that an incoming message should be read and causing a jump to the appropriate interrupt service routine (ISR). The ISR, in turn, starts the PWM, configured to generate a 100 µs period.

The master unit periodically sends a starting message so that repeated tests of residual delay on first rising PWM edges can be done.

Due to the bit stuffing property of the CAN protocol, a valid message cannot have more than five consecutive bits with the same logical value except for the end of frame (EOF) field, which is composed by seven recessive bits. This makes it easy to recognize the acknowledge (ACK) that can be used as a common synchronization point for the PWM generation. The time period between the last rising edge of the CAN packet (ACK) (Figure 3) and the first rising edge of the PWM can be divided into four different subperiods:

1. Validation;
2. Peripheral FIFO register signaling;
3. Interrupt management (ends with first instruction of ISR);
4. PWM starting sequence.

It is clear that the first subperiod is bit-rate-dependent, because the message is valid for the receivers, if there is no error until the last but one bit of the EOF [23]. The last two subperiods are inserted by the MCU that is peripheral-frequency-independent, so it is logical to consider the sum of these periods fixed and deterministic because all units are subjected to the same calculation load.

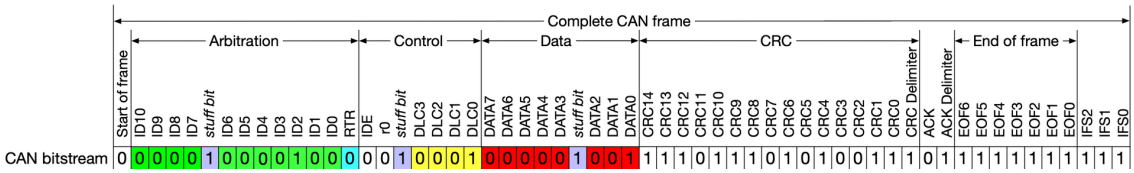

Figure 3. Example of CAN bus frame. Green bits make up the message ID field, yellow bits are DLC (data length code), red are data bits, violet are stuff bits. Image courtesy of Ken Tindell, Canis Automotive Labs Ltd, through *Wikipedia*.

2.4. GPIO Interrupt Synchronization

Leaving the synchronization to the CAN peripheral interrupt brings uncertainties especially when the time quantum (TQ) is large, as shown in the results section. Therefore, a second strategy was tested, in which the synchronization is performed using the general-purpose input–output (GPIO) peripheral of the MCU. With this strategy, one line of the CAN bus is also routed to a GPIO pin set up as an input, while the CAN peripheral is used to recognize the start-up message. The GPIO pin raises an interrupt whenever a rising edge is detected in a CAN packet. This happens regardless of the message that has been sent, so a particular algorithm (Figure 4) is used to discriminate the start-up event.

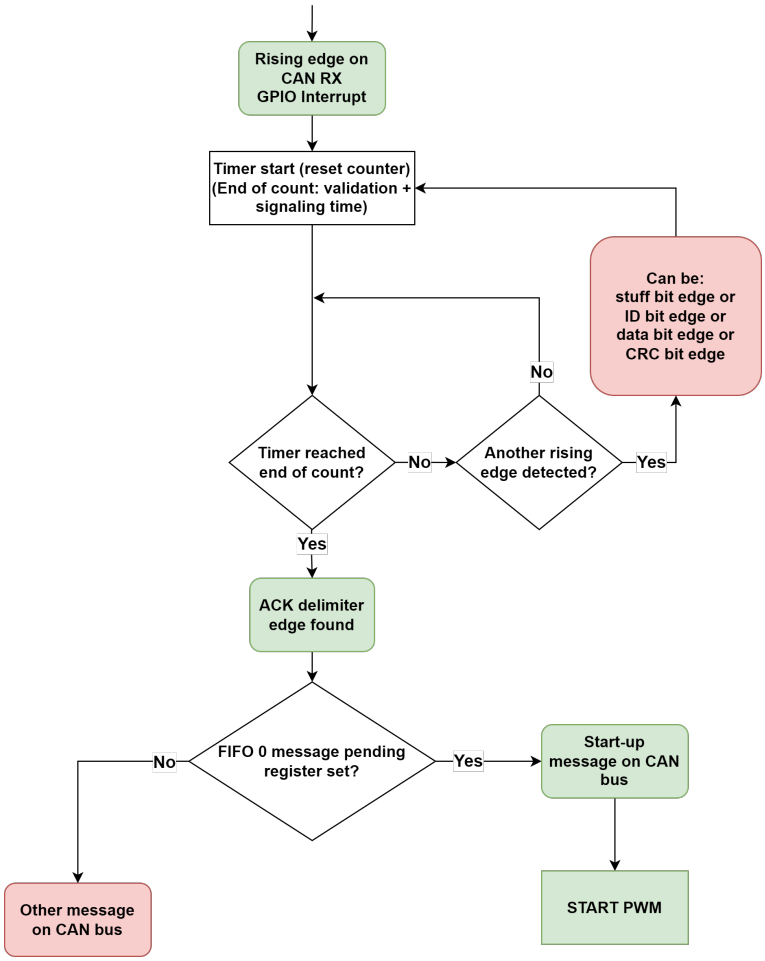

Figure 4. Start message detection algorithm.

Each time a new GPIO interrupt event occurs, a timer starts counting up from zero. The timer is set to raise an interrupt event after an interval that is the sum of the validation and peripheral signaling subperiods previously defined. This delay ensures the CAN peripheral has enough time to store an incoming message in the FIFO and set the corresponding

register. Crucially, the delay is also longer than the longest possible stream of bits of the same value, so the timeout will only occur after the last edge of a CAN packet, that is the ACK delimiter edge. At this time, the algorithm knows that a CAN message has been fully transmitted and correctly received, but it still needs to check if the message was indeed a start-up message from the master node. The timer ISR, therefore, instructs the MCU to poll the CAN peripheral FIFO: if a start-up message is found, the PWM is finally started. This solution ensures that all the units are synchronized on a common event (ACK) caused by the slowest node. The timer count is clock drift dependent, but not CAN peripheral synchronization dependent.

3. Results

3.1. Frequency Drift

Measurements of the realignment time (T_{SY}) between each pair of nodes are reported in Table 1, where 2 $\longrightarrow$ 1 indicates the realignment time between the PWM signals of converter 2 and converter 1, and similarly for the other pairs of units. Data was captured using the statistical functions of a digital storage oscilloscope (Figure 5).

Combining the results of Tables 1 and 2 confirms the intuitive idea that increasing realignment time results in a smaller oscillator mismatch, i.e., frequencies are better matched. The values in Table 2 confirm that, even if all the microcontrollers are clocked by quartz oscillators of the same nominal value, the actual clock frequencies are randomly dispersed. This frequency mismatch, although small, if left uncontrolled, can quickly lead to arbitrarily large phase differences, which justifies the need for a closed loop control (not described in this paper) to strictly maintain the required phase match after the initial alignment.

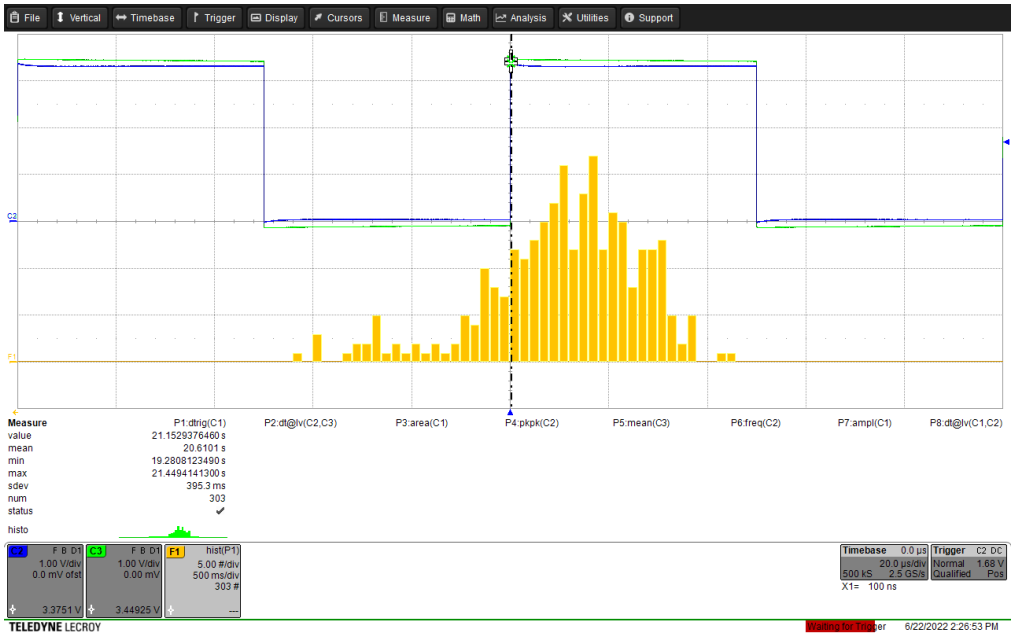

Figure 5. Experimental determination of realignment time statistics between the PWM signals of converter 2 and converter 1.

Considering Equations (4) and (5), it is possible to estimate the relative oscillator tolerance between units. These tolerances are reported in Table 2.

Table 2. Oscillator mismatch between each pair of units.

Units under Test	Oscillator Mismatch [ppm]
2 $\longrightarrow$ 1	4.85
3 $\longrightarrow$ 1	12.83
3 $\longrightarrow$ 2	17.89

3.2. CAN Peripheral Interrupt Synchronization

Tests on residual PWM delays inserted by preliminary synchronization using CAN peripheral interrupt are shown in Figure 6. Tests were performed between pairs of units, whereas one unit was sending the start-up message and both were trying to synchronize their PWM generators based upon the arrival of the message in the CAN buffer. It can be seen that the standard deviations of the three relative delays change monotonically with an increase of TQ.

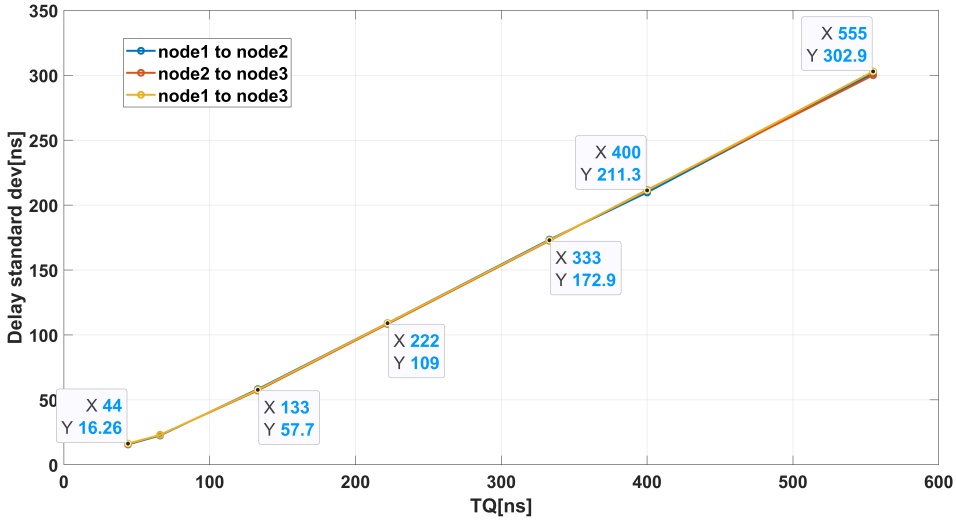

Figure 6. CAN peripheral synchronization: standard deviations of delays as a function of time quantum.

The monotonical increasing trend confirms that, with larger TQ, the CAN peripheral can make larger bit-time jumps to synchronize units, resulting in a less precise overall synchronization.

Different bit rates can be obtained using the same TQ by modifying the phase segments length during CAN initialization. The results in Table 3 show that increasing the bit rate with the same TQ does not result in a better synchronization, so it is clear that synchronization precision depends more on TQ than on the CAN bit rate.

Table 3. Standard deviations of three delays with different bit rates.

Delay Sigma	$200\frac{kbit}{s}@TQ = 200$ ns	$1\frac{Mbit}{s}@TQ = 200$ ns
$2 \longrightarrow 1[\sigma_{21}]$	96.23 ns	110.1 ns
$3 \longrightarrow 1[\sigma_{31}]$	115.6 ns	135.2 ns
$3 \longrightarrow 2[\sigma_{32}]$	95.40 ns	112.1 ns

3.3. GPIO Interrupt Synchronization

This test was performed on pairs of units, similarly to the CAN peripheral synchronization test. In this case, the CAN signal was routed in parallel to a GPIO input and the algorithm of Figure 4 was used to synchronize the start of the PWM generation. The results are reported in Figure 7.

The results show that this synchronization method is TQ independent because the parallel units have a common synchronization point (the last rising edge of the message) and then the uncertainty is given only by the timer peripheral, which is strongly related with oscillator tolerance. The independence from TQ yields a synchronization precision over an order of magnitude better for this second method compared with the first one with large TQ.

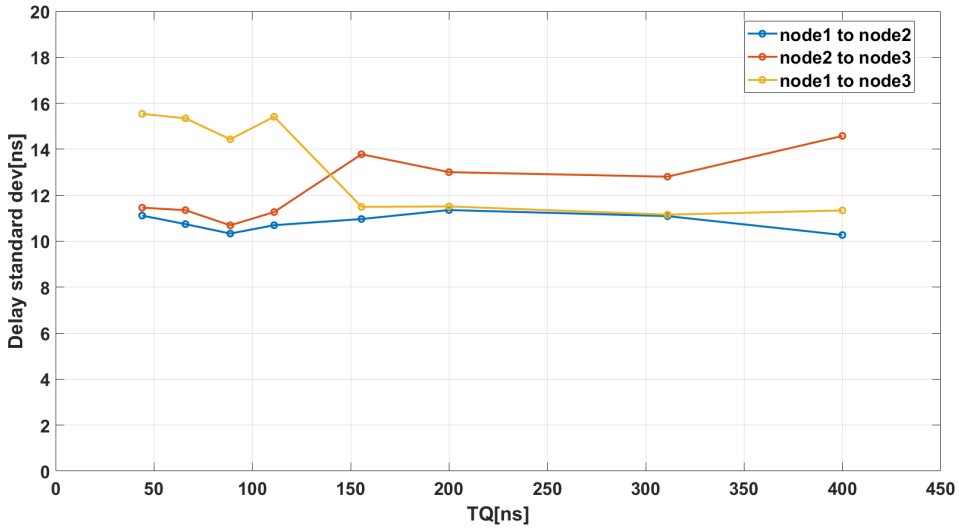

Figure 7. GPIO peripheral synchronization: standard deviations of delays as a function of the time quantum.

4. Conclusions

The goal of a less than 1% synchronization error between parallel converters PWM signals can be achieved using both methods presented in this paper. The difference is that the CAN peripheral interrupt method is strongly related to the CAN peripheral behavior; using, for example, a 550 ns TQ results in a synchronization uncertainty that is more than the required 1%. It is clear that the results in Figure 6 represent the standard deviation of the delay, but some bad cases have been recorded during tests, where the delay was higher than 1 µs so that, with a 100 µs PWM period, the specification was not met.

The GPIO interrupt method is intrinsically CAN peripheral independent and tests have shown a less than 0.1% synchronization error, one order of magnitude better than the requirements, even in the worst case.

This work paves the way for the second phase (fine synchronization) that is required to parallelize converters without any reactive filters.

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