An Ultra Low-Power Programmable Voltage Reference for Power-Constrained Electronic Systems

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Michele Caselli, *Member, IEEE*, Evgenii Tiurin, Stefano Stanzione, *Member, IEEE*, Andrea Boni, *Member, IEEE*

***Abstract*—This paper proposes a novel architecture for the generation of a programmable voltage reference: the background-calibrated (BC)-PVR. Our mixed-signal architecture periodically calibrates a static ultra low-power voltage reference generator, from an accurate bandgap reference. The portion of the chip used for the calibration can be powered down with a programmable duty-cycle. The system aims to fully exploit the small temperature derivative vs time D_T of several application domains to minimize the average current consumption. The BC-PVR has been designed and implemented in TSMC 55-nm CMOS technology, and it achieves the largest reported programming reference output range [0.42 - 2.52] V, over the temperature range [-20 , 85] $^{\circ}$C. The duty-cycle mode allows nanoampere current consumption, and the large design flexibility permits to optimize the system performance for the specific application. These features make the BC-PVR very well-suited for power-constrained electronic systems.**

***Index Terms*—Programmable Voltage Reference, Low-Power Systems, Duty-cycle, Self-Calibration, Mixed-Signal SoC**

I. Introduction

Portable electronic devices, low-power micro-controller units, Internet-of-things (IoT) sensor systems, and implantable devices for biomedical applications require dedicated power saving schemes to extend their battery lifetime. For these systems, ultra low-power voltage regulators can ensure voltage supply generation with quiescent current at nanoampere levels [1]–[3]. However, these supply schemes require accurate voltage references, and the power consumed for their generation has become a major fraction of the total power budget [4]. Therefore, Systems-on-Chip (SoC) for power-constrained applications must be also equipped with ultra low-power voltage references. Smart SoCs require multiple references at different voltage levels, and the possibility to dynamically program the reference allows significant energy saving [5], [6]. Indeed, a programmable voltage reference (PVR) enables dynamic voltage scaling, in digital blocks. On the other hand, in the analog domain, significant power saving can be obtained with voltage regulators exploiting a PVR and the unity feedback gain configuration, so removing the feedback resistors and the associated current consumption [3].

A low-power PVR generator can be implemented as either a static or a duty cycle-based architecture. The former approach guarantees a stable voltage reference V_{REF}, not affected by environmental temperature variations, with a constant current consumption I_{DD}. The continuous time (CT)-PVR in [7] derives the voltage reference from a leakage-based bandgap circuit to minimize the power consumption. The concept is shown in Fig. 1(a), where the value of V_{REF} is obtained by selecting with a multiplexer the tapping point in the bandgap load. This design achieves remarkable figures of merit, but it cannot provide any voltage amplification, limiting the reference programmability below a sub-bandgap output voltage. Additionally, it is penalized by the large process variations affecting the leakage-based bandgap [8]. An alternative static approach is the floating gate-based (FG)-PVR proposed in [9] and [10], and shown in Fig. 1(b). Here, a specific amount of charge is memorized in a floating gate, with a write procedure, to set the desired V_{FG}. This voltage is then buffered to guarantee sufficient driving capability. This PVR benefits of a simple and straightforward design, at the cost of the integration of a non-standard technology option.

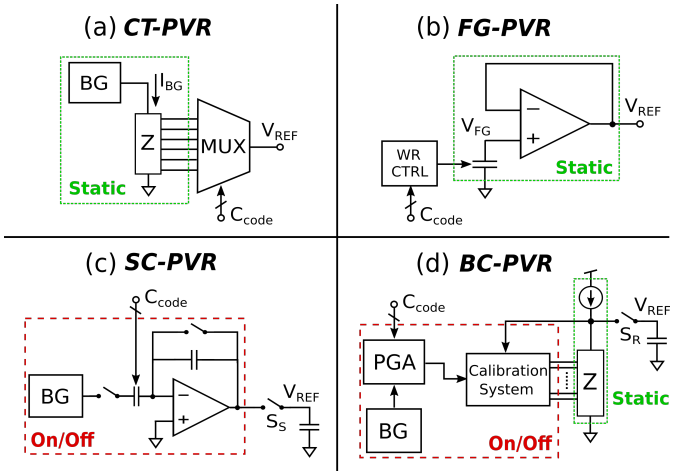

Fig. 1. (a),(b) Static architectures: continuous time and floating gate PVRs; (c),(d) Duty cycle-based architectures: switched-capacitor and background calibrated PVRs. C_{code} is used to set the desired reference value.

The duty cycle-based PVR architecture periodically calibrates a low-power voltage reference, from an accurate bandgap circuit with larger power consumption. The circuits used for the reference generation are powered down after each calibration, but they are periodically re-activated to compensate shifts of V_{REF} due to temperature variations. With large compensation periods T_s (i.e. low duty cycles DC), with respect to the

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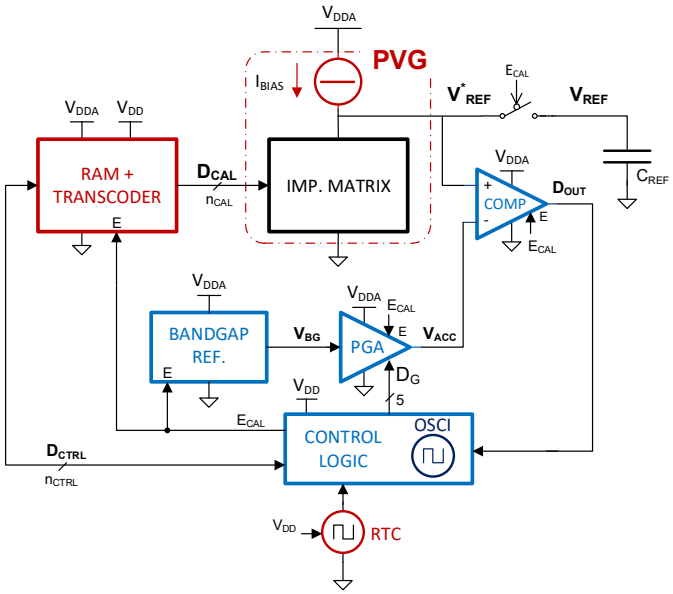

Fig. 2. Block diagram of the BC-PVR mixed-signal architecture. Red blocks: always on-state. Blue blocks: on-state only in the calibration/re-calibration phase.

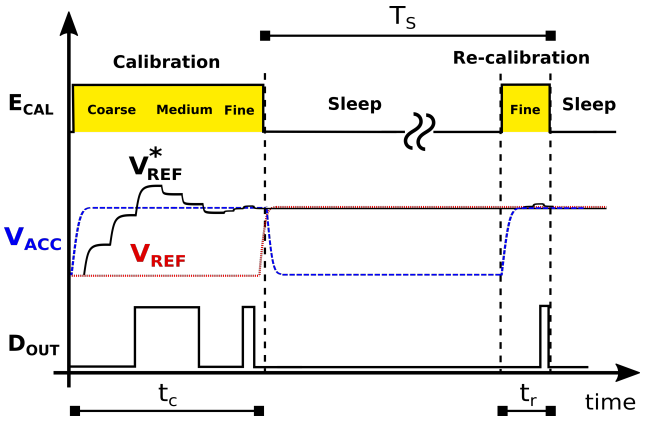

Fig. 3. Conceptual time graph of the BC-PVR. After the first calibration and the sleep phase, the control implements only periodic re-calibrations, much shorter than the first calibration.

calibration time t_r, the energy cost for the calibration becomes negligible, and the overall energy consumption is drastically reduced. In this approach, the maximum temperature derivative vs time of the application D_T provides the duty-cycle specification for the maximum acceptable variation of V_{REF}. Given that the energy consumption depends on the duty cycle, the best energy performance of this PVR architecture is obtained for small D_T values. As reported in [4], application domains like automotive, pharmaceutical, implantable, and food show maximum D_T values below 1°C/s, making duty cycle-based PVRs competitive with static PVRs. Among the duty cycle-based topologies, the switched-capacitor (SC)-PVR, derived from sample-and-hold (SH) bandgaps like those described in [11]–[13] and shown in Fig. 1(c), exploits a programmable gain amplifier (PGA) to set V_{REF} from a bandgap output voltage [14]. The so-generated reference is sampled with a capacitor and memorized, and then part of the power-hungry circuits is turned off. This PVR does not require any special technology option, and it can be easily ported among different nodes. The current consumption values reported in literature are in the order of few microampere, although a model for power-driven design optimization was recently proposed in [15]. This architecture suffers the leakage current through the sampling switch (S_S in Fig. 1(c)). This undesired effect grows with the temperature, forcing to shorten T_S and hence to increase the power consumption.

In this paper, we propose an alternative duty cycle-based approach: the background-calibrated (BC)-PVR. This topology aims to fully exploit the small D_T values proper of many application domains to minimize the current consumption of the reference generator circuit. Our architecture, conceptually shown in Fig. 1(d), periodically calibrates a static ultra low-power voltage reference generator (PVG) by means of an accurate voltage reference, generated by a bandgap circuit and amplified with a PGA circuit. After the calibration, all the power-hungry circuits are turned off, while the static PVG is kept on-state. A re-calibration system is turned on periodically to compensate for the effects of temperature variations on V_{REF}. Differently from the SH implementations, the BC-PVR does not suffer the leakage through the switch, thanks to the short duration of t_r and to the small voltage difference across S_R in Fig. 1(d). On the contrary, it inherently benefits of a large T_S, which reduces the power consumption without affecting the output voltage. The BC-PVR was designed and implemented in the TSMC 55-nm CMOS technology node, for a programming output reference range of more than 2 V, with a resolution of 100 mV, over the temperature range [-20 , 85] °C, with an ultra low current consumption.

This paper is organized as follows. Section presents II the architecture of the BC-PVR. Section III describes with equations the ultra low-power PVG. Section IV illustrates the implementation of a mixed-signal BC-PVR, and Section V reports the measurement results and a comparison with the PVR at the state of the art.

II. BC-PVR Architecture

The block diagram of the proposed ultra low-power, background-calibrated programmable voltage reference is shown in Fig. 2. A bandgap circuit provides the voltage V_{BG} with low temperature sensitivity, and a PGA is used for the amplification $V_{ACC} = G \cdot V_{BG}$, with the voltage gain G set by the control word D_G. V_{ACC} is used to calibrate the voltage V^*_{REF}, generated by the static low-power progammable voltage generator (PVG), made with a sub-nanoampere current source biasing a programmable impedance matrix. The calibration is carried out by a digital control, which targets the minimum voltage difference between V^*_{REF} and V_{ACC}. The control modifies the impedance in the matrix, by changing the code D_{CAL}. The output signal of a comparator D_{OUT} is used as feedback signal to close the calibration loop. At the end of the calibration, all the analog circuits used for the calibration are powered down to minimize the power consumption, except for a static random-access memory (SRAM), storing D_{CAL}, and the PVG, used to generate the static V^*_{REF}. In the digital

domain, the clock is disabled and the control enters the sleep mode, with no operations. In this phase, the reference voltage V_{REF} is generated by connecting V^*_{REF} to the on-chip capacitor C_{REF}. The capacitor improves the supply rejection and reduces the noise bandwidth of the programmable reference. During the calibration, C_{REF} is disconnected from PVG to reduce the settling time, relaxing the driving capability requirements.

In the system of Fig. 2 the PVG is a critical circuit. It sets the output range and the inaccuracy of the programmable reference, while being a relevant contributor to the system power consumption. It is worth to notice that the requirement for an ultra low-power consumption combined with a large output span leads to worse temperature coefficient and supply sensitivity, compared with standard bandgap circuits. Indeed, after calibration, the reference shares the non-negligible temperature coefficient of the PVG. Therefore, to compensate V_{REF} variations, due to possible environmental temperature variations, the mixed-signal system actuates a periodic verification and re-calibration of V^*_{REF}. While entering the sleep mode, the digital control launches a programmable counter. At the end of the counting, a signal EOC enables the clock generator and wakes up the digital control for the re-calibration. If a temperature variation has occurred in the sleep phase, causing a reference drift, the control restores V_{REF}, with a different D_{CAL} code. The timing diagram of the signals and the different phases controlling the BC-PVR are shown in Fig. 3.

The time required for re-calibration t_r depends on the D_T of the application and on the temperature coefficient (TC) of the PVG. The compensation period T_S must be defined from the user for the maximum acceptable peak-to-peak voltage reference variation V_{pp}. In the proposed design, the code D_{CAL}, stored in the SRAM, is used as starting point for the re-calibration procedure. This choice drastically shortens t_r, with respect to the time length of the first calibration t_c, and reduces the dynamic power consumption component of this phase. The control duty cycle of the BC-PVR is defined as:

$$DC = \frac{t_r(TC, D_T)}{T_S} \tag{1}$$

In applications with small temperature derivative vs time, DC can be also very small. This pushes the power consumption of the PVR close to its static component, since the contribution for the re-calibration to the average power consumption of the circuitry becomes negligible. The power consumption of the BC-PVR architecture is mainly ascribed to the PVG block, with an overhead due to the real-time clock (RTC) reference generator and to the leakage. Summarizing, the system in Fig. 2 provides a voltage reference with a temperature coefficient close to the original bandgap, but with a dramatic reduction of the power consumption. Moreover, the inclusion of the PGA in the loop guarantees the programmability of V_{REF}, at negligible additional power consumption cost.

III. Programmable Voltage Generator

The programmable voltage generator represents the static circuit in many PVR topologies. In reported PVRs like [16], [17], PVG is essentially based on a resistor with many tapping

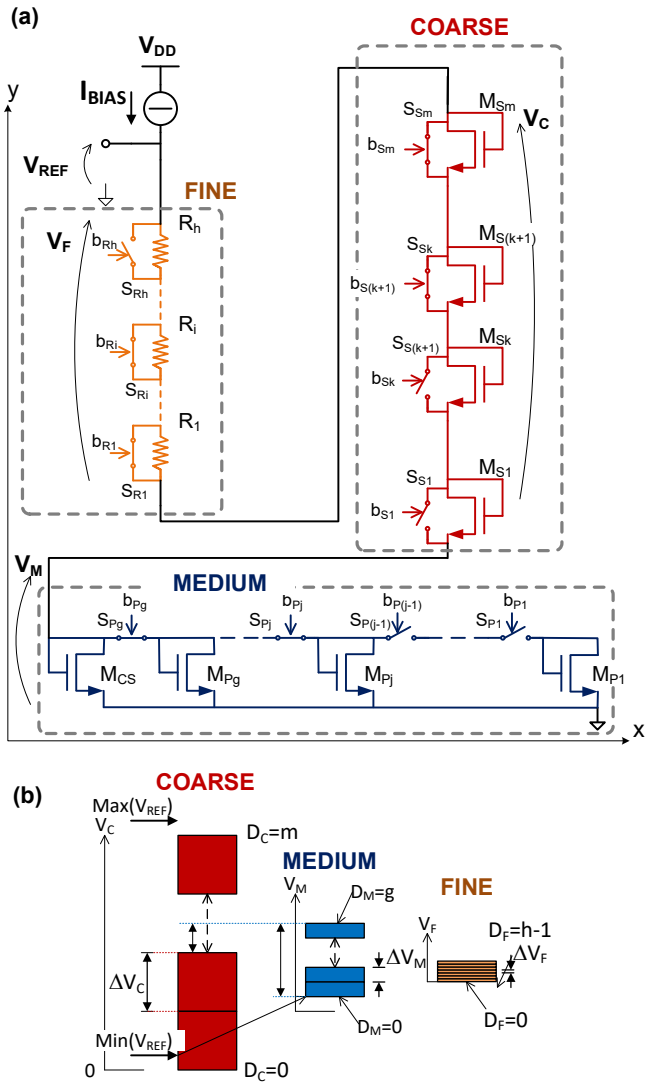

Fig. 4. (a) Programmable voltage generator based on a hybrid MOS and resistor network. (b) Conceptual scheme for the generation of a programmable voltage with BC-PVR.

points, biased with a current source. However, this implementation suffers the trade-off between the power consumption and the programmable output range V_{RG}, at fixed silicon area. Indeed, voltage ranges of volts cannot be obtained with nanoampere currents, unless using very big resistors, with large silicon area. This limitation can be circumvented with the hybrid network included in the proposed PVG, made with MOS transistors and resistors, and shown in Fig. 4(a). This structure allows a V_{RG} of volts and a reference accuracy of microvolts, when biased with a sub-nanoampere current, with a huge silicon area saving compared with the resistor-based PVG approach. In the network of Fig. 4(a), V_{REF} is given by the additive contributions of three sections, with different resolutions, biased with the same current I_{BIAS}. The network corresponds to a matrix of impedance, with, at the top, a resistor string and a stack of MOS transistors in diode configuration programmed in series, and, at the bottom, a bank of MOS transistors in diode configuration programmed by changing the number of devices connected

in parallel. The stack of MOS diodes M_{S1}-M_{Sm} in series enables a large V_{RG}, in spite of a sub-nA I_{BIAS}, with the coarse resolution ΔV_C. The medium section, made with a bank of MOS diodes connected in parallel, is designed to provide the intermediate resolution ΔV_M. The overall voltage V_M of this section increases to the maximum value, if the g switches are progressively open from S_{P1} to S_{Pg}. This maximum V_M corresponds to the gate-source voltage of the corner-stone MOS diode M_{CS}, biased with the full I_{BIAS}. The fine reference resolution ΔV_F is set by a programmable resistance. Fig. 4(b) shows how V_{REF} is obtained from the superposition of the output of each section, from coarse to fine. It also highlights how the summing of the voltage steps of each section must be larger than the voltage resolution of the next block. This condition is mandatory to guarantee the reference resolution ΔV_F on the entire V_{RG}.

A. PVG Design Equations

All the MOS transistors in the circuit of Fig. 4(a) are expected to be in the weak inversion (W.I.) region, with the following current-voltage equation [18]:

$$I_{D<x>} = I_{SS} \cdot \left(\frac{W_{<x>}}{L_{<x>}}\right) e^{\frac{V_{GS<x>} - V_{TN}}{(n_n \cdot v_{th})}} \tag{2}$$

where $I_{D<x>}$, $V_{GS<x>}$, and $(W_{<x>}/L_{<x>})$ are, respectively, the drain current, the gate-source voltage, and the aspect ratio of the $M_{<x>}$ transistor, with the gate and the drain terminals shorted. v_{th} and V_{TN} are the thermal and the threshold voltages, respectively, and n_n is the slope factor. I_{SS} is the sub-threshold NMOS saturation current, normalized to the aspect ratio. The effect of the drain-source voltage, $V_{DS<x>}$, has been neglected in equation (2), considering the diode configuration and assuming $V_{GS<x>}$ much higher than v_{th}.
In the coarse section of Fig. 4(a) all the NMOS devices M_{S1}-to-M_{Sm} are sized with the same nominal aspect ratio (W_C/L_C). From (2), this leads to a constant voltage step, when changing the state of a switch in the stack:

$$\Delta V_C = V_{TN} + n_n \cdot v_{th} \cdot \left[\ln\left(\frac{I_{BIAS}}{I_{SS}}\right) - \ln\left(\frac{W_C}{L_C}\right)\right] \tag{3}$$

A complementary thermometer code is used for the *m*-bit word D_C, setting the switches of this section. The output voltage $V_C(D_C)$ progressively increases from $D_C \equiv b_{Sm}..b_{S1}$ = 1..1, corresponding to *r* = 0, to $D_C \equiv b_{Sm}..b_{S1}$ = 0..0, for *r* = *m*, where *r* is the value of D_C in decimal format:

$$V_C(r) = r \cdot \Delta V_C \tag{4}$$

A smaller voltage step V_M is obtained with a programmable bank of MOS diodes connected in parallel: the medium section. The programmability of this block is implemented along the x-axis direction. The switches are controlled by the g-bit word $D_M \equiv b_{Pg}..b_1$, coded in complementary thermometer format and with a value, *j*, ranging from 0 to *g*. With $D_M = j$ and $j < g$, the MOS transistors from M_{Pg} to $M_{P(j+1)}$ are connected in parallel to M_{CS}, whereas, if $j \geq 1$, the devices from M_{Pj} to M_{P1} are disconnected from M_{CS}. From (2), the

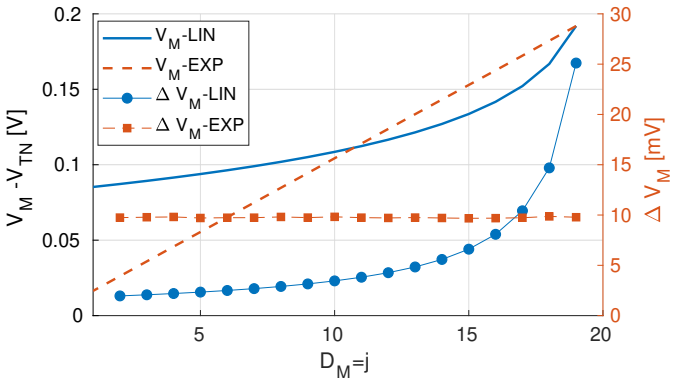

Fig. 5. V_M vs. D_M (left y-axis) and ΔV_M (right y-axis) with a linear and exponential scaling of the devices in the medium resolution section.

equation of the output voltage of this section as a function of D_M = *j*, for j < *g*, is:

$$\begin{aligned} V_M(j) =& V_{TN} + n_n \cdot v_{th} \cdot \left[\ln\left(\frac{I_{BIAS}}{I_{SS}}\right) + \right. \\ & \left. - \ln\left(\frac{W_{CS}}{L_{CS}} + \sum_{i=j+1}^{g} \frac{W_{Pi}}{L_{Pi}}\right)\right] \end{aligned} \tag{5}$$

$D_M = g$ generates the maximum output value of the medium section. This value corresponds to the gate-source voltage of M_{CS}, biased with the maximum drain current:

$$V_M(g) = V_{TN} + n_n \cdot v_{th} \cdot \left[\ln\left(\frac{I_{BIAS}}{I_{SS}}\right) - \ln\left(\frac{W_{CS}}{L_{CS}}\right)\right] \tag{6}$$

It is worth to notice that M_{CS} must be sized with a smaller aspect ratio than the devices in the coarse section, to set the maximum value of V_M larger than the coarse step, i.e. $V_M(g) > \Delta V_C$. Furthermore, the voltage range of the medium section $V_M(g) - V_M(0)$ must exceed the coarse step, consequently the voltage $V_M(g) - \Delta V_C$ must be larger than the minimum of the medium section $V_M(0)$, as shown in Fig. 2(b). This requirement sets a constraint on the minimum value of the sum of the aspect ratios of the NMOS devices in the medium section, according to (5).
The value of the voltage step of the medium section ΔV_M depends on the number and on the aspect ratios of the devices connected to M_{CS}. From (5) the voltage step at D_P = j is:

$$\begin{aligned} \Delta V_M(j) &\equiv V_M(j) - V_M(j-1) \\ &= n_n v_{th} \ln\left(\frac{1 + \sum_{i=j}^{g} \alpha_i}{1 + \sum_{i=j+1}^{g} \alpha_i}\right) \end{aligned} \tag{7}$$

where α_i is the aspect ratio of M_{Pi} normalized at M_{CS}:

$$\alpha_i \equiv \frac{W_{Pi}/L_{Pi}}{W_{CS}/L_{CS}} \tag{8}$$

Therefore, with all the devices in the parallel bank sized with the same aspect ratio, $\Delta V_M(j)$ is not constant but increases

with *j*. Instead, a constant voltage step can be obtained with an exponential-scaling of the aspect ratios:

$$\frac{W_{Pg}}{L_{Pg}} = \frac{W_{CS}}{L_{CS}} \cdot (\Omega - 1) \quad (9)$$

$$\frac{W_{P(j-1)}}{L_{P(j-1)}} = \left(\sum_{i=j}^{g} \frac{W_{Pi}}{L_{Pi}} + \frac{W_{CS}}{L_{CS}} \right) \cdot (\Omega - 1) \quad (10)$$

where

$$\Omega \equiv \exp\left(\frac{\Delta V_M}{n_n \, v_{th}} \right) \quad (11)$$

The exponential scaling makes ΔV_M not dependent on I_{BIAS} and I_{SS}, provided that all the involved transistor are biased in the weak inversion region. The output voltages of the medium section with linear and exponentially scaled devices are compared in Fig. 5. In these example graphs, W_{P1}/L_{P1} = 1 and the exponential scaling of the aspect ratio has been set from equation (10) for $\Delta V_M \approx 10$ mV.

In the impedance matrix of Fig. 4, the fine step is provided by a resistors string with binary-scaled values, i.e. R_1 to R_h. The control word D_F, coded with complementary binary format, drives k-switches, with $k \in [0, h-1]$, for a resistance value $R_k = 2^k \cdot R_{LSB}$ and a resolution $\Delta V_F = R_{LSB} I_{BIAS}$. The output voltage with D_F = *k* is:

$$V_F(k) = 2^k \, R_{LSB} \, I_{BIAS} \quad (12)$$

The reference voltage generated by the PVG block is given by the superposition of the outputs of the three sections:

$$V_{REF}(D_C, D_M, D_F) = V_C(r) + V_M(j) + V_F(k) \quad (13)$$

The variation of V_C and V_M over the process and temperature design (PT) space are correlated, since they are both obtained from the same NMOS transistor. In the fine section, polysilicon resistors are used for linearity reasons, leading to a substantial uncorrelation over the PT space of V_F with respect to V_C and V_M. Additionally, V_F exhibits a linear dependence on I_{BIAS}, whereas the V_C and V_M contributions exhibit the same logarithmic dependence, as highlighted by (3) and (6). Therefore, in the design of the impedance matrix, V_F must be oversized with respect to the typical corner, to guarantee the overlapping of ΔV_M over the PT space, as shown in Fig. 4(b). Additional devices are required also in the medium section, taking into account the difficult layout matching, due to the exponential scaling, and the process tolerance affecting the NMOS model parameters. In the coarse section, oversizing is necessary to ensure the target range V_{RG} on the process corners. From equations (3) and (5), the main contributors to the process non-ideality affecting V_{REF} are the threshold voltages and the slope factor. I_{SS} and I_{BIAS} have lower impacts due to the logarithmic dependence. Process variations of I_{BIAS} and of the polysilicon resistance impacts the to die-to-die V_F. However, by combining a PTAT current source and polysilicon resistance with negative TC, is possible to generate an almost constant ΔV_F on temperature. The temperature sensitivity of V_{REF} is mainly due to V_{TN}, which exhibits a negative temperature coefficient, and to v_{th}, whereas the slope factor n_n exhibits a negligible temperature dependence [19]. From equations (3) and (5):

$$\begin{aligned} \frac{dV_{REF}}{dT}(r,j) \approx (r+1)\,\frac{dV_{TN}}{dT} + \\ + (r+1)\, n_n \frac{k}{q}\, ln\left(\frac{I_{BIAS}}{I_{SS}}\right) + \\ - n_n \frac{k}{q}\, ln\left(\left(\frac{W_C}{L_C}\right)^r + \frac{W_{CS}}{L_{CS}} + \sum_{i=j+1}^{g} \frac{W_{Pi}}{L_{Pi}} \right) \end{aligned} \quad (14)$$

where *k* and *q* are the Boltzmann constant and the electron charge, respectively. Since, the absolute value of the temperature coefficient of V_{TN} is usually higher than k/q, V_{REF} exhibits a complementary dependence to the absolute temperature (CTAT), as confirmed by the measurement results reported in Section V. It is worth to notice that the temperature coefficient of V_{REF} depends on the value of the code D_C, due to the multiplication of V_{TN} in equation (4). Equation (14), together with the D_T of the specific application and D_{CTRL}, allows the sizing of DC in (1) for every V_{REF}.

TABLE I
PARAMETERS OF THE IMPLEMENTED PVG

	value	unit
W_C/L_C	0.12/1	$\mu m/\mu m$
W_{CS}/L_{CS}	0.12/5	$\mu m/\mu m$
W_{Pg}/L_{Pg}	0.12/26	$\mu m/\mu m$
ΔV_C	160	mV
ΔV_M	7	mV
ΔV_F	30	μV
D_{CAL}	104	Bits
m	41	
g	54	
h	9	

IV. System Implementation

The BC-PVR shown in Fig. 2 and described in Section II was designed and implemented in TSMC 55-nm CMOS technology, with thick-oxide devices, withstanding up to 3.6 V across the gate-source and gate-drain terminals. The bias current of the PVG circuit in Fig. 4 is generated from a resistorless, leakage-based current reference generator, derived from the circuit proposed in [20]. The typical current value at 27 °C is $I_{BIAS} \approx 600$ pA. The resistors and the MOS devices in the programmable matrix have been sized from the design equations in Section II, taking into account the process tolerance and the temperature range. To minimize the lower bound of the output range, NMOS transistors with extreme low-voltage threshold V_{TN} have been chosen for the impedance matrix. Moreover, since V_{TN} is a major component of the coarse voltage steps, the lower the NMOS threshold, the lower the overall aspect ratio of the devices in the medium section in Fig. 4(a), with benefits in terms of silicon area. The number of devices *g* in the medium section sets the voltage step ΔV_M that must be overlapped by the voltage range of the fine section. This choice impacts the minimum value of $V_F(k)$, where high-density poly-silicon resistors have been used to

limit the silicon area. The device sizes and the main parameters of the PVG in Fig. 4 are summarized in Tab. I.

A. PVR Analog Section

The schematic of the bandgap reference circuit used in the BC-PVR, is shown in Fig. 6 [21]. The circuit section including the native-MOS devices M_1 and M_2, and the resistors R_1 and R_2, generates the current I_{BG}, proportional-to-absolute temperature (PTAT). This current is used to bias the base-to-emitter diode of substrate pnp transistor Q_B, and to generate a PTAT voltage across the high-value polysilicon resistor R_B. The combination of this PTAT voltage and of the emitter-to-base voltage, with complementary-to-absolute temperature (CTAT) behavior, leads to the output reference voltage:

$$V_{BG} = V_{EB} + \frac{N n_n v_{th} R_B}{R_1} \cdot ln\left[N \cdot (K_1 + 1)\right] \qquad (15)$$

where V_{EB} is the base-to-emitter voltage of Q_B, N = R_1/R_2, n_n the slope factor of the native-MOS devices, v_{th} the thermal voltage, and $K_1 \equiv (W/L)_6/(W/L)_3$ the nominal current ratio of the current mirror M_3-M_6 in Fig. 6. The current ratio of the mirror M_3-M_4 is $N \cdot (K_1 + 1)$.

This bandgap reference circuit does not need a start-up circuit. Indeed, the start-up is inherently safe, due to the absence of additional bias points for the PTAT current generator [21]. This feature is particularly relevant in the proposed PVR architecture, where the bandgap circuit is turned-on periodically, at every re-calibration. The bandgap circuit in Fig. 6 exhibits a typical current consumption of 420 nA and a measured temperature sensitivity of 10 ppm/$^\circ C$, over the considered temperature range. The approach proposed in this paper can support every bandgap topology. However, since the calibration procedure is based on the amplified reference voltage, the best achievable temperature sensitivity is bounded at the bandgap performance. Moreover, the bandgap power consumption requirements can be relaxed, since the circuit is

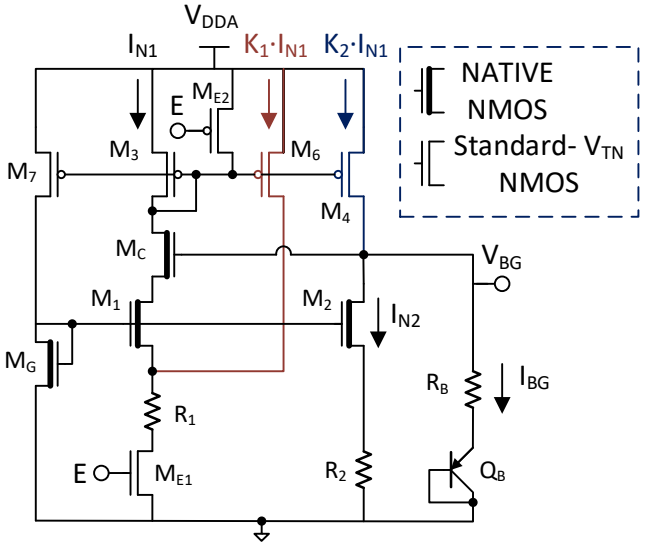

Fig. 6. Schematic view of the bandgap reference included in the silicon implementation of the BC-PVR [21].

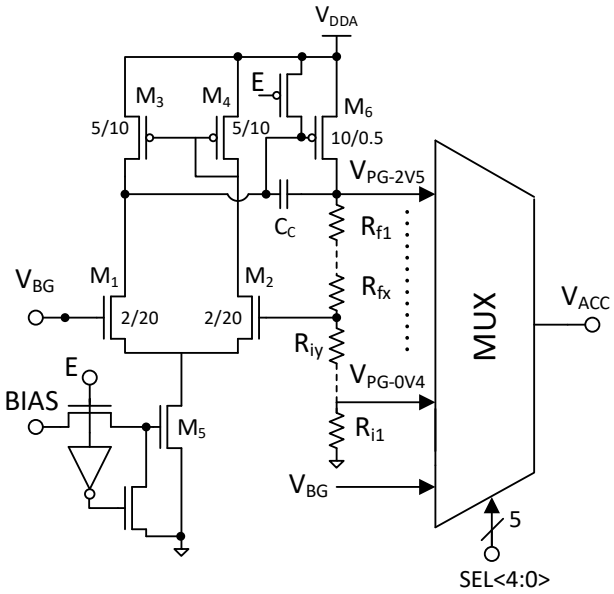

Fig. 7. Schematic view of the amplifier with gain programmability.

turned-on only during the calibration/re-calibration phases, and the contribution to the average power consumption is drastically limited by the duty-cycled operation. Therefore, bandgap topologies optimized for temperature sensitivity, sample-to-sample inaccuracy, and occupied area should be preferred for the BC-PVR architecture.

In the implemented BC-PVR, the PGA is designed to scale the bandgap output voltage V_{BG} over the nominal output range [0.42 , 2.52] V, with twentytwo steps of resolution V_S = 100 mV. As shown in the schematic circuit in Fig. 7, the amplifier is based on the linear voltage regulator architecture, with Miller compensation. An analog multiplexer (MUX), connected to the tapping points of the resistor strings $R_{f1} - R_{fx}$ and $R_{i1} - R_{iy}$ and controlled with the 5-bits digital word D_G<4:0>, enables the selection of V_{ACC}. One MUX input is dedicated to the bandgap output voltage. It is used to implement a PGA by-pass function and calibrate V_{REF} with V_{BG}. This solution removes the contributions of the PGA offset and noise voltage from V_{REF}. It also allows the evaluation of the PGA performance by comparing the bypass solution with the unitary gain configuration. The design relies on the transistor sizing to limit the PGA input referred offset V_{OS-PGA}. As for the bandgap circuit, the PGA is driven in power down during the sleep phase of the system.

The analog section includes a comparator circuit (COMP) to provide the calibration feedback signal D_{OUT} to the digital control, Fig. 8(a). Rail-to-rail input operation is obtained with the combination of two comparators NCOMP, whose schematic diagram is shown in Fig 8(b), and PCOMP with complementary input pairs. The comparators operate alternatively, depending on the target V_{ACC} selected by the most significant bit of the PGA control word D_G<4>. The multi-stage linear amplifier is preferred to a latch comparator to minimize the kick-back noise, considering the large output resistance of the PVG. The first stage provides a small voltage gain to limit the swing on M1-M2, so minimizing the kick-

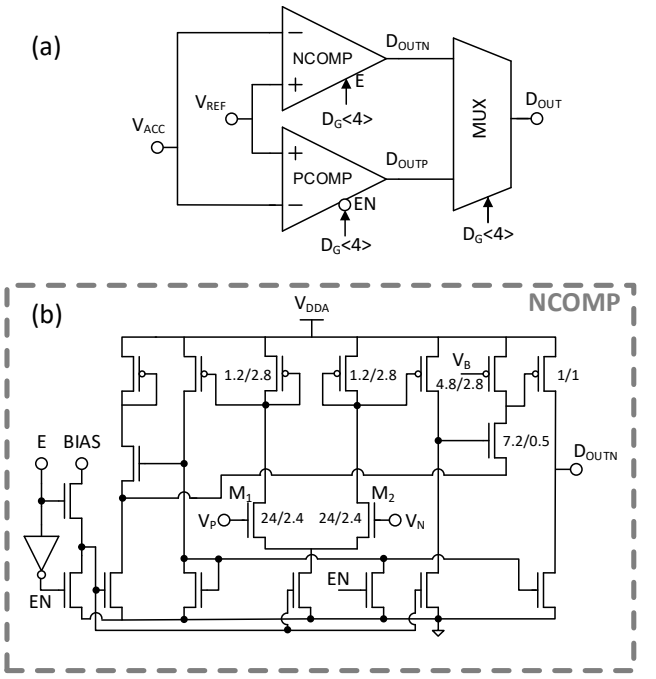

Fig. 8. (a) Block diagram of the rail-to-rail comparator. (b) Schematic view of the comparator NCOMP used for the lower half of the output range

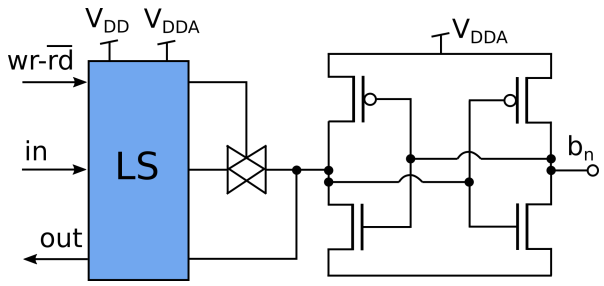

Fig. 9. Schematic view of the designed SRAM bit-cell.

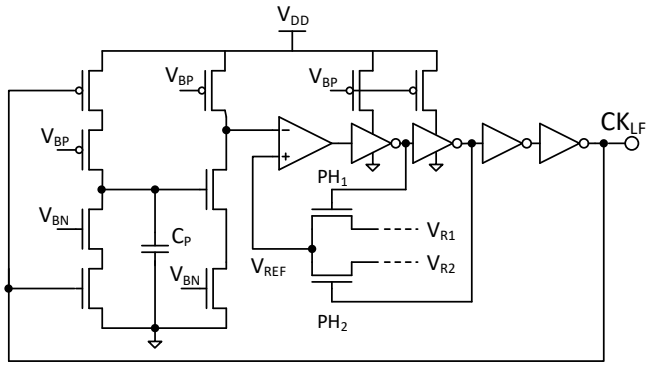

Fig. 10. Schematic view of the low-frequency oscillator included in the RTC.

back on the input nodes. Moreover, the time allocated by the digital control for the settling of every calibration step allows to tolerate with margin the residual kick. The current consumption is approximately 250 nA for both comparators. The overall error on V_{REF} at the end of the calibration phase is affected by non-idealities in the analog section. In particular, the main sources are the relative inaccuracy (ε_{acc}) and the effective resolution (ε_{res}) of the system, together with the inaccuracy of the bandgap reference (ε_{bg}):

$$V_{REF} = V_{BG} \cdot G + \varepsilon_{acc} + \varepsilon_{res} + \varepsilon_{bg} \cdot G \quad (16)$$

$$\varepsilon_{acc} = V_{BG} \cdot \Delta G + |V_{OS-PGA}| \cdot G + |V_{OS-C}| \quad (17)$$

$$\varepsilon_{res} = \sqrt{\frac{V_{LSB}^2}{12} + G^2 \cdot \sigma_{n-PGA}^2 + \sigma_{n-C}^2 + \sigma_{n-PVG}^2} \quad (18)$$

where and σ_{n-PGA} and σ_{n-C} are respectively the rms noise voltage of the PGA and COMP, ΔG is the absolute gain error of the PGA with respect to the nominal value G, $V_{LSB} = \Delta V_F$ and σ_{n-PVG} are the nominal resolution and rms ouput noise of the PVG.

B. PVR Digital Domain

The BC-PVR architecture of Fig. 2 incorporates an SRAM to store the binary control word D_{CTRL}, and a transcoder logic circuit, which explodes D_{CTRL} in the PVG calibration code D_{CAL}. D_{CTRL} is a 21-bit word, where nine bits are used for the fine section, while the medium and the coarse sections require six control bits each. The SRAM is based on the 6T-cell shown in Fig. 9 [22]. It includes two inverter gates in latch configuration and a transmission gate to access the memory in the read/write phases. Since the control code must be available also in the sleep phase, the SRAM and the transcoder circuit are custom designed, in the analog domain. Level shifters are required at the interface between these block and the digital control. The level shifters are powered down during the sleep phase.

Two integrated oscillator circuits are used for the synchronization of the system. A low-frequency oscillator is used in combination with a binary counter to generate the RTC reference and set T_S. When the counter reaches the end of counting, a wake-up signal (EOC) is sent to the digital control to start the re-calibration phase. The BC-PVR architecture does not need an RTC with extremely low temperature sensitivity. Indeed, considering the temperature derivative vs time of the target applications and the average I_{DD} consumed, the system can tolerate relatively large spreads of the RTC and T_S, with very limited penalties in terms of energy consumption. On the contrary, the use of an RTC generator very accurate in temperature, like those reported in [23], [24], would worsen the BC-PVR energy performance, and require dedicated pads and additional area for the external quartz crystal. Therefore, the integrated oscillator of Fig. 10, similar to a relaxation oscillator, was preferred in this design. The oscillator is based on the charging and the discharging of the capacitor C_P, with a current I_B, regulated with the bias voltage V_{BN} and V_{BP}, and controlled by the output of a comparator. At the start up, a pMOS current generator charges C_P, and the rising voltage on the capacitor is compared to the reference voltage V_{R1}, by means of a transconductance amplifier. When the output of the comparator toggles, the selection disables the charging current source and enables an nMOS current sinker to discharge C_P. At the same time, the comparator reference voltage is changed to the lower reference value V_{R2}. This sequence guarantees

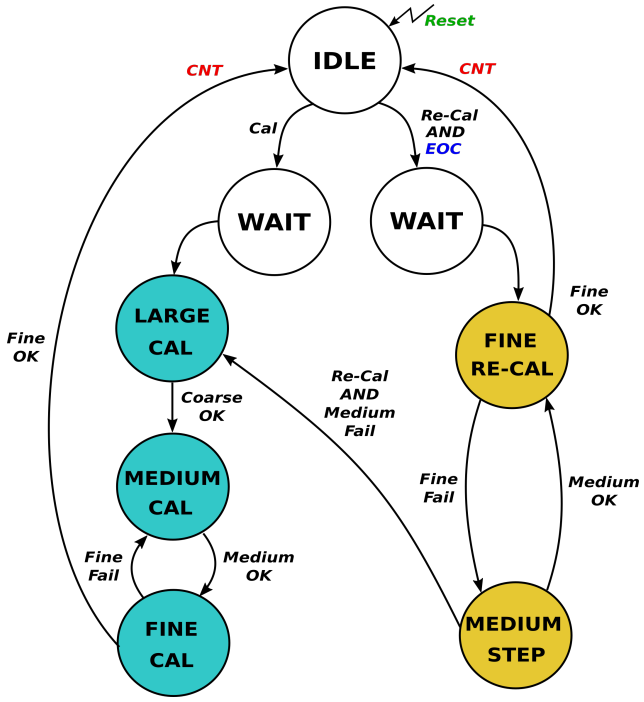

Fig. 11. State diagram of the calibration-control FSM. Azure states: calibration routine. Orange states: re-calibration routine.

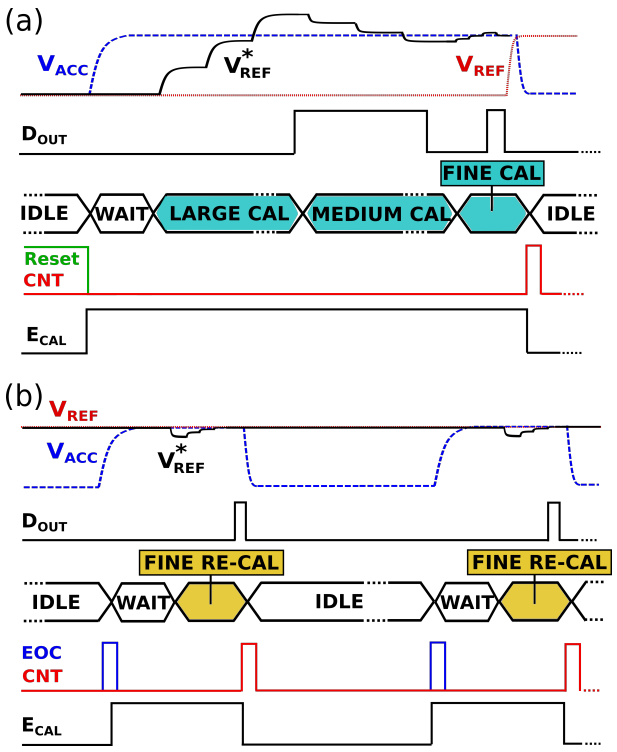

Fig. 12. Timing diagrams: (a) Calibration phase - (b) Re-calibration phase.

a periodic triangular-shape wave on C_P, used to generate a square-wave at the output. At steady state, if the charge and discharge currents are equal, the period of the output CK_{LF} is approximately $t_{LF} = 2C_P \cdot (V_{R1} - V_{R2})/I_B$. The reference voltages V_{R1} and V_{R2} are generated internally with a dedicated branch. Despite the relatively large temperature spread, this topology guarantees a simple design, a small area, and very low current consumption. The period of the RTC can be programmed by the user for different D_T and to compensate for process variations, by externally selecting among binary-scaled C_P values and controlling the bits of a register at the output of the oscillator, used as frequency divider. In our BC-PVR implementation, T_S can be set in the range [0.005 - 5] s. The current consumption of the RTC is 1.8 nA at 27 °C. The clock signal for the digital control is generated by a current-starved ring oscillator [25]. This circuit is switched off in the sleep phase and resumed by the RTC at the end of the counting. Also in this oscillator the specification on the temperature sensitivity is relaxed, allowing a simplified design with small power consumption and area. Indeed, given the short duration of the re-calibration phase with respect to the sleep phase for the target applications, a variation of the clock frequency due to temperature, causing for instance a longer enabling of the analog blocks, does not significantly degrade the energy system performance. The oscillator operates with a nominal frequency $f_{ck} = 30$ kHz, with a current consumption of 35 nA, at 27 °C.

C. Digital Control and Calibration Procedure

The digital self-calibration procedure minimizes the off-chip interaction and guarantees large flexibility. Therefore, the implemented BC-PVR architecture includes a digital finite state machine (FSM), which controls all the circuits in the system to carry out the calibration and the successive re-calibrations of V_{REF}. Fig. 11 shows the state diagram of the main FSM controlling the calibration and re-calibration of the BC-PVR. The azure circles refer to the states that implement the calibration routine, operating on the different sections of the PVG. The states in yellow refer to the re-calibration routine. The target of these routines is the minimization of the voltage difference between V^*_{REF} and V_{ACC}, operating on the PVG by means of the code D_{CTRL}, using the output of the comparator D_{OUT} as feedback signal. A WAIT state is included in both the calibration and re-calibration branches to allow the settling of V_{ACC}, before acting on D_{CTRL} and on the PVG network. The MEDIUM STEP state in the re-calibration sequence acts again on the bank of MOS diodes in parallel, to cope with possible failures of the fine tuning in re-calibration. Indeed, if T_S is set too large with respect to the temperature derivative vs time of the target application, the variation of V_{REF} in the sleep phase could exceed the voltage range of the fine section, leaving the FSM locked in an undefined state. Fig. 12 (a) shows the timing diagram of the main signals involved in the calibration phase. The first calibration begins after the reset. The analog blocks are enabled via E_{CAL} to generate the V_{ACC} defined by the user, and the matrix is programmed with V^*_{REF} below the minimum programmable V_{ACC}. All the switches m in the coarse section of Fig. 4(a) are closed, all the j switches in the medium section are open, and the resistor string is programmed in the middle configuration. In the first part of the routine, V^*_{REF} is increased by opening the switches in

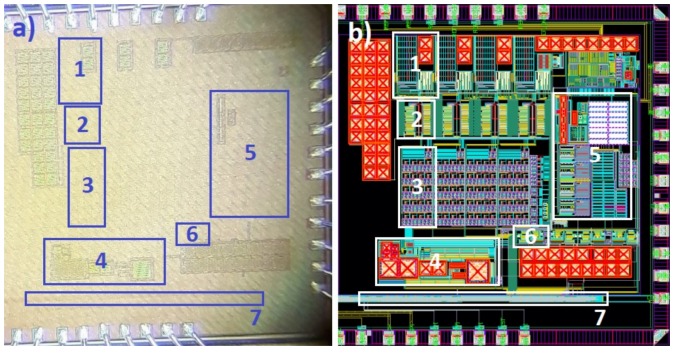

Fig. 13. a) Die micro-photograph, b) layout view of four BC-PVR. Highlighted blocks: (1) PVG - 170x300 μm^2, (2) Transcoder - 165x170 μm^2, (3) SRAM memory - 155x320 μm^2, (4) Timing systems - 625x230 μm^2, (5) Bandgap and PGA - 450x650 μm^2, (6) Comparators - 160x100 μm^2, (7) Digital control - 900x45 μm^2.

TABLE II
TEST-CHIP SUMMARY

Parameter	Value	Unit
Tech. Node	55	nm
Num. of Outputs	4	–
1-PVR Area	0.28	mm^2
$V_{DDA} - V_{DD}$	3.2 , 1.2	V
V_{REF}	0.42 - 2.52	V
Temp. Range	-20 - 85	^{o}C
T_S	0.005 - 5	s

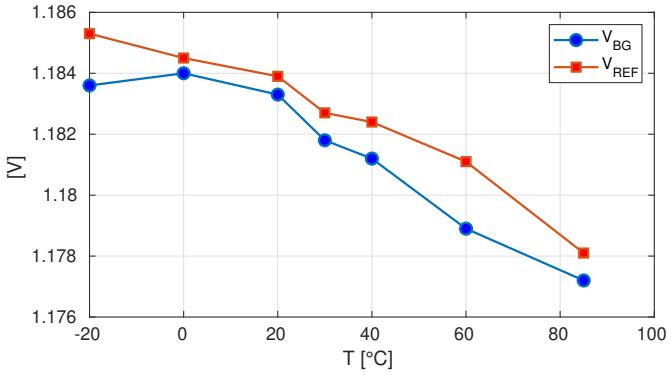

Fig. 14. PVR output V_{REF} after calibration (squares) and bandgap output reference V_{BG} (circles)

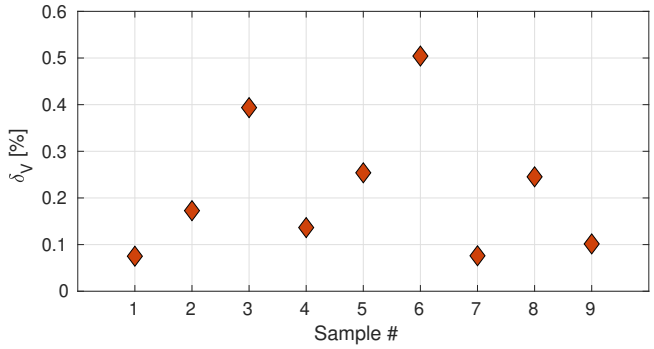

Fig. 15. Voltage difference between V_{BG} and V_{REF} on nine samples, at T = 30 ^{o}C, after calibration.

the coarse section and adding in series the MOS diodes of the stack M_{S1}-M_{Sm}. When V_{REF} exceeds V_{ACC}, D_{OUT} toggles, this phase is stopped, and the control starts to operate on the medium section. By closing the switches in the bank M_{P1}-M_{Pg}, the contribution of the medium-resolution section V_M is progressively reduced, as in equation (13). When V^*_{REF} drops below V_{ACC}, D_{OUT} flips again, the digital control stops to operate on the medium section, to proceed with the calibration of the fine-resolution section. A dichotomic search algorithm is implemented through a successive approximation calibration (SAR), by opening the control switches and adding in series binary-scaled resistors [26]. When the calibration is finished, the code D_{CTRL} is memorized in the SRAM, and the digital control turns off the unnecessary circuits, enabling the RTC generator for the sleep phase, with the pulse CNT. The timing diagram of Fig. 12(b) shows the control sequence for the re-calibration routine. The system operates on the impedance matrix starting from D_{CRTL} stored in the SRAM. In standard operation, the signal EOC wakes up the digital control, which re-enables the analog section via E_{CAL}, and actuates a new SAR calibration on the fine section of PVG. When the new D_{CRTL} code is found, the system re-enters the sleep phase. Considering the D_T values reported in literature, t_r is expected to be much shorter than t_c in Fig 3, allowing a large energy saving [27]–[31].

V. EXPERIMENTAL RESULTS AND DISCUSSION

A test chip was implemented in TSMC 55-nm CMOS technology, with four BC-PVRs sharing the duty-cycled analog blocks and the control circuits. Given the D_T values of application domains like automotive, pharmaceutical, implantable, and food, multiple references can be calibrated in series with almost no impact on accuracy and energy performance, but with large area saving. The four PVR are designed to operate over the [-20 , 85] ^{o}C temperature range, with the programming range [0.42 , 2.52] V. The nominal digital and analog supply voltages are $V_{DD} = 1.2$ V and $V_{DDA} = 3.2$ V, respectively. The die photograph and the layout views of the implemented system are shown in Fig. 13, with an average area per BC-PVR of 0.28 mm^2. A single PVG, with the related SRAM and transcoder, occupies approximately the 47% of a BC-PVR area, while $C_{REF} = 50$ pF takes the 3%. The 26% of the area is occupied by the shared analog blocks, and the 17% by the timing circuits and the digital control. The test-chip summary is reported in Table II.

Experimental measurements have been carried out with an ACS DY110 climatic chamber on multiple silicon samples. The test chip package is a 48-pin dual-in-line ceramic package, mounted over a dedicated test-board. The temperature of the package was measured with a Platinum PTAT resistor (PT-100). The temperature stability of the experimental setup was within ±0.1 °C. Fig. 14 shows the measured BC-PVR output voltage V_{REF} after the calibration compared to the

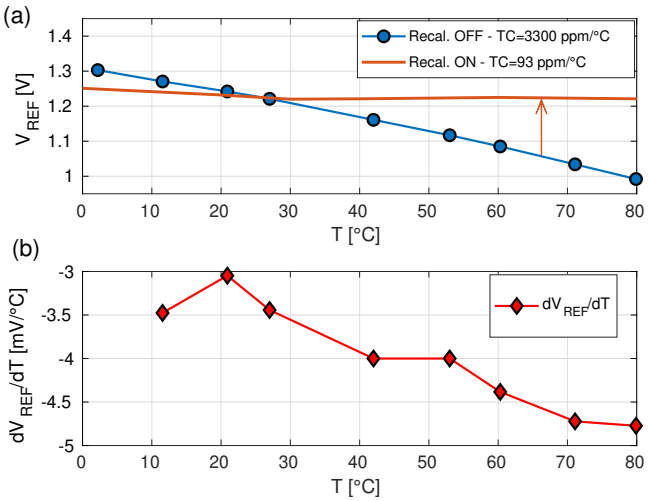

Fig. 16. (a) PVG output with calibration frozen vs. temperature (circles), and with calibration running (orange, solid line), for $T_S = 1$ s and $V_{pp} = 300$ μV. (b) V_{REF} temperature sensitivity with calibration frozen (diamonds).

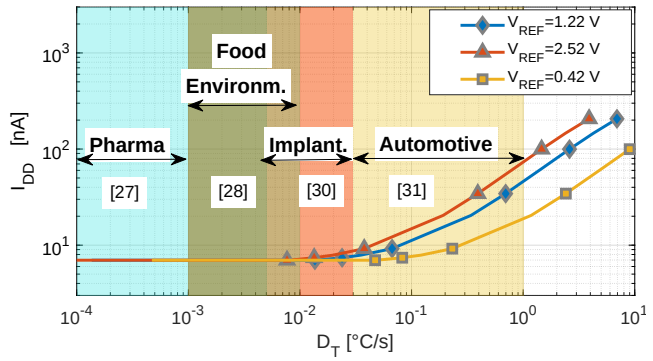

Fig. 17. BC-PVR current consumption at 27 ^{o}C for typical ranges of D_T in different application domains.

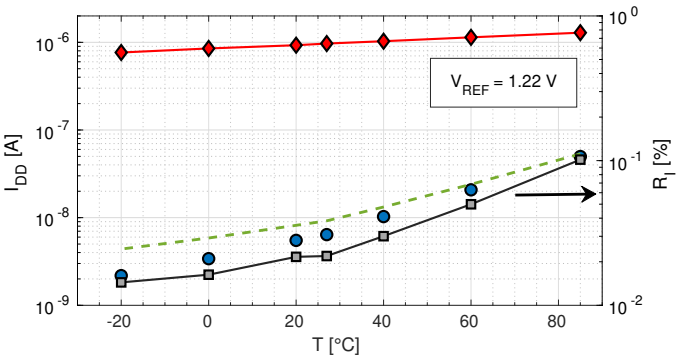

Fig. 18. Left axis: PVR current consumption vs. temperature in sleep (I_{DD-s}, blue circles) and in re-calibration (I_{DD-rc}, red diamonds). Overall I_{DD} for T_S = 1 s, green, dashed line. Right y-axis: Current ratio I_{DD}-to-bandgap vs. temperature (grey squares).

bandgap reference voltage V_{BG}, over the full temperature range. As shown in Fig. 15, an average inaccuracy of 0.21% and a maximum inaccuracy of 0.5% have been measured on a set of nine samples, at T = 30 °C. In these measurements the PGA was bypassed. The residual error after the calibration routine can be mainly ascribed to the offset voltage of the comparator in eq. (17). Fig. 16(a) shows the measured PVG output over temperature with the calibration running and with the calibration frozen at $V_{REF} = 1.22$ V at 27 ^{o}C. In these measurements the PGA gain was set to one. Fig. 16(a) also reports the TC values in the two operating conditions, highlighting the remarkable benefit of the calibration. The TC performance can be further improved by removing the comparator and PGA offset with a cancellation technique, not included in this silicon implementation [14]. Fig 16(b) shows the measured TC of the PVG with the calibration frozen. The PVG has a negative TC, with an average value of approximately 4 mV/^{o}C and a maximum value of 4.7 mV/^{o}C. These values are in good agreement with those obtained from equation (14) in Section III-A. As explained in the previous sections, the BC-PVR exploits the duty cycle operation to limit the power consumption. The choice of the compensation period T_s is defined from TC of the PVG, from the maximum acceptable peak-to-peak variation of the reference, V_{pp}, and from the maximum D_T expected for the specific application. Fig. 17 reports the measured average I_{DD} of the BC-PVR plotted vs. D_T. The graph includes three curves for the output voltage set at the maximum, at the minimum of the range, and at $V_{REF} = 1.22$ V. All the curves are obtained for $V_{pp} = 300$ μV. With $V_{REF} = 1.22$ V, for temperature derivative vs time below 0.017 $°C/s$, requiring a $T_S < 4$ s, the current consumption of the PVR is pushed at its intrinsic lower bound $I_{DD} = 7$ nA, set by the sum of the consumption of the always-on PVG and RTC generator and the leakage current. The minimum and the maximum V_{REF} lead to the boundary I_{DD} curves of the whole PVR, as expected from equation (14). Given D_T, the maximum V_{REF} always corresponds to the maximum I_{DD}, since the larger the number of devices involved in the calibration, the larger the TC of PVG, forcing a shorter T_S, at fixed V_{pp}. Conversely, the minimum value of V_{REF} always corresponds to the minimum I_{DD}. Nonetheless, both values can achieve the I_{DD} lower boundary, for different values of D_T. For a broader comprehension of the potential of this approach, Fig. 17 also includes the ranges of temperature derivative vs time of different application domains [27]–[31]. In domains with low D_T, the current consumption can be always pushed at the minimum, thanks to limited number of re-calibrations per second required. Nonetheless, the BC-PVR achieves remarkable I_{DD} performance, for all the V_{REF} values, in all the considered application domains. Fig. 18 shows the average I_{DD} in the two phases of the main control period, vs. the temperature. I_{DD-s} is the contribution in the sleep phase, ascribed to the always-on blocks and the leakage current, whereas I_{DD-rc} is dominated by the analog and digital blocks executing the re-calibration procedure. In this measurement $T_S = 1$, and the overall current consumption almost overlaps the I_{DD} in the sleep phase. The maximum temperature corresponds to the maximum I_{DD}. This is mainly due to the increase of the leakage current in both the analog and digital sections. Fig. 18 also shows the ratio of the measured BC-PVR I_{DD} on the current of the bandgap included in the architecture $R_I \equiv I_{DD}/I_{BG}$. On the entire temperature range, the system current consumption represents a minimal

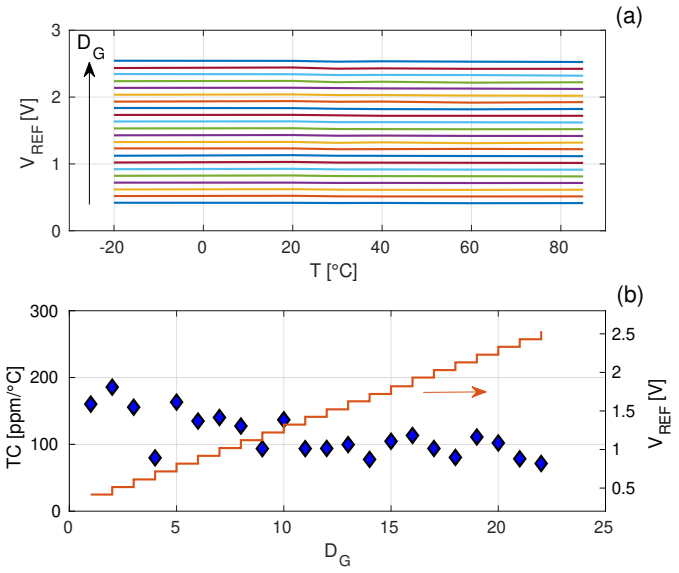

Fig. 19. (a) V_{REF} over the temperature range for all the available D_G levels; (b) temperature coefficient (diamonds, left y-axis) and V_{REF} at 30 °C (stairstep graph, right y-axis) vs. D_G.

fraction of the current consumption of the bandgap circuit from which derives. The measured power consumption at room temperature of the circuits composing the PVR are reported in Tab. III. The calibrated V_{REF} values over temperature, for all the D_{CAL} codes, are shown in Fig. 19(a). The PVR output can be programmed from 0.42 to 2.52 V, with voltage steps of approximately 100 mV. Fig. 19(b) reports the TC of each calibration code, with an average value $TC_{avg} = 113$ ppm/°C. The increase of TC with respect to the bandgap can be mainly ascribed to the temperature variability of V_{OS-PGA} and V_{OS-C} in equation (17). The spectra of the noise voltage at the reference output, measured with a SR785 Dynamic Signal Analyzer, are plotted in Fig. 20, with V_{REF} set to 0.42, 1.32, and 2.22 V. The rms noise, obtained with integration over the 10 Hz-to-1 kHz frequency band, is 83, 178, and 420 μV for the low, intermediate, and high V_{REF} values, respectively. The noise values reported in Fig. 20 are partially increased by the 50-Hz harmonics coupled to the PVG output.

In Table IV, the BC-PVR described in this paper is compared with the previously reported PVRs. The BC-PVR achieves the largest range of programmability in literature, which allows its full exploitation in power management of SoCs, for reducing power consumption both in analog and digital domains. This feature partially penalizes the area, since the PVG, the

TABLE III
POWER CONSUMPTION OF PVR CIRCUITS

Block	I_{DD} **[nA]**	V_{DD} **[V]**
Bandgap	420	3.2
PGA	250	3.2
Comparator	230	3.2
RTC	1.8	1.2
Oscillator	35	1.2

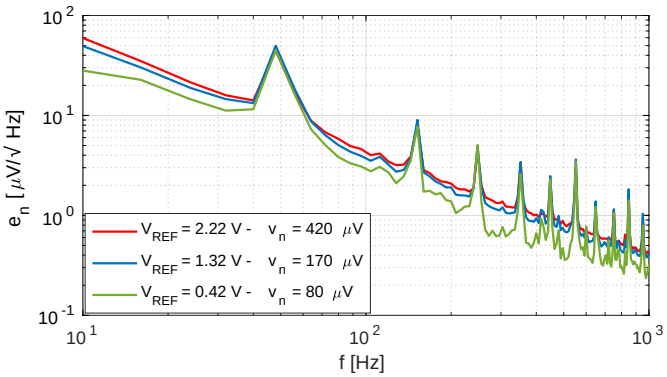

Fig. 20. BC-PVR output noise spectrum at V_{REF} = 0.42 V, 1.32 V, and 2.22 V.

memory, and transcoder physical dimensions are related to the temperature and programming ranges, and to the reference accuracy. However, our system shows large flexibility, and it can be designed with more relaxed specifications, to limit the occupied area. Additionally, the performance of the BC-PVR are obtained irrespective of the bandgap topology which can be optimized not only for the best accuracy and TC, but also for the minimum area. To the best of authors' knowledge, the proposed system is the first, complete mixed-signal implementation of a programmable voltage reference, reported in literature. It integrates on-chip the digital control and the clock generation circuits, which also represent a significant fraction of the area breakdown. For example, the floating gate references in [9] and [10] report the smallest areas, but both systems do not include any circuit for the necessary writing phase. The BC-PVR exhibits the smallest current consumption after the leakage-based PVR in [7], which, however, provides a small programmability range. Moreover, the reference value of this architecture is inherently below the voltage of the original sub-bandgap, thereby preventing its exploitation for power consumption reduction in SoCs, without additional circuits. In literature, the minimum I_{DD} reported for the FG-PVR is approximately two orders of magnitude higher than our programmable reference. No SC-PVRs with current consumption in the same range are available in literature, even if the optimization proposed in [15] allows a reduction of I_{DD}. The SC-PVR in [14] includes offset cancellation to obtain the best average TC among the state-of-the-art PVR. The proposed BC-PVR shows a competitive temperature coefficient. This performance can be improved with the inclusion in the analog section of offset cancellation techniques, such as auto-zero or correlated double sampling, at limited area and energy costs.

VI. CONCLUSION

This paper has presented a novel architecture for generation of an ultra low-power programmable voltage reference. The duty cycle-based BC-PVR is designed to be integrated in the power management of power-constrained electronic systems. Our mixed-signal architecture aims to exploit the small values of temperature derivative vs time of many application domains to minimize the system current consumption. Implemented in TSMC 55-nm CMOS technology node, the BC-PVR achieves

TABLE IV
STATE-OF-THE-ART PROGRAMMABLE VOLTAGE REFERENCES

	[7] 2019	[9] 2013	[10] 2008	[14] 2017	This work 2022
Tech. node	250 nm	500 nm	350 nm	180 nm	55 nm
Architecture	CT-PVR	FG-PVR	FG-PVR	SC-PVR	BC-PVR
V_{DD} [V]	3.5	1.8−4	2.5−3.8	3.6	2.7−3.6
Prog. Range [V]	0.08−0.41	0.6−1.4	0.1−0.5	1.25−2.88	0.42−2.52
Number of levels	64	NA	5	3	22
T. Range [°C]	-20−60	-30−120	-60−140	5−85	-20−85
TC_{avg} [ppm/°C]	85	35	141	30	113
Ref. Noise [$\mu V/\sqrt{Hz}$]	NA	NA	NA	2.6@10Hz	3.5@100Hz
I_{DD} [nA]	0.6	1000	5000	50000	7 @T_s=4s
Measured Samples	1	5	1	12	9
PVR Area [mm^2]	0.086	0.052	0.0022	0.09	0.28

in measurements an ultra low I_{DD} of 7 nA, for D_T below 0.017 °C/s. The large flexibility of the BC-PVR has allowed to achieve the largest reported programming reference range, over the temperature range [-20 , 85] °C.

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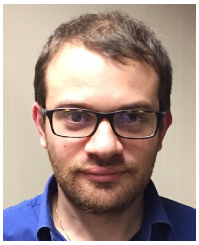

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