A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply

A 10mA LDO with 16nA-IQ and operating from 800 mV supply

Nicola Adorni, Stefano Stanzione, and Andrea Boni

***Abstract*—A low dropout regulator (LDO) with a quiescent current in the tens of nA range and operating from 800 mV supply is proposed. A rail-to-rail buffer with zero I/O voltage shift and based on the differential flipped voltage follower is used for combined gate and bulk driving of the output device. Therefore, bulk modulation with forward-body bias is implemented without any additional amplifier. The proposed buffer is a crucial block for the sub-1 V supply and for limiting the contribution of the output device to the quiescent current. The error amplifier is adaptively biased with a bias shaper block, which implements a current limiting at high loads and a linear dependence on the output current at moderate loads. The feedback signal for the bias control is the output of the amplifier instead of the gate voltage of the pass device, thus combining a nA bias at light load with the ability to follow a fast output current transient. Finally, a corner-tracking load is used to set the bias current of the output device to the minimum value at the target stability margin, over the temperature and process parameters space.**

The LDO was implemented in a 55 nm CMOS technology. The measured quiescent current is 16 nA, with a minimum Power Supply Rejection of 42.7 dB up to 50 kHz and a maximum load current of 10 mA. In order to compare the transient behavior of state-of-the-art designs, a modified figure-of-merit is proposed, taking into account the penalty caused by the low supply.

***Index Terms*— Low dropout regulators, CMOS LDO, Adaptive bias, Bulk modulation, Forward body-bias, Rail-to-Rail buffer, Low-quiescent current, Low-voltage, Tracking compensation.**

I. Introduction

Battery-powered devices for Internet of Things (IoT) applications, remote sensing, and implantable or wearable biomedical equipment require extremely efficient power management circuits for extending the battery life or eventually enabling autonomous operation with energy harvesting [1], [2].

For power saving reasons, those devices generally operate in duty cycle mode, hence periodically switching from standby to the on-state. Additionally, in recent years, a number of electronic systems consuming a few µA have been realized, pushing the power management blocks to consume a negligible fraction of the total system consumption. A logical consequence is that power management circuits must be able to operate at a very low output current, maintaining a safe stability margin of the involved feedback loops and high current efficiency. Therefore, a low quiescent current (I_Q) in the hundreds nA is required.

An additional requirement is to have a fast transient performance, capable to cope with the turn-on of load circuits recovering from the sleep mode. Furthermore, the low-voltage operation is becoming a mandatory feature of power management circuits. A trend of reduction of the load circuits voltage supply is forced by the need for consuming less power [3]. It is important to note that this trend is valid also for analog circuits. However, sensitive analog circuits require low-dropout regulators (LDO), which provide a stable supply voltage from a higher, unregulated or dirty, input [4]. LDOs are efficient only if the input voltage is close to the output voltage. This means that also such LDO will need to be correctly operating at very low supply voltages (under 1 V).

An additional feature that is often overlooked is the kickback noise related to a wide and fast transient of the load current. Indeed, in ultra-low-power designs the voltage reference circuit, providing the set-point for the regulation of the supply voltage, is usually unbuffered, thus extremely

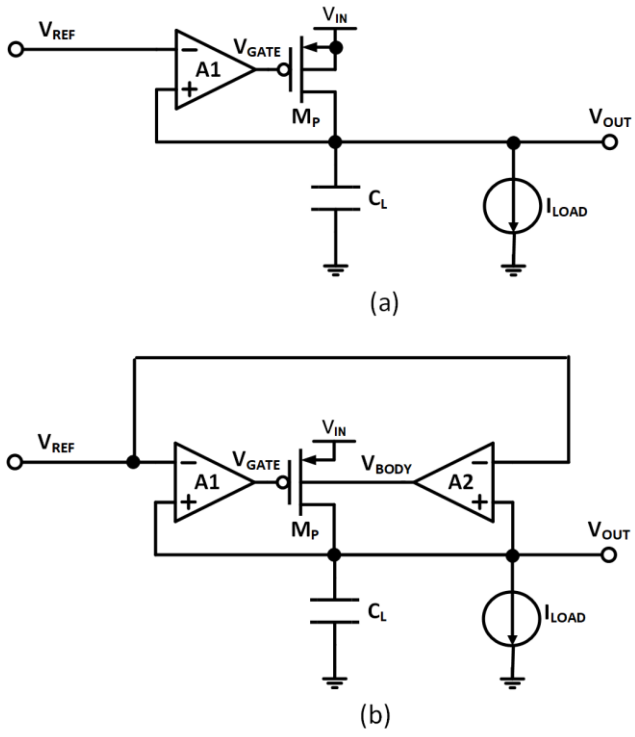

Fig. 1. Black-box schematic of LDO with unity gain feedback: (a) without body bias control and (b) with bulk-modulation.

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exposed to cross-talk, coupled to its output. A possible attenuation of this problem consists in integrating a large decoupling capacitor, but this implies an excessive Silicon area.

A black-box schematic of a generic LDO with unity gain feedback is reported in Fig. 1(a). A critical design aspect is the stability margin, which is severely affected by the load capacitance of the error amplifier A1, due to the gate of the pass device, M_P. Adequate compensation is either achieved by means of a large off-chip or an internal capacitor or both, while a buffer with a low output impedance is often introduced [5], [6] between the amplifier and the pass device.

Other relevant specifications of this circuit are the load and the line regulation. The former is a relevant parameter if the load current undergoes large variations because of the activity of the logic circuits and the periodic change of state of the wireless device. The latter is a crucial parameter for maintaining the regulated supply during almost all the battery discharge or with an energy harvesting source.

The above requirements raise several design problems that were addressed with various approaches in state-of-the-art designs reported in the literature. In [7] the bulk voltage of the output transistor is controlled by a separate feedback loop to improve the load and line regulation together with the stability margin. The modification of the basic architecture is shown in Fig. 1(b), where an additional amplifier, featuring a moderate voltage gain and a large bandwidth, is used for driving the bulk of the pass device. Nevertheless, this amplifier increases the quiescent current of the regulator. In [8] the forward body bias (FBB) was implemented for the output device to reduce the gate area and improve the regulation characteristics. An additional circuit, not reported in that paper, is required, thus leading to additional power consumption. Furthermore, the extensive usage of cascoding in the error amplifier severely affects the minimum input voltage that is indeed limited to 2.8 V.

In order to strongly reduce the quiescent current, in particular with a light load, adaptive bias was proposed for the error amplifier and the buffer [5], [6], [9]. In [5] a minimum quiescent current as low as 0.9 μA was achieved by making the bias current of the single-stage amplifier dependent on the gate voltage of the pass device. This solution may suffer from a slow transient in the case of a positive step of the load current, because of the large gate capacitance of that device. This problem was avoided with an enhanced current mirror buffer. The limits of this implementation are twofold: the quiescent current is not upper limited by design and the output buffer does not exhibit a rail-to-rail output. The former characteristic is prone to cause an excessive kickback noise at the reference input. The latter limits the maximum source-gate voltage of the pass device. In [6] an impressive transient time was achieved by means of a high-speed super current mirror, which drives the pass device and controls the adaptive bias. However, the added complexity of the buffer design, based on three branches, leads to a minimum I_Q well above 1 μA.

In [10] a cap-less LDO (i.e. without off-chip compensation capacitance) featuring 100 nA I_Q at 1 V input and with a minimum 100 nA load is presented. Besides the typical adaptive bias circuit driven by the gate voltage of the pass device, a dynamic bias current generator is added. The drop-out voltage is monitored and used to enable the additional bias current. Therefore, the I_Q is expected to strongly depend on the unregulated input voltage.

This regulator is based on the flipped-voltage-follower (FVF) topology with a folded-cascode gain stage [11]. In such LDOs the pass device is embedded in the FVF and it corresponds to the upper PMOS in the common-source configuration [12]. The gain provided by the folded-cascode stage allows removing the error amplifier, with some power saving, at the cost of a worse Power Supply Rejection (PSR). Moreover, it is worth to notice that cap-less LDOs usually exhibit larger under/overshoot in the presence of a fast transition time of the load current.

Furthermore, in [13] an LDO design featuring 1 μA minimum I_Q is reported. The regulator is based on an NMOS output device, which hence requires an internal charge pump for achieving a similar drop-out than PMOS-based regulators. The complexity of the circuit generating the adaptive bias and the multi-branch buffer severely limit the scaling of the quiescent current, that can be hardly reduced to hundreds of nA. Furthermore, the minimum input voltage is limited to 1.5 V, and high-voltage devices (7 V) are required.

A different approach is proposed in [14] where the power efficiency of the LDO is maximized at high load by keeping the minimum drop-out as low as 50 mV. This was achieved with a self-supplied error amplifier that limits the PSR degradation. However, the relatively large I_Q makes this design not suitable for duty-cycled systems, where the regulator works for most of the time in light-load conditions.

Extending the survey to low-I_Q LDOs available on the market, a quiescent current as low as 500 nA is achieved by [15], but the minimum input voltage is 2.2 V and the PSR in the 0-50 kHz range is very low, i.e. lower than 10 dB at 1mA load.

Therefore, on the basis of the survey of state-of-the-art designs reported in the literature, and on the authors' knowledge, no LDO design achieving all the required specs for pushing the performance of low-power devices, was reported.

The design target of the LDO discussed in the paper was to simultaneously achieve a quiescent current of few tens of nA, a sub-1 V minimum input voltage, a strong line regulation, and a minimum PSR of about 40 dB up to few tens of kHz. The targets were achieved by extending the concept of the adaptive bias to all the involved blocks, thus leading to a super-adaptive LDO, and by an innovative implementation of the concurrent bulk-modulation and FBB of the pass device. Unlike the reported implementations, the bias current of the error amplifier is almost linearly dependent on the load current and it is upper limited by design, leading to an almost

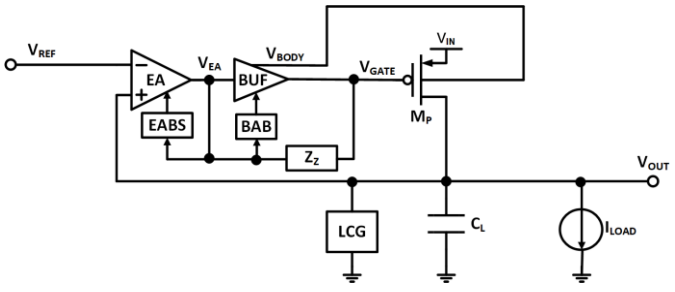

Fig. 2. Black box schematic of the proposed LDO.

constant gain of the error amplifier over all the current range (affecting all LDO parameters, both static and dynamic). Furthermore, the kickback noise problem is mitigated because of the smaller voltage swing of the internal nodes of the amplifiers. In addition, a fast transient is achieved by means of a modified driving concept with respect to the conventional adaptive bias solutions.

A second relevant improvement of the proposed design is the rail-to-rail buffer that exhibits almost 0 V input-output (I/O) shift and it is based on a differential-flipped voltage follower (DFVF) [12], This circuit, never used as a buffer in LDO designs, drives both the gate and the bulk terminal of the output device. This offers a relevant power saving since the auxiliary amplifier, used for bulk modulation as in [7], is removed.

Finally, for loop stability reasons, a minimum bias current must be provided to the pass device in the case of zero load current. To this aim, a corner-tracking output bias generator was implemented. This is a specific feature of the proposed design, which allows adapting the minimum current of the pass device to its leakage, over the temperature range and process corners.

It is worth to notice that all the implemented circuit solutions are compatible with a low input voltage. Indeed, the proposed LDO accepts an unregulated input supply from 1.4 V down to 0.8 V. To the authors' knowledge this is the first reported regulator featuring a sub-1 V input with a quiescent current in the tens nA range. The LDO was implemented in a bulk 55 nm CMOS technology. The expected performance was validated by the experimental characterization of the silicon samples.

The paper is organized as follows: the proposed architecture is discussed in Section II, the circuit implementation is described in Section III together with the circuit analysis, whereas in Section IV the implemented frequency compensation is discussed. Finally, the measurement results and a comparison with the state-of-the-art designs are reported in Section V.

II. Proposed Architecture

The black-box schematic of the proposed LDO, based on the common-source configuration with a PMOS as the pass device, is shown in Fig. 2. If the output voltage must be set to a higher value than the reference voltage, a resistive voltage divider is required at the LDO output. Since those resistors set the minimum current of the pass device with open-load, a unity feedback factor was preferred.

The main blocks in Fig. 2 are a rail-to-rail error amplifier (EA), a unity-gain buffer (BUF), and a corner-tracking Load Current Generator for M_P (LCG). Unlike the other reported designs, such as shown in Fig. 1(b), the auxiliary amplifier A2 is not required in the proposed design.

The bias generator LCG sets the bias current of the pass device to the minimum value, corresponding to its leakage current. This proposed bias technique is mandatory to minimize the contribution of the output device to the LDO quiescent current. The Error Amplifier Bias Shaper block (EABS), sets the bias current of the error amplifier depending on the load current I_{LOAD}. The output of the error amplifier, V_{EA}, is used to sense the load current, instead of the gate voltage, V_{GATE}, [5], [6], [9], [13]. This proposed solution strongly improves the transient response of the adaptive bias generator, avoiding the detrimental effect of the buffer delay. The precision of the load-dependent bias control is not impaired, thanks to the proposed buffer that exhibits almost no I/O voltage shift. Since the load current modulates the transconductance and the output resistance of M_P, achieving an adequate stability margin over a wide range of load current is a challenging task. To this aim, a combination of an off-chip capacitor (C_L) and an internal R-C network for implementing the tracking-zero technique (Z_Z) was used. As known in the literature, and discussed in Section IV, the resistive part of Z_Z tracks the drain-source resistance of M_P, hence maintaining an adequate stability margin over the design space.

III. Circuit Implementation

A simplified schematic of the proposed LDO is shown in Fig. 3. The error amplifier (M_1-M_{10}), EA, has a relevant impact on the PSR and the output voltage static errors. For this reason, it must exhibit an adequate DC gain and bandwidth over the supply and load current range. The

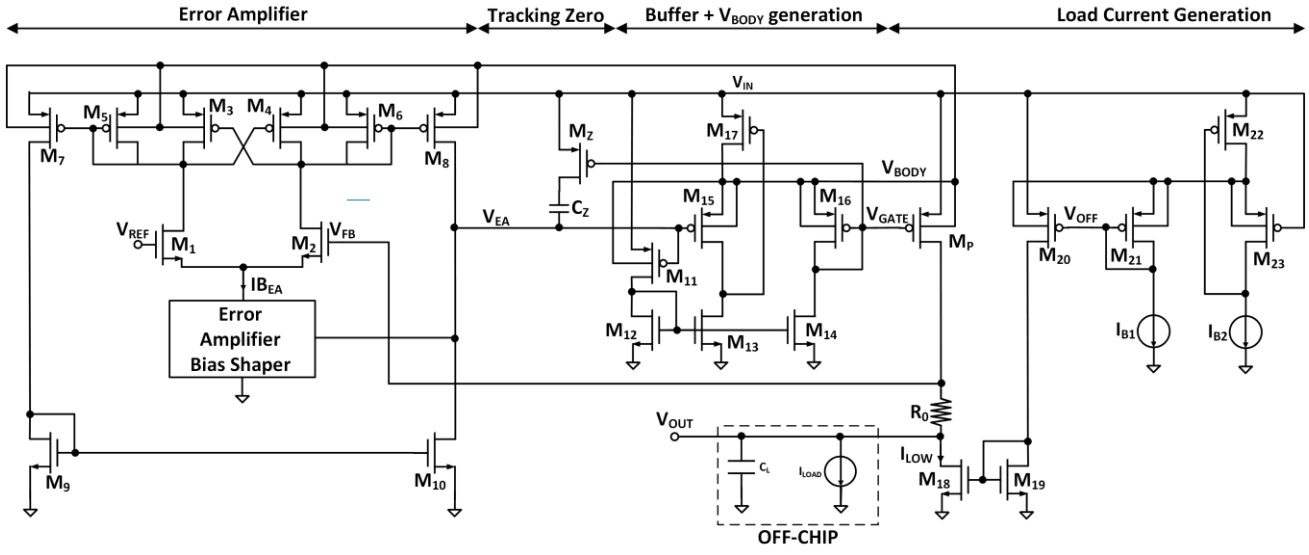

Fig. 3. Simplified circuit schematic of the low I_Q and low voltage LDO.

requirement for a sub-1 V operation calls for alternative design strategies to cascoding. Therefore, the output stage of the amplifier (M_8-M_{10}) is implemented as a rail-to-rail complementary common-source, whereas the local positive feedback with a cross-coupled PMOS load (M_3-M_4) boosts the DC gain of the first stage, without affecting the output range [16], [17]. Notice that bias currents I_{B1}, I_{B2} and also I_{BL} and I_{BH} (in Fig. 5) are all generated by mirroring an input current reference provided externally.

The transfer function of the error amplifier exhibits two non-dominant poles:

$$p_{A1} = -\frac{g_{m5} - g_{m3}}{C_{gs5} + C_{gs3}} \quad (1)$$

$$p_{A2} = -\frac{g_{m9}}{C_{gs9} + C_{gs10}} \quad (2)$$

where $C_{gs<i>}$ and $g_{m<i>}$ are the gate-source capacitance and small-signal transconductance of $M_{<i>}$, and any random mismatch has been neglected. The pole p_{A1} is pushed to a higher frequency, without affecting the voltage gain of EA, by reducing the width of M_3-M_6, at a fixed current, provided that the involved devices are maintained in Weak-Inversion (W.I.). However, this lowers the DC voltage at the drain of M_1-M_2, thus reducing the common-mode input range of the error amplifier. To relax the latter constraint, the FBB is exploited by sharing the same body bias with the pass device. It is worth to notice that the stability constraints of the LDO dictate that such non-dominant poles are always well above the unity-gain frequency (UGF) of the LDO loop gain, as discussed in Section IV.

A. Buffer with Adaptive Bias and Embedded Body Bias Generation

If the buffer exhibits a significant I/O voltage shift, the rail-to-rail output range of the error amplifier is underused. For the same reason, also the buffer must feature an almost rail-to-rail behavior and properly operate with a sub-1 V supply voltage. To this aim, a Differential Flipped-Voltage-Follower (DFVF) has been used, M_{11}-M_{16} [12]. This circuit is based on an input side (M_{13}, M_{15}, M_{17}) with negative feedback through device M_{17} for achieving a low output resistance at the source of M_{15} and M_{16}. By means of the output branch (M_{14}, M_{16}) an almost zero voltage shift is obtained, at the cost of increased output resistance of the buffer, R_{ob}, with respect to the simple flipped-voltage follower (FVF):

$$R_{ob} \approx \frac{1}{g_{m17}A_{15}} + \frac{1}{g_{m16}} \quad (3)$$

where $A_{15} = g_{m15} \cdot r_{ds15}$ is the intrinsic voltage gain of M_{15}, with r_{ds15} the drain-source small-signal resistance. The above equation is rewritten considering that the involved devices are sized for weak inversion (W.I.) bias, up to the maximum I_{LOAD}:

$$R_{ob} \approx \frac{n_p \cdot v_{th}}{I_{D16}} \quad (4)$$

where $I_{D<i>}$ is the drain current of $M_{<i>}$, v_{th} is the thermal voltage, n_p is the slope factor of PMOS devices, and $A_{15} >> 1$ has been assumed. The contribution of the input branch, i.e. first term in (3), is negligible because of the feedback, hence limiting the current consumption, whereas the bias current of the output branch, I_{D16}, must be set accordingly to the required value of R_{ob}. As discussed in Section IV, a higher R_{ob} does not affect the stability margin with a light load, whereas R_{ob} must decrease at high output currents. This feature is achieved with the proposed adaptively biased DFVF (ABDFVF), where the replica of the pass device, M_{11}, sets the bias currents of the buffer. Therefore, the bandwidth of the buffer at light load condition is expected to be extremely limited. Hence, a relevant delay in the low-to-high load transient is expected if V_{GATE} is used to control the gate of the replica device, as in conventional implementations. On the contrary, in the proposed adaptive bias, the output of the error amplifier, V_{EA}, is used to drive M_{11}, instead. This solution provides clear benefits to the LDO step response.

A relevant advantage of this buffer with respect to other reported LDOs is the generation of the body bias (V_{BODY}) of the output device without any additional amplifier and, therefore, any further contribution to the quiescent current. To the authors' knowledge, this is the first reported low-I_Q LDO with a DFVF used for both gate driving and bulk modulation/bias. By construction, the source-bulk voltage of M_P, V_{SBP}, is:

$$V_{SBP} = V_{SGP} - V_{SG16} \quad (5)$$

Where $V_{SG<i>}$ is the source-gate voltage of $M_{<i>}$ device. Since both M_P ad M_{16} are biased in W.I., the following expression for V_{SBP} is obtained:

$$V_{SBP} = n_p v_{th} \ln\left(\frac{I_{LOAD}\, I_{S16}}{I_{D16}\, I_{SP}}\right) \quad (6)$$

where $I_{S<i>}$ is

$$I_{S<i>} = v_{th}^2 \cdot \mu_p \cdot C_d \left(\frac{W}{L}\right)_{M<i>} \cdot exp\left(\frac{V_{T<i>}}{n_p\, v_{th}}\right) \quad (7)$$

with μ_p being the hole mobility, C_d the depletion capacitance, and $V_{T<i>}$ the threshold voltage of PMOS $M_{<i>}$ [18]. Since the bias currents of M_{16} and M_P are linked through M_{11} and the mirror M_{12}-M_{13}, (6) is rewritten as:

$$V_{SBP} = n_p\, v_{th} \ln\left(\frac{K_{16-11}}{K_{14-12}} \cdot \frac{V_{T16}}{V_{TP}}\right) + (V_{EA} - V_{GATE}) \quad (8)$$

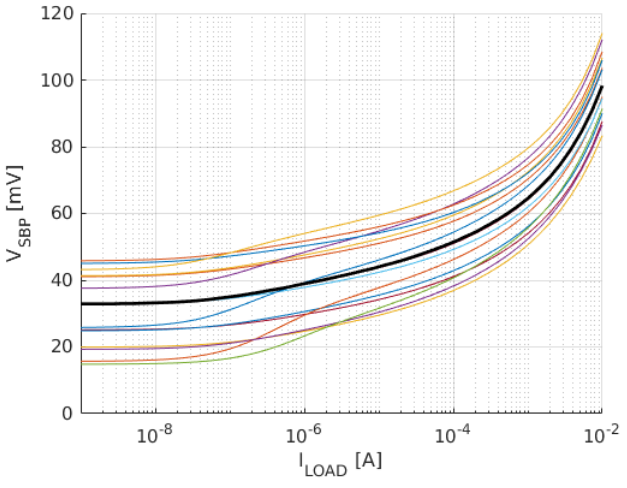

Fig. 4. Simulated source-bulk voltage of M_P over process corner, temperature, and I_{LOAD} at 0.8 V input. The thick-black line corresponds to the typical corner.

where $K_{16\text{-}11}$ and $K_{14\text{-}12}$ are the ratios between the W/L, of M_{16}-M_{11}, and M_{14}-M_{12}, respectively, and the effect of the different body bias of M_P and M_{16} has been taken into account. If the residual I/O shift of the buffer is neglected together with the difference of the thresholds, the body-to-source diode voltage of M_P depends only on the ratio between geometrical parameters of MOS devices. Therefore, the proposed body bias generator exhibits relevant robustness against process corner, temperature, and supply voltage.

The simulated value of V_{SBP} as a function of the load current is shown in the graph of Fig. 4. At light load, the spread of V_{SBP} over corners and temperature is within +/- 15 mV with respect to the typical case. This variation is mainly due to the residual voltage shift of the buffer according to (8). Furthermore, the dependence on I_{LOAD} is negligible up to tens of μA, whereas, at higher currents, the source-bulk voltage progressively increases since M_P leaves the W.I. to enter in the moderate (M.I.) and, strong inversion (S.I.) region. Indeed, if M_P is assumed in S.I. with M_{16} in W.I., the value of V_{SBP} is roughly approximated by the overdrive voltage of the output transistor:

$$V_{SBP} \approx V_{SGP} + V_{TP} \tag{9}$$

where V_{SG16} has been assumed approximately equal to $-V_{TP}$. It is worth to notice that the value of V_{SB} is independent of the input voltage, at a fixed value of maximum I_{LOAD}. Therefore, if M_P is sized for the maximum load current at the 0.8 V input and considering a V_{TP} of about -0.5 V, we can conclude that V_{SBP} is always below the diode threshold. However, from (9) it is evident that using the ABDFVF buffer (with combined gate and bulk driving) at a sub-1 V supply severely limits the maximum FBB that can be achieved, as shown in Fig. 4. Therefore, the benefit in terms of width reduction for M_P, thanks to the body effect [18], is lower than in other designs where a dedicated circuit is used for the body bias. In the present design, the FBB provides a 20% reduction of the M_P area, with no additional quiescent current. Hence, it is evident that the area reduction thanks to FBB is here constrained by the design optimization for the lowest I_Q and by the low supply. Finally, it is worth to notice that the benefits of the bulk modulation extend to the improved load and line regulation [7].

The lower bound of the output range of the buffer is set by the saturation limit of M_{14}:

$$V_{GATEmin} = V_{DSsat14} \approx 4 \cdot v_{th} \tag{10}$$

where $V_{DSsat14}$ is the drain-source saturation voltage of M_{14}. It is worth to notice that the adaptive bias in the DFVF buffer introduces a potential risk of stability margin degradation at high-load conditions. This is due to the increased value of V_{SG17}, which reduces the drain-source voltage of M_{13}. If the saturation limit of M_{13} is exceeded downwards, (3) loses its validity, since the voltage gain of M_{15} can no longer be approximated with its intrinsic gain. Hence, the value of R_{ob} increases and the associated pole in the closed-loop transfer function is moved at a lower frequency, thus leading to a smaller phase margin or to the instability of the regulator. The issue is discussed in Section IV. Therefore, the proposed ABDFVF has to be sized for maintaining M_{13} in weak inversion and in saturation over the whole corner space.

With regard to the upper limit of the output range, it is interesting to note that it is extended up to V_{IN} by means of the implemented adaptive bias. Indeed, with a very light load, V_{GATE} is forced to a high value to reduce the source-gate voltage of M_P, thus driving M_{17} in the triode region. Hence, the gate voltage of M_{17} decreases to maintain the same current being set by M_{13} and M_{14}. However, thanks to the adaptive bias, the current of such devices are reduced in the sub-nA range, thus limiting the variation of V_{SG17}, from the medium to the light load condition and keeping M_{13} in saturation. This condition is mandatory to maintain the current ratio I_{D14}/I_{D13} almost equal to the design value and thus to keep a unitary voltage gain and almost zero DC voltage shift. Furthermore, the adaptive bias allows achieving $V_{SG16} << -V_{T16}$ at light load and thus an almost rail-to-rail output capability.

$$V_{GATEmax} \approx V_{IN} \tag{11}$$

The only drawback of V_{GATE} pushed close to V_{IN} is that A_{15} in (3) is strongly reduced, leading to an increased value of R_{ob}. However, this does not impair the stability margin, because of the dependence of the dominant pole with the load current.

B. Adaptive Bias generators for the Error Amplifier

In order to achieve tens nA quiescent current, the error amplifier is adaptively biased, on the basis of the load current, as for other reported low-I_Q implementations. This solution, however, raises a few design problems. Indeed, it is hard to maintain a constant voltage gain over a wide range of bias current, leading to the degradation of DC and AC system parameters. Furthermore, a large variation of the amplifier bias current causes kickback noise at the reference input.

Such problems have been successfully addressed by means of the Error Amplifier Bias Shaper (EABS), shown in the simplified schematic of Fig. 5(a). The input of the bias block is the drain current of M_{29}, which mirrors the load current with a scaling factor equal to N. Unlike to conventional adaptive bias circuits [5], the gate of the replica device, M_{29}, is driven by the error amplifier itself, instead of the buffer, thus greatly improving the transient behavior of the bias circuit in the case of a low-to-high load current step. In addition, the load-dependent bias current is here limited by design, thus maintaining a high PSR at high load condition.

As shown in Fig. 5b, the bias current, IB_{EA}, settles to the upper bound I_{BH} at I_{LOAD} higher than I_{LTH}. This occurs when the drain current of M_{26} is higher than the saturation current of M_{30}, i.e. I_{D30sat}, and thus the mirror M_{24}-M_{25} is turned on:

$$I_{BH} = k \cdot I_{D30sat} + I_{BL} \tag{12}$$

where k is the ratio between the aspect ratio of M_{25} and M_{24}, and M_{27} and M_{26}, M_{28}. The higher threshold for I_{LOAD} is:

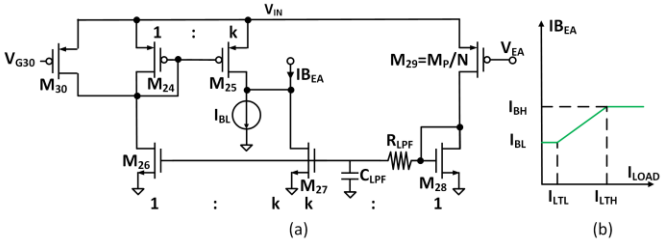

Fig. 5 (a) Error Amplifier Bias Shaper (EABS) simplified schematic and (b) I/O characteristic as function of the LDO load current.

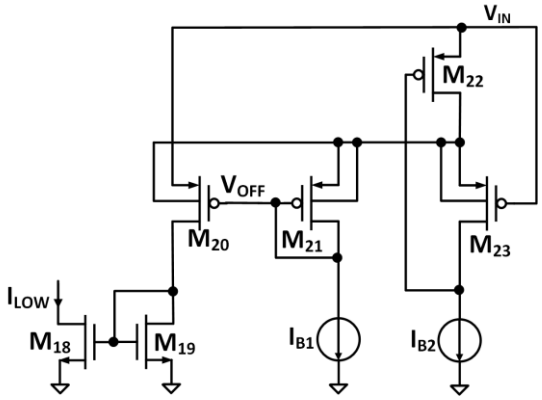

Fig. 6 Corner-tracking load current generator: simplified schematic.

$$I_{LTH} = N \cdot I_{D30sat} \tag{13}$$

With a moderate load, i.e. I_{LOAD} lower than I_{LTH}, the bias current depends almost linearly on the load current:

$$IB_{EA} = \frac{k}{N} \cdot I_{LOAD} + I_{BL} \tag{14}$$

Finally, with a very light load, IB_{EA} reaches a lower plateau at I_{BL}. This occurs for I_{LOAD} much lower than (I_{BL} ·N / k). In that condition, all devices but the I_{BL} current generator are off, hence limiting the current consumption of the bias shaper to the leakage currents of the PMOS devices in Fig. 5(a).

In our design I_{BL} was set to 10 nA and I_{D30sat} to 16 nA with k=8 and N=3960, leading to I_{BL} and I_{BH} in Fig. 5(b) equal to 10 nA and 140 nA, respectively.

The low-pass filter R_{LPF}-C_{LPF} (65 kΩ-370 fF) attenuates the kickback noise at the input reference pin and improves the transient behavior at the high-to-low load variation. Indeed in presence of a fast increase of the load current, the filter limits the slew-rate of the EA bias current and, consequently, of the voltage of shared sources of M_1 and M_2, and of the drain of M5. It is worth to notice that the proposed solution, with the adaptive biasing circuits driven by the EA output, maintains better transient performance than conventional solutions, even in the presence of the above filter. Indeed, the R-C time constant is much smaller than the equivalent time constant at the buffer output at light-load conditions, due to the high value of R_{ob} from (4).

In presence of a high-to-low load transition, without the added filter the bias current would be suddenly reduced, because of the fast adaptive loop. The consequent degradation of the transient behavior is here avoided thanks to the filter, which allows maintaining a relatively high bias current during the settling of the LDO output.

C. *Corner-tracking Load Current Generator*

The absence of the resistive voltage divider as the feedback circuit, requires a block providing the pass device with the bias current. The absolute minimum bias for M_P corresponds to its own leakage current. Indeed, if the overall load current is lower than the leakage, the LDO feedback loop is not able to control the output voltage. Since the leakage current exhibits a huge variation over the process and temperature design space, setting the load current to the maximum leakage would strongly worsen the overall quiescent current of the regulator in typical conditions. This design problem has been solved by means of the corner-tracking bias block, shown in Fig. 6 and connected to the LDO output, as in Fig. 3. This circuit implements a low-power replica of the DFVF buffer (M_{21}-M_{23}) without the adaptive bias feature and driving a scaled replica of the pass device, M_{20}. A constant bias (i.e. I_{B1} and I_{B2}) corresponding to the minimum bias current of the main ABDFVF is used here, with the input connected to the unregulated supply, V_{IN}. Therefore, the drain current of M_{20} is a scaled copy of the leakage current of the pass device, M_P. Finally, transistors M_{18}-M_{20} mirror to the output the generated corner-dependent load current I_{LOW}. It is worth to notice that this solution always provides the pass device with the minimum bias current, thus achieving the minimum overall quiescent current.

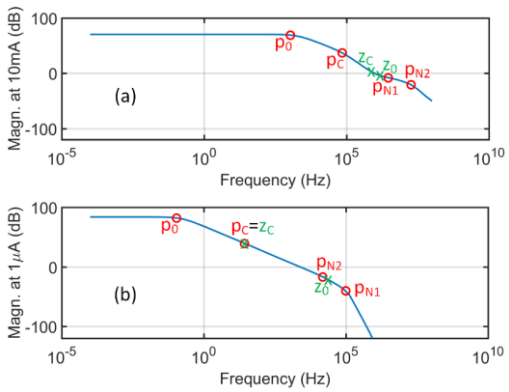

Fig. 7. Simulated loop-gain (module) of the LDO with unity feedback-factor: (a) high-load conditions and (b) light load with pole-zero cancellation.

IV. Frequency Compensation Strategy

Maintaining a suitable stability margin in a linear regulator is a critical design task if the load current exhibits a broad range, starting from the open-load condition. If an off-chip capacitor is used for stabilization, the dominant pole of the loop gain is due to that capacitance, while the second pole, being related to the gate capacitance of the pass device, usually occurs before the UGF of the loop-gain. A phase margin in excess of 45° can be achieved by means of a compensation zero within the unity-gain bandwidth, which is introduced by the effective series resistance (ESR) of the off-chip load capacitor [19]. Nevertheless, the tolerance affecting the ESR makes this technique almost useless if an adequate stability margin must be maintained at light load [20].

A better solution is to link the compensation zero to the UGF, which in turns depends on the load current, temperature and process parameters. This is achieved by means of a shunt R-C network, placed at the output of the error amplifier (Z_Z

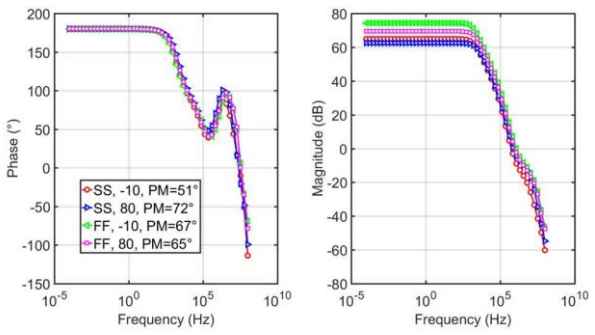

Fig. 8. Simulated loop gain at high-load condition over MOS corners and temperatures (-10 °C and 80 °C).

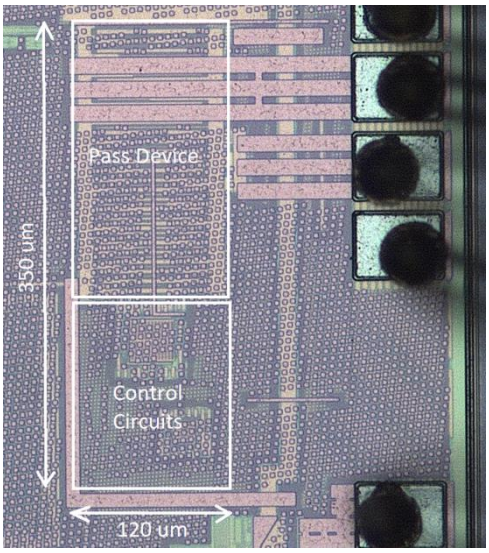

Fig. 9. Chip photograph.

in Fig. 2). The resistive part of Z_Z is linked to the drain-source resistance of M_P, which sets the value of the dominant pole [21]. As shown in Fig. 3 the compensation network is implemented with the on-chip capacitor, C_Z, and a transistor, M_Z, which is biased in the linear region and with the same gate-source voltage of M_P, Therefore, its drain-source resistance exhibits an inverse dependence on the load current, thus leading to a UGF-tracking zero. Even if this compensation technique is promising for improving the stability of ultra-low power LDOs, a buffer with a low output resistance is generally mandatory. As discussed in the previous section, the buffer can be a real bottleneck if the LDO must handle a sub-1 V unregulated supply. The required performance was achieved in the proposed design by a rail-to-rail DFVF buffer.

The approximate expressions of the most relevant poles and zeroes of the LDO loop gain are obtained by circuit analysis:

$$p_O \approx -\frac{1}{r_{dsP} \cdot C_L} \tag{15}$$

$$p_C \approx -\frac{1}{C_Z \cdot (R_{OA} + R_Z)} \tag{16}$$

$$p_{N1} \approx -\frac{R_Z^{-1} + R_{OA}^{-1}}{C_{IB}} \tag{17}$$

$$p_{N2} \approx -\frac{1}{R_{OB} \cdot C_{gsP}} \tag{18}$$

$$z_C = -\frac{1}{C_Z \cdot R_Z} \tag{19}$$

$$z_O = -\frac{1}{C_L \cdot (R_{ESR} + R_0)} \tag{20}$$

where r_{dsP} and C_{gsP} are the drain-source resistance and gate capacitance of M_P, C_{IB} and R_{OB} are the input capacitance and the output resistance of the buffer, ESR is the effective series resistance of capacitor C_L, R_Z is the drain-source resistance of M_Z, and R_{OA} is the output resistance of the Error Amplifier:

$$R_{OA} = \frac{1}{r_{ds10}^{-1} + r_{ds8}^{-1}} \tag{21}$$

It is worth to notice that the small-value on-chip resistor R_0, partially desensitizes the frequency of z_0 to ESR. In the analysis above, the pole due to the body driving by the DFVF was not considered. Indeed such pole is expected to be located at a higher frequency than p_{N2} since the equivalent resistance at the source of M_{15} is lower than R_{ob} and the well-to-substrate junction capacitance of the pass device is lower than its gate capacitance.

In Fig. 7(a) the plot of the LDO loop gain is shown for the case of high load current. If the current is progressively reduced, both the tracking zero (z_C) and p_{N1} move to lower frequencies with the dominant pole, p_0, because of the approximate inverse dependence of R_Z on I_{LOAD}. The behavior of p_C is quite different in the high-to-medium load current range since R_{OA} is much higher then R_Z and independent from I_{LOAD}, because of the current-limiting behavior of the EABS. Therefore, p_C is almost constant until, at light load, R_Z approaches R_{OA}. If the current is further decreased, both p_C and z_C exhibit almost the same dependence on R_Z and, hence, on I_{LOAD}, leading to a pole-zero cancellation, Fig. 7(b). Furthermore, because of the adaptive bias of the buffer, R_{OB} tracks I_{LOAD} and thus p_{N2} moves at lower frequencies with p_O.

The simulated loop gain of the LDO at the maximum load current and at the extreme MOS corners and temperatures (i.e. -10 °C and 80 °C) is shown in Fig. 8. The reduction of the stability margin at the slow and minimum temperature corner is mainly ascribed to M_{13} in the ABDFVF buffer that is pushed to the limit of the saturation region, thus affecting the value of R_{ob} as discussed in Section III.A.

A further benefit of the implemented compensation is a relevant improvement of the PSR. Indeed, any medium-to-high frequency ripple affecting the input supply is coupled to the gate through M_Z-C_Z and the buffer. Therefore, as long as the gain of the buffer is close to one, the source-gate voltage of the pass device is not affected by that ripple, leading to a high PSR.

V. Experimental Results

The chip has been fabricated in the TSMC 55nm CMOS process and the active area of the circuit is 0.042mm^2. A photograph of the die is shown in Fig. 9. The relatively large area is due to the design optimization for minimum I_Q and to the 0.8 V supply. Indeed, only thick-oxide (I/O) devices were

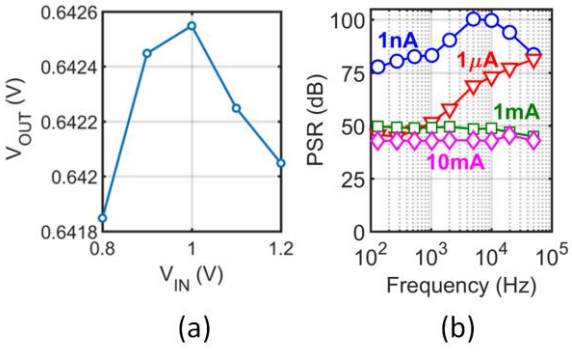

Fig. 10. (a) Measured line regulation at 100 µA load current and (b) PSR for V_{REF}=600 mV and V_{IN}=800 mV.

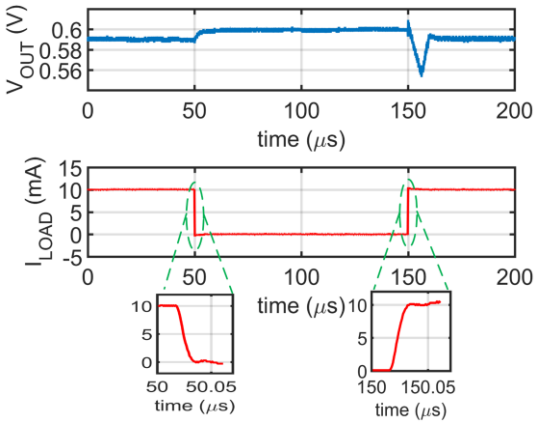

Fig. 11. Measured transient load regulation at V_{REF}=600mV and V_{IN}=800mV.

used due to their lower leakage current than core devices.

All the measurements have been performed with a load capacitor of 1 µF. As shown in Fig. 10(a), a good DC line regulation is insured at 600 mV voltage reference and 100 µA load current. Furthermore, the measured DC line regulation is 0.5 mV/V at V_{REF}=600 mV (supply varied from 0.8 V to 1.2 V). As shown in Fig. 10(b), the LDO PSR remains very high over a wide range of frequency and load currents. Indeed, even varying the load current 10^7 times (from 1nA to 10mA), the minimum PSR from DC to 50 kHz is 42.7 dB at 800 mV supply and V_{REF}=600 mV. At light load conditions the PSR increases of about 25 dB with frequency. This is due to the drain-source resistance of M_P that becomes very high at those load conditions. According to the model in [22] this resistance, combined with the load capacitance leads to a high-pass behavior in the low-frequency range.

In Fig. 11 the transient response of the proposed LDO is shown for a reference voltage of 600 mV and an input voltage of 800 mV. The current is changed from 10 mA to 100 µA and then to 10 mA again. The current rise and fall times are about 20 ns, as shown in the zooms at the bottom of Fig. 11. A voltage drop of 70 mV is measured, leading to a figure of merit FOM-t = $C_L I_Q \Delta V/\Delta I^2$ [23] of 11.4 ps.

The comparison with the state of art is shown in Table I.

The proposed LDO exhibits the lowest minimum supply voltage and quiescent current while being well aligned to other performance parameters shown in the literature. FOM-t is not the best if compared to other reported design, since [5], [6], [13] show better FOM-t. However, they all have larger voltage supplies and the regulator with the lowest supply voltage i.e. 1.05 V, among those three references, is the one with the highest FOM-t (10.66 ps) [6]. This is not happening by case, but due to the fact that, for operating the LDO with the same maximum current at low supply voltages, its pass device needs to be larger, leading to larger parasitic capacitance to drive and, hence, a worst FOM-t. This is an intrinsic weakness of this widely used parameter for comparing low-voltage LDO designs. For this reason, FOM-t is modified as FOM-tV for taking into account the gate capacitance penalty occurring with the scaling down of the supply voltage:

$$\text{FOM-tV} = \left(C_L \cdot I_Q \Delta V/\Delta I^2\right) \cdot (V_{IN}/1\,V)^2 \qquad (22)$$

Indeed, at high currents, the output device is biased in S.I. and, hence, the gate capacitance is inversely proportional to the square of the maximum overdrive of the pass device, i.e. $(V_{IN}+V_{TP})^2$, at a fixed value of maximum I_{LOAD}. Therefore, an accurate definition of the FOM-tV would require to multiply the FOM-t for $(V_{IN}+V_{TP})^2$, leading to an impractical figure-of-merit, since the value of V_{TP} is seldom reported. For this reason, the definition in (22) was preferred, even if the penalty caused by the lower supply is not completely de-embedded.

The scatter plots in Fig. 12 show a comparison with best-in-class low-I_Q LDOs in terms of FOM-tV, vs. I_Q and minimum PSR from DC to 50 kHz (PSR_{MIN}) vs. I_Q [2], [5], [6], [9], [10], [13], [15], [24]–[26]. The achieved FOM-tV is the lowest reported in the literature after [5] and [10]. It is worth to notice that [5] exhibits more than 10x quiescent current, whereas the outstanding performance of the cap-less LDO in [10] are achieved with a dynamic biasing approach, requiring calibration and causing a significant dependence of the quiescent current on the input voltage. Finally, the plot in

TABLE I
COMPARISON WITH STATE OF ART

	[5]	[6]	[7]	[24]	[15]	[13]	**This work**	**Unit**
Technology	180	350	130	N.A.	N.A.	250	55	**nm**
Minimum input voltage	1.4	1.05	1.2	2.3	3.5	1.5	0.8	**V**
Output voltage	1.2	0.9	1	1.8	3	1 - 3	0.6	**V**
Maximum load current	50	50	5	50	150	150	10	**mA**
DC Load regulation	0.14	0.06	N.A.	2.25	0.2	0.17	1.05	**mV/mA**
DC Line regulation	7.25	N.A.	N.A.	4.5	15	N.A.	0.5	**mV/V**
Active area	0.03	0.05	0.002	N.A.	N.A.	0.108	0.042	**mm^2**
Trans. Drop (ΔV_{OUT})	18	7	200	350	545	160	70	**mV**
Trans. Load Variation (ΔI_{LOAD})	50	50	5	50	10	150	10	**mA**
Load current edge time	10	10	200	1000	N.A.	10	20	**ns**
FOM-t	3.04	10.6	N.A.	490	4800	8.8	11.4	**ps**
FOM-tV	6.0	11.7	N.A.	2590	58800	19.8	7.3	**ps**
Load capacitor	0.47	1	N.A.	1	2.2	1	1	**µF**
Min. PSR from DC to 50 kHz	44	50	70	8	8	13	42.7	**dB**
Quiescent current	0.9	4.04	99	3 *	0.4 **	1.24	0.016	**µA**

* For fair comparison quiescent current is reduced of 1µA with respect to the reference, because it contains also a bandgap reference.
** For fair comparison quiescent current is reduced of 100nA with respect to the reference, because it contains also an ultra-low-power bandgap reference.

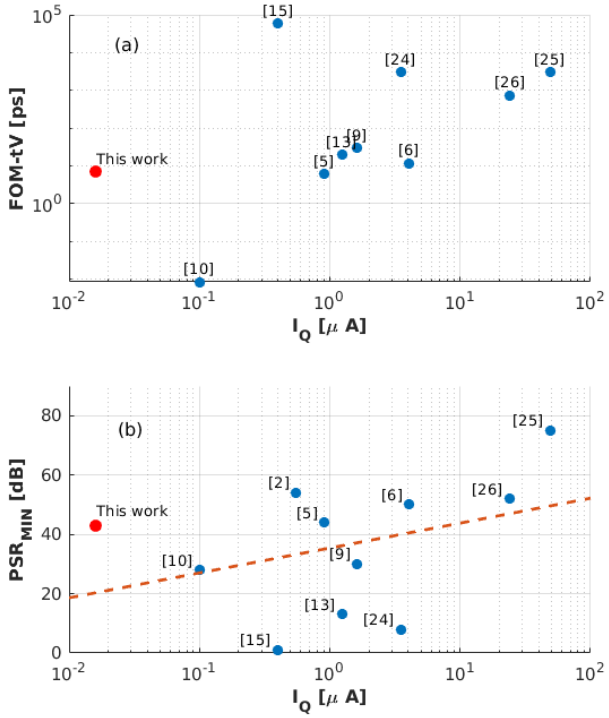

Fig. 12. Scatter plots comparing the proposed LDO with best-in-class low-power regulators. PSR_{MIN} is the minimum PSR over the 0-50 kHz range.

Fig. 12(b) shows that the achieved PSR is similar to that of other designs featuring two orders of magnitude higher I_Q.

VI. Conclusion

A low-drop-out regulator operating down to 0.8 V input with a quiescent current of 16 nA has been presented. This extremely low I_Q was achieved by extending the concept of adaptive bias to all the LDO blocks and by means of a corner-tracking bias generator for the output device. The transient behavior, line regulation, and PSR are not impaired by the low-I_Q thanks to a bias shaper, which limits by design the maximum step of the bias current and exhibits an almost linear dependence on the load current with moderate loads. Furthermore, the innovative driving concept for the adaptive bias generator provides relevant advantages for the transient behavior with a low-to-high step of the load current. A key block of the proposed design is the buffer, which is based on an adaptively biased DFVF, featuring zero DC voltage shift, rail-to-rail behavior over the huge load range and an additional output for driving the bulk terminal of the output transistor. Therefore, concurrent FBB and bulk modulation were implemented without any additional amplifier. An adequate stability margin was achieved over the load, supply, temperature range, and process corner by means of a UGF-tracking compensation circuit, which, as additional benefits, boosts the PSR of the LDO with respects to other compensation techniques.

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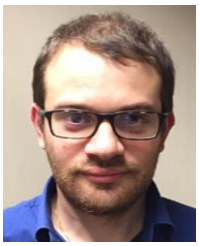

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